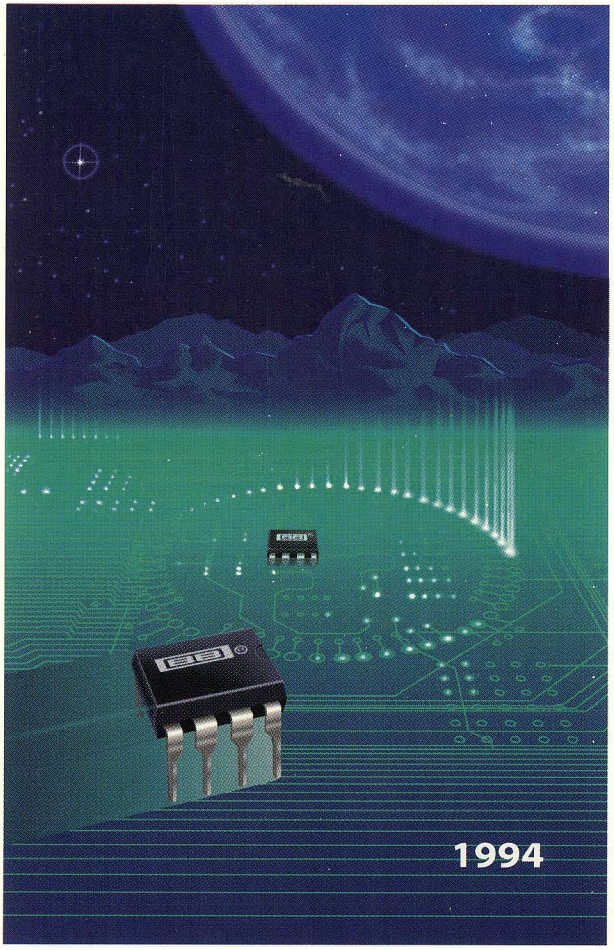
BURR-BROWN



APPLICATIONS HANDBOOK

BURR-BROWN ISO9001 CERTIFIED

BURR-BROWN®

BURR-BROWN®

Burr-Brown IC Applications Handbook

LI-459

Printed in USA

Burr-Brown Corporation
International Airport Industrial Park

Mailing Address:
PO Box 11400
Tucson, AZ 85734

Street Address:
6730 S. Tucson Blvd.
Tucson, AZ 85706

Tel: (602) 746-1111 • Twx: 910-952-1111 • FAX: (602) 889-1510
Cable: BBRCORP • Telex: 066-6491

For immediate Product Information or Technical Assistance, call
1-800-548-6132
in the USA.

Outside the USA,
FAX 1-602-889-1510.

About Burr-Brown

Burr-Brown Corporation is an international leader in the design and manufacture of precision microcircuits and microelectronic-based systems for use in data acquisition, signal conditioning, and control applications throughout the world.

The Company's products range from precision linear integrated circuits to data collection systems and personal computer instrumentation. The Company's integrated circuit components are used in analog and digital signal processing applications found in medical and scientific instrumentation, factory automation, automatic test equipment, process control, and consumer products such as electronic musical instruments and professional audio equipment.

Company Facts

- Founded in 1956.
- Corporate headquarters: Tucson, Arizona.
- 1404 employees.
- 1000+ products.
- Manufacturing and technical facilities in: Tucson, Arizona; Atsugi, Japan; Livingston, Scotland.
- 10 North American direct sales offices, 130 sales representatives and distributors in 180+ locations.
- International sales and distribution subsidiaries in Austria, France, Germany, Italy, Japan, the Netherlands, Switzerland, and the United Kingdom; 26 sales representatives throughout the rest of the world.
- Over 200 sales and service staff worldwide.

Burr-Brown Receives ISO9001 Certification in U.S. and Europe

In September 1993, Burr-Brown Corporation received ISO9001 certification in the United States and Europe, simultaneously. In the United States, registration is recognized through the AT&T Quality Registrar by the Registration Accreditation Board (RAB). Certification is accepted through the Electronics Industries Quality Registrar by the Dutch Registration Board (RCV) in Europe.

ISO9001 is the international standard for assessing the quality systems of companies that design, manufacture, and test products. Adopted by 91 member countries, it's the international quality standard for manufacturing, trade, and communications industries. Certification indicates that a formal quality system exists for all processes and that these processes are audited on a timely basis.

Table of Contents

ANALOG-TO-DIGITAL CONVERTERS

DATA CONVERTERS

INSTRUMENTATION AMPLIFIERS

ISOLATION AMPLIFIERS

OPERATIONAL AMPLIFIERS

POWER OPERATIONAL AMPLIFIERS

MULTIPLEXERS

REFERENCES

SPECIAL FUNCTIONS

VOLTAGE-TO-FREQUENCY CONVERTERS

Or, Call Customer Service at 1-800-548-6132 (USA Only)

BURR-BROWN® APPLICATION BULLETIN

Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

DYNAMIC TESTS FOR A/D CONVERTER PERFORMANCE

This article describes useful theory and techniques for evaluating the dynamic performance of A/D converters. Four techniques are discussed: (1) beat frequency, (2) histogram analysis, (3) sine wave curve fitting, and (4) discrete finite Fourier transform.

The key to confidence in the quality of a waveform recorder is assurance that the analog-to-digital converter (ADC) encodes the signal without degrading it. Dynamic tests that cover the frequency range over which the converter is expected to operate can provide that assurance. The results of the dynamic tests give the user a model of resolution versus frequency for the recorder. More elaborate models of failure mechanisms can be obtained by varying the conditions of the tests.

All of the dynamic tests used for the 5180A Waveform Recorder use sine waves as stimulus. Sine waves were chosen primarily because they are the easiest to generate in practice at the frequencies of interest with adequate fidelity. While it may be possible to generate a square wave, for example, whose function is known to the 10-bit resolution of the 5180A, no square wave generators exist that can guarantee the same waveshape to 10-bit resolution at 10MHz from unit to unit. Another motivation for choosing a sine wave stimulus is the simple mathematical model a sine function provides for analysis. This benefit greatly simplifies the algorithms used for data analysis.

Four dynamic tests for waveform recorder characterizations are presented here: beat frequency testing[1] histogram analysis [2] sine wave curve fitting,[3,4] and discrete finite Fourier transform.[5] The last three tests operate in the same way. A sine wave source is supplied to the waveform recorder and one or more records of data are taken. A computer is then used to analyze the data. The tests differ primarily in the analysis algorithms and consequently in the sort of errors brought to light. Critical to the success of these tests is the purity of the sine wave source. Synthesized sources are necessary to provide the short-term and long-term stability required by the dynamic range of the ADC. Passive filters (a six-pole elliptical filter is used for 5180A tests) are required to eliminate harmonic distortion from the source.

These tests provide the most stressful conditions for the ADC with the input signal amplitude at full scale. Generally speaking, nonlinear effects increase more quickly than the signal level increases because of the nonideal large-signal DC behavior of the ADC components and the higher slew rates large amplitudes imply.

BEAT FREQUENCY TESTING

The beat frequency and envelope tests are qualitative tests that provide a quick, simple visual demonstration of ADC dynamic failures. An input frequency is selected that provides worst-case range changes and maximal input slew rates that the ADC is expected to see in use. The output is then viewed on a display in real time.

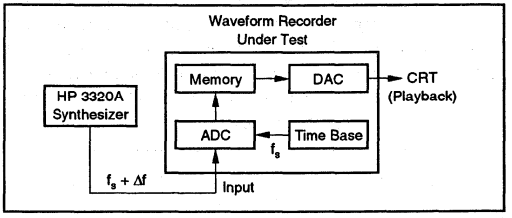


FIGURE 1. Beat Frequency Test Setup.

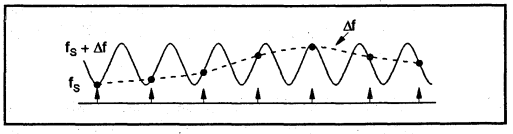


FIGURE 2. When the Input Frequency is Close to the Sample Rate f_S, the Encoded Result is Aliased to the Difference or Beat Frequency, Δf.

The name "beat frequency" describes the reasoning behind the test. The input sinusoid is chosen to be a multiple of the sample frequency plus a small incremental frequency (Figure 1). Successive samples of the waveform step slowly through the sine wave as a function of the small difference or beat frequency (Figure 2). Ideally, the multiplicative properties of sampling would yield a sine wave of the beat frequency displayed on the waveform recorder's CRT. Errors can be seen as deviations from a smooth sine function. Missing codes, for example, appear as local discontinuities in the sine wave. The oversize codes that accompany missing codes are seen as widening in the individual codes appearing on the sine wave. By choosing an arbitrarily low beat frequency, a slow accurate DAC may be used for viewing the test output. For best results, the upper limit on the beat frequency choice is set by the speed with which the beat frequency walks through the codes. It is desirable to have one or more successive samples at each code. This

alleviates the settling constraint on the DAC and ensures that the display covers all possible code failures. For a 20MHz sample rate and a 10-bit ADC, this implies a 3kHz maximum beat frequency for a minimum of one sample per code bin.

Although the usual input frequency for a beat frequency test is near the sample rate, the analog bandwidth of the ADC may be measured by setting the carrier to a number of different multiples of the sample rate. The band limit is observed as a rolloff in amplitude as the carrier frequency is increased.

The envelope test differs from the beat frequency test in the choice of input frequency that the ADC encodes. Instead of a multiple of the sample frequency, an input frequency near one-half the sample rate is used. Now the ideal output is two out-of-phase sine waves at the beat frequency (Figure 3). This means that successive samples can be at the extreme ends of the ADC range, which is useful for examining slew problems that might not appear when successive samples are at adjacent codes. To avoid placing the same stress on the DAC used for display, a bank of D flip-flops removes every other sample before the data arrives at the DAC. Thus only one phase of the beat frequency remains.

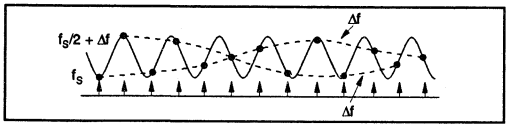


FIGURE 3. When the Input Frequency is Near One-half the Sample Rate, the Envelope of the Difference Frequency Results.

Figure 4 shows 5180A beat frequency test results for a 10.0031MHz input sine wave sampled at 10MHz. For comparison, Figure 5 shows a 10.0031MHz sine wave being sampled at 10MHz by a commercially available 8-bit, 20MHz ADC.

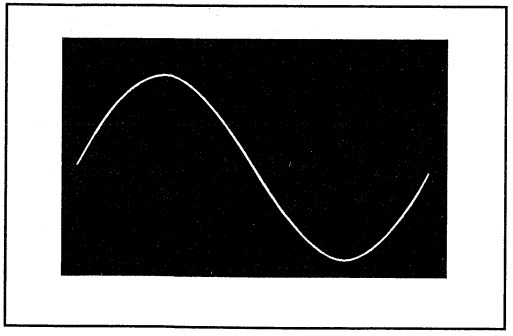


FIGURE 4. A Beat Frequency Display Produced by the 5180A Waveform Recorder with a 10.0031MHz Input Frequency and a 10MHz Sample Rate. The smooth sine wave indicates freedom from dynamic errors.

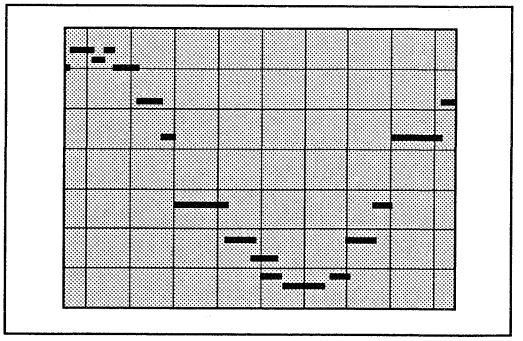


FIGURE 5. A Beat Frequency Display for a Commercially Available 10MHz, 8-Bit ADC with a 10.0031MHz Input.

HISTOGRAM TESTING

A sine-wave-based histogram test provides both a localized error description and some global descriptions of the ADC. Using the histogram test, it is possible to obtain the differential nonlinearity of the ADC, to see whether any missing codes exist at the test frequency, and to get a measure of gain and offset at the test frequency. Of the sine-wave-based tests presented here, the histogram test yields the best information about individual code bin size at an arbitrary frequency.

A statistically significant number of samples of the input sinusoid are taken and stored as a record (Figure 6). The frequency of code occurrence in the record is then plotted as a function of code. For an ideal ADC, the shape of the plot would be the probability density function (PDF) of a sine wave (Figure 7) provided that the input and sample frequencies are relatively independent. The PDF of a sine wave is given by:

$$p(V) = \frac{1}{\pi\sqrt{A^2 - V^2}}$$

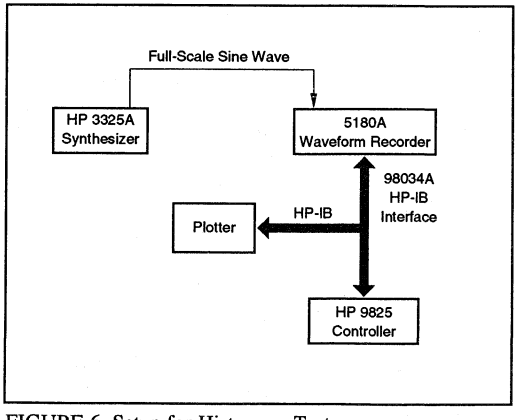


FIGURE 6. Setup for Histogram Test.

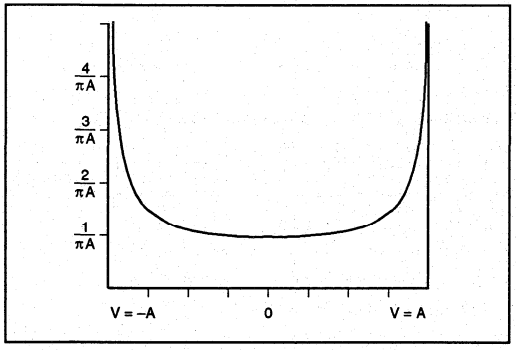


FIGURE 7. Sine Wave Probability Density Function.

Where A is the sine wave amplitude and V is the independent variable (voltage). For a real ADC, fewer than the expected number of occurrences for a given code bin indicates that the effective code bin width is smaller than ideal at the input frequency.(1) No occurrences indicate that the code bin width is zero for that input. A greater-than-expected number of occurrences implies a larger-than-ideal code bin width.

What is a statistically significant number of samples? We can determine significance from probability theory. For a given input PDF and record size, each bin of an ideal ADC has an expected number of occurrences and a standard deviation around that expectation. The confidence that the number of occurrences is close to the expectation is equal to the probability that the occurrences fall within the appropriate number of standard deviations. The ratio of the standard deviation to the expectation (and thus the error for a given confidence) decreases with more samples. To get the confidence for the entire range, the probabilities for all codes lying within the desired error are multiplied together.

For an ideal 10-bit ADC, 100,000 samples would give us a 12% confidence that the peak deviation from the input PDF is less than 0.3LSB and a 99.9% confidence that the peak deviation is less than 0.5LSB. The notion of confidence relies on the input's being a random process. We can model the sine wave input as random process only if the input and sample frequencies are relatively independent.

The specification of greatest interest that can be calculated using the histogram test is differential nonlinearity. Differential nonlinearity is a measure of how each code bin varies in size with respect to the ideal:

$$\text{Differential Nonlinearity} = \frac{\text{actual P (nth code)}}{\text{ideal P (nth code)}} - 1$$

Where actual P(nth code) is the measured probability of occurrence for code bin n, and ideal P(nth code) is the ideal probability of occurrence for code bin n. The code bin number n goes from 1 to 2^N, where N is the number of ADC bits. Using the probability of occurrence eliminates dependence on the number of samples taken. To calculate the probability for each code in the actual data record the number of occurrences for each code is divided by the number of samples in the record. The ideal probability of occurrence is what an ideal ADC would generate with a sine wave input. For each code bin, this is the integral of the probability density function of a sine wave over the bin:

$$P(n) = \frac{1}{\pi}\left[\sin^{-1}\left(\frac{B\left(n-2^{N-1}\right)}{A2^N}\right) - \sin^{-1}\left(\frac{B\left(n-1-2^{N-1}\right)}{A2^N}\right)\right]$$

Where n is the code bin number, B is the full-scale range of the ADC, and N is the number of ADC bits. To avoid large differences in code probability caused by the sinusoid cusp, a sine wave amplitude A is chosen that slightly overdrives the ADC.

A judicious choice of frequency for the input sinusoid in this test is necessary for realistic test results. An input frequency that is a submultiple of the sample frequency violates the relative independence criterion and will result in sampling of the same few codes each input cycle. Using an input frequency that has a large common divisor with the sample frequency generates similar problems since the codes repeat after each cycle of the divisor frequency. Ideally, the period of the greatest common divisor should be as long as the record length.

A 5180A histogram is shown in Figure 8 for an input sine wave at 9.85MHz. For comparison, Figure 9 shows data from a commercially available, 8-bit 20MHz ADC for an input sine wave at 9.85MHz, while Figure 10 shows data from an 8-bit, 100MHz ADC taken at 9.85MHz.

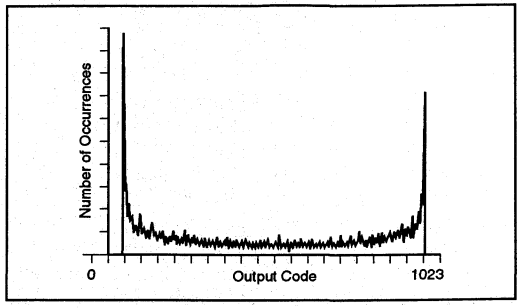


FIGURE 8. A 100,000-sample Histogram for a 5180A with a 9.85MHz Sine Wave Input. All Discontinuities are Less Than 1LSB.

NOTE: (1) Histogram testing can be thought of as a process of sampling and digitizing the input signal and sorting the digitized samples into bins. Each bin represents a single output code and collects samples whose values fall in a specific range. The number of occurrences or samples collected in each bin varies according to the input signal. If N is the number of ADC bits, there are 2^N bins. Ideally, if B is the full-scale range of the ADC in volts, each bin corresponds to a range of sample sizes covering $B/2^N$ volts. In a real ADC, the bins may not all have the same width.

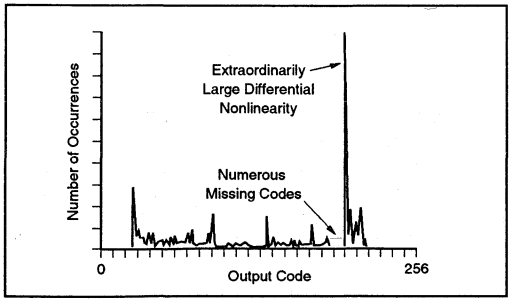


FIGURE 9. A 100,000-sample Histogram Plot for a Commercially Available 20MHz, 8-bit ADC with a 9.85MHz Input. Large differential nonlinearities and numerous missing codes are apparent.

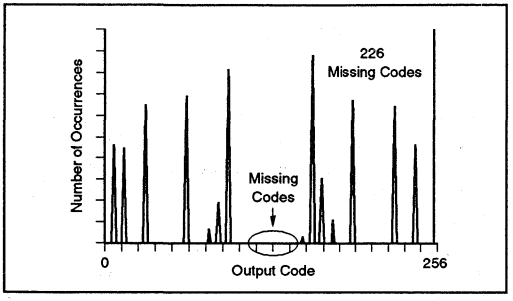


FIGURE 10. A 100,000-sample Histogram Plot for a 100MHz, 8-bit ADC with a 9.85MHz Input Sampled at 20MHz. Extremely large differential nonlinearities and numerous missing codes are apparent.

CURVE FITTING

The curve-fit test is a global description of the ADC. This means that the errors measured by the test are averaged to give a general measurement of the ADC transfer function. The result of this test is a figure of merit called the number of effective bits for the ADC. The effective bit number is a general measure of how much an ADC's nonlinearity has impaired its usefulness at a given frequency.

The number of effective bits is obtained by analyzing a record of data taken from a sine wave source (Figure 11). The analysis consists of generating a sine wave in software that is a best fit to the data record. Any difference between the data record and the best-fit sine wave is assumed to be error (Figure 12). The standard deviation of the error thus calculated is compared to the error an ideal ADC of the same number of bits might generate. If the error exceeds the ideal, the number of effective bits exhibited by the ADC is less than the number of bits it digitizes. Errors that cause degradation in this test are nonlinear effects such as harmonic distortion, noise, and aperture uncertainty. Gain, offset, and phase errors do not affect the results since they are ignored by the curve-fit process.

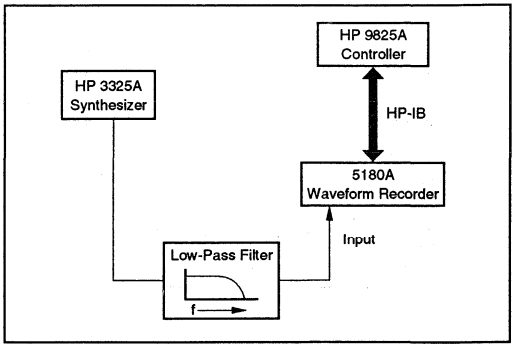


FIGURE 11. Setup for the Curve-fit Test and the Discrete Finite Fourier Transform (DFT) Test.

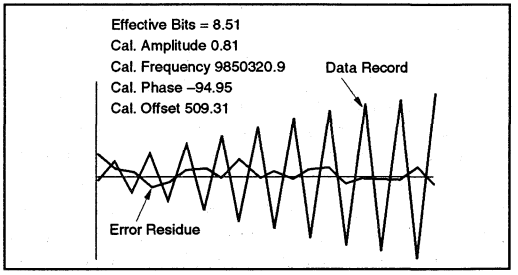


FIGURE 12. The First 20 Points of the Curve-fit Data Record and the Error Residue from a Fitted Sine Wave.

The number of effective bits is computed using expressions for average errors as follows:

$$\text{Effective bits} = N - \log_2\left(\frac{\text{actual rms error}}{\text{ideal rms error}}\right)$$

where N is the number of ADC bits. The ideal rms error is not actually computed for the input waveform, but is assumed to be the quantization noise exhibited by an ideal ADC with a uniform-probability-density (UPD) input such as a perfect triangle wave. The ideal error is found from the expectation of squared error for a rectangular distribution. A rectangular distribution is used since that represents a UPD taken over an ideal code bin. The result thus obtained is:

$$\text{Ideal rms error} = \frac{Q}{\sqrt{12}}$$

where Q is the ideal code bin width. Although the input sine wave is not a UPD function, the UPD assumption is still valid since it is locally applied over each code bin. The deviation from a UPD over each code bin is very small, so the errors in using sine waves to approximate UPD inputs are negligible.

The actual rms error is simply the square root of the sum of the squared errors of the data points from the fitted sine wave. The actual rms error is given by:

$$E = \sum_{k=1}^{m} \left[x_k - A\cos(\omega t_k + P) - C \right]^2 \quad (1)$$

where E is the actual rms error, x_k and t_k are the data points, m is the number of data points in the record, and the fitted sine wave parameters are amplitude A, frequency ω, phase P, and offset C.

Equation 1 is also used to find the best-fit sine wave by minimizing the error E. The error is minimized by adjusting the fit parameters: frequency, phase, gain, and offset. This is done by taking the partial derivative of E in Equation 1 with respect to each of the four parameters. The error minimum occurs when all of the derivatives are equal to zero. This gives the four simultaneous equations:

$$\sum_{k=1}^{m} x_k \cos(\omega t_k + P) = A \sum_{k=1}^{m} \cos^2(\omega t_k + P) + C \sum_{k=1}^{m} \cos(\omega t_k + P) \quad (2)$$

$$\sum_{k=1}^{m} x_k = A \sum_{k=1}^{m} \cos(\omega t_k + P) + nC \quad (3)$$

$$\sum_{k=1}^{m} x_k t_k \sin(\omega t_k + P) = A \sum_{k=1}^{m} t_k \cos(\omega t_k + P)\sin(\omega t_k + P) + C \sum_{k=1}^{m} t_k \sin(\omega t_k + P) \quad (4)$$

$$\sum_{k=1}^{m} x_k \sin(\omega t_k + P) = A \sum_{k=1}^{m} \cos(\omega t_k + P)\sin(\omega t_k + P) + C \sum_{k=1}^{m} \sin(\omega t_k + P) \quad (5)$$

Equations 2 and 3 result from gain and offset adjustments. These are substituted into the other two equations, 4 and 5, giving two nonlinear equations:

$$\frac{\sum_{k=1}^{m} (x_k - \bar{x}) t_k \sin(\omega t_k + P)}{\sum_{k=1}^{m} (x_k - \bar{x}) \cos(\omega t_k + P)} = \frac{\sum_{k=1}^{m} \left[\cos(\omega t_k + P) - \bar{a} \right] t_k \sin(\omega t_k + P)}{\sum_{k=1}^{m} \left[\cos(\omega t_k + P) - \bar{a} \right] \cos(\omega t_k + P)} \quad (6)$$

$$\frac{\sum_{k=1}^{m} (x_k - \bar{x}) \sin(\omega t_k + P)}{\sum_{k=1}^{m} (x_k - \bar{x}) \cos(\omega t_k + P)} = \frac{\sum_{k=1}^{m} \left[\cos(\omega t_k + P) - \bar{a} \right] \sin(\omega t_k + P)}{\sum_{k=1}^{m} \left[\cos(\omega t_k + P) - \bar{a} \right] \cos(\omega t_k + P)} \quad (7)$$

$$\text{Where } \bar{a} = \sum_{k=1}^{m} \cos(\omega t_k + P)$$

These are solved iteratively to give values for the parameters. The difference between the right and left sides of Equation 6 is defined as error parameter R and the difference between the right and left sides of Equation 7 is defined as error parameter S. An approximation algorithm using a first-order Taylor series expansion drives R and S to zero. This approximation algorithm requires an initial guess for frequency and phase close to the solution to ensure convergence to the best-fit sine wave. For frequency, the frequency of the generator output in Figure 11 is used as a guess. For phase, a guess is based on an examination of the data record by a software routine.

Although the result of this process is a single figure of merit, some enlightenment can be gained about the error components in the ADC by varying the test conditions. White noise produces the same degradation regardless of input frequency or amplitude. That is, the error term in Equation 1 is independent of test conditions for this sort of error. Another way of identifying noise in this test is by the randomness in the error residue, or the difference between the best-fit sine wave and the data taken.

Aperture uncertainty is identifiable because it generates an error that is a function of input slew rate. When this is the dominant error causing a low number of effective bits, the number of effective bits will vary linearly with both input frequency and amplitude. If the input waveform is sampled only at points of constant slew rate, such as zero crossings, then the aperture uncertainty corresponds to the amount that the effective bits decline as a function of slew rate.

Harmonic distortion is usually a nonlinear function of amplitude and frequency. Its distinguishing characteristic is the presence of the harmonics (or aliased harmonics if the fundamental is close to the Nyquist frequency) in the error residue. The amplitudes of the harmonics can be extracted by fitting the error residue with best-fit sine waves of the important harmonic frequencies. The impact of noise and aperture uncertainty in the presence of large distortion errors can be assessed by effective bit values and error residues with the fitted harmonics removed.

The greatest pitfall in the curve-fit test is using an input frequency that is a submultiple of the sample frequency. Since the same codes are sampled at exactly the same voltage each cycle, the locally uniform probability distribution assumption is violated. In the worst case, a submultiple of one-half, the quantization error would not be measurable at all. From a practical standpoint, this also defeats the global description of the test by sampling only a handful of codes.

Another potential pitfall is lack of convergence of the curve-fit algorithm. There are a few occasions where this can become a problem, such as when the data is very poor or the computational resolution is inadequate.

Figure 12 shows the error plot for a 5180A curve-fit test taken at a 9.85MHz input frequency. The number of effective bits associated with this error is 8.51.

FFT TESTING

The fast Fourier transform (FFT) is used to characterize an ADC in the frequency domain in much the same way that a spectrum analyzer is used to determine the linearity of an analog circuit. The data output for both techniques is a presentation of the magnitude of the Fourier spectrum for the circuit under test. Ideally, the spectrum is a single line

that represents the pure sine wave input and is devoid of distortion components generated by the circuit under test. There are, however, significant differences between the spectrum analyzer and ADC spectra because of the sampling operation of the ADC.

The Fourier transform of a signal x(t) that is continuous for all time is defined as:

$$X(f) = \int_{-\infty}^{\infty} x(t) e^{-i2\pi ft} dt$$

and includes the amplitude and phase of every frequency in x(t). The Fourier transform cannot be used in this form for an ADC, however, because x(t) is only digitized at a finite number of points, M, spaced Δt apart. Instead, the discrete finite transform (DFT) must be used. It is defined as:

$$XD(f) = \sum_{m=0}^{M-1} x(m\Delta t) e^{-i2\pi f(m\Delta t)} \Delta t$$

There are significant differences between X(f) and XD(f). While X(f) has infinite spectral resolution, XD(f) has a discrete frequency resolution of $\Delta f = 1/m\Delta t$ because of the finite number of points in the data record. The finite record size also accounts for another difference between X(f) and XD(f) whenever a nonintegral number of cycles of X(t) is contained in the record. Since the DFT assumes that the record repeats with a period of $M\Delta t$ (to satisfy the Fourier transform condition that x(t) be continuous for all time) sharp discontinuities at the points where the start of one record joins the end of the preceding record cause the spectral components of X(f) to be spread or smeared in XD(f).

The smearing, called leakage, can be explained as follows. The finite record size of x(t) can be considered the consequence of multiplying x(t) by a rectangular function having unity amplitude during the time period $M\Delta t$ that the record is acquired and zero amplitude elsewhere. Since multiplication of two functions in one domain (time, in this case) is equivalent to convolution in the other, the spectrum of XD(f) is derived by convolving X(f) with W(f), the Fourier transform of the rectangular function. W(f) is the familiar sinx/x function (see Figure 13 for |W(f)|), consisting of a main lobe surrounded by a series of sidelobes whose amplitudes decay at a 6dB-per-octave rate. It is these sidelobes that are responsible for leakage. Even if the spectrum of X(f) is a single line, the sidelobes of W(f) during the convolution smear the energy in the single line into a series of spectral lines spaced $1/M\Delta t$ apart whenever the frequency of x(t) is not an integral multiple of $1/M\Delta t$.

Leakage can be reduced by multiplying the data in the record by a windowing function that weights the points in the center of the record heavily while smoothly suppressing the points near the ends. Many different windowing functions exist that offer various tradeoffs of amplitude resolution versus frequency resolution. A function commonly used with sine waves is the Hanning window, defined by $|(1/2)(1 - \cos 2\pi t/M\Delta)|$. Notice in Figure 13 that both the window and its derivative approach zero at the two ends of the record and that the transform's main lobe is twice as wide as that of the rectangular function, while the amplitudes of the sidelobes decay by an additional 12dB per octave. The reduced level of the sidelobes reduces leakage, but the wider main lobe limits the ability to resolve closely spaced frequencies. Furthermore, the shape of the main lobe can attenuate the spectral amplitudes of X(f) by as much as 1.5dB. However, for the DFT testing to be described here, the Hanning window was selected as a good compromise between frequency and amplitude resolution.

The third difference between the spectra of X(f) and XD(f) is the limited range of frequencies displayed for XD(f). The sampling process causes the two-sided spectrum of X(f), symmetrical about the origin, to be replicated as the sampling frequency L and at all of its harmonics. If X(f) contains components that exceed $f_S/2$, then these components are folded back, or aliased, onto spectral lines below f_S, causing aliasing errors. The frequency $f_S/2$ is sometimes called the Nyquist frequency, referring to the Nyquist criterion, which requires the sampling rate to be twice the highest frequency present in the input signal to define the waveform uniquely.

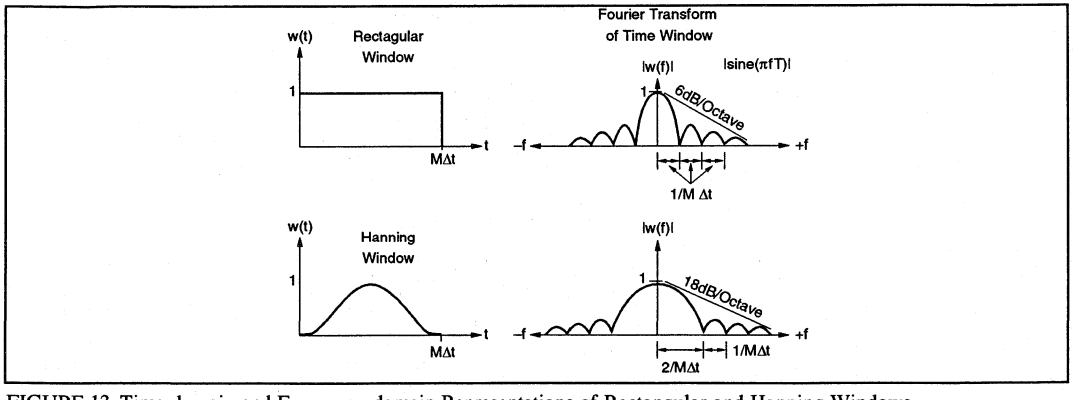


FIGURE 13. Time-domain and Frequency-domain Representations of Rectangular and Hanning Windows.

The result is that the spectrum of XD(f) is displayed only from DC to $f_S/2$ and the maximum input frequency must be limited to less than $f_S/2$ to avoid aliasing.

Figure 14 presents the magnitude of the spectra derived from the DFT for perfect 10-bit and 6-bit ADC's given a pure sinusoidal input. Useful information about the ADC's performance can be derived from three features of the spectra: the noise floor, the harmonic level, and the spurious level.

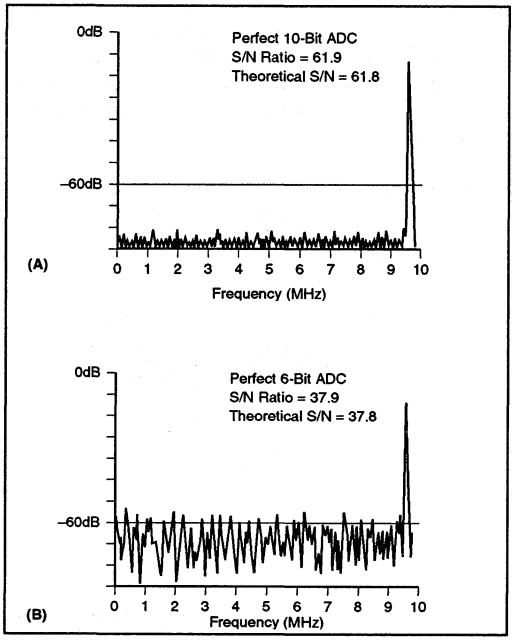


FIGURE 14. FFT Plots for 0.85MHz Data Quantized by Perfect 10-bit (a) and 6-bit (b) ADCs. The signal-to-noise ratio computed in each case agrees closely with the theoretical value of 6N + 1.8dB where N is the number of ADS bits.

Two classes of noise sources determine the level of the noise floor. The first is called quantization noise. This is the error, bounded by ±1/2LSB, that is inherent in the quantization of the input amplitude into discrete levels. As can be seen in Figure 14, even ideal ADCs have noise floors determined by quantization noise. The higher the number of bits, the smaller the error bound and, therefore, the lower the noise floor.

All real-life ADCs have noise floors that are higher than that solely from quantization noise. The second class of noise source includes wideband noise generated within the ADC, along with other sources. In a parallel-ripple ADC, for example, such things as misadjustment between the first-pass and second-pass ranges (exceeding the redundancy range) or inadequate DAC settling can cause localized code errors or differential nonlinearities in the ADC's status transfer function. Furthermore, localized code errors can increase in amplitude and in the number of codes affected under dynamic input conditions. Aperture jitter is another major source of dynamic error; the magnitude of this localized code error is dependent upon the slew rate of the input at the time of sampling. Each of these localized code errors can be modeled as a sharp discontinuity in the time domain that when transformed into the frequency domain results in a broad spectrum that raises the height of the noise floor above that caused by quantization noise alone.

The second feature of the DFT-derived spectrum that indicates an ADC's level of dynamic performance is the harmonic content. Static and dynamic integral nonlinearities cause curvature in the ADC's transfer function. If the input frequency f_{IN} is much lower than the Nyquist frequency ($f_S/2$), then the harmonic components will be in the expected locations: $2f_{IN}$, $3f_{IN}$, etc. If, on the other hand, the harmonics of f_{IN} are greater than $f_S/2$, then these frequencies will be aliased onto components below $f_S/2$. Take, for instance, a 20-megasample-per-second (f_S) ADC with an input of 9.85MHz. The second harmonic at 19.7MHz is aliased to 0.3MHz, the third harmonic at 29.55MHz is aliased to 9.55MHz, the fourth at 39.4MHz is aliased to 0.6MHz, and so on.

Care must be exercised in selecting the input frequency for the DFT test. An incorrectly chosen frequency can alias one of its harmonic components on to the fundamental and thereby understate the harmonic distortion (in the example above, an input of exactly 5MHz would place the third harmonic at the fundamental frequency). The input frequency should be chosen so that the harmonics are far enough away to be easily resolvable from the fundamental, whose energy has been spread into several adjacent bins ($1/M\Delta t$ locations) by the Hanning window. This accounts for the 0.15MHz offset from 10MHz used in the example of Figure 14.

The third feature of the DFT-based spectrum that is indicative of the ADC's level of dynamic performance is the spurious content. Spurious components are spectral components that are not harmonically related to the input. For example, a strong signal near the ADC may contaminate the ADC's analog ground somehow and thereby appear in the spectrum. The nearby signal will not only appear as itself, but because of nonlinearities within the ADC, can combine with the input signal to form sum and difference terms resulting in intermodulation distortion.

The combined effects of noise floor, harmonic distortion and spurious errors are reflected in the ADC's rms signal-to-noise ratio, which can be derived from the DFT magnitude spectrum. The signal energy is determined by summing the energy in all the bins associated with the fundamental. The noise energy is the sum of the energy in all other bins. By taking the logarithm of the ratio of signal energy to noise energy and multiplying by 20, the signal-to-noise ratio for the ADC can be calculated. An ideal N-bit ADC having quantization noise only is theoretically known to have a signal-to-noise ratio equal to (6N + 1.8)dB, which sets an

upper bound. A signal-to-noise ratio below this ideal limit is indicative of errors of all types that the ADC produces.

The FFT test setup is presented in Figure 11. A full-scale sine wave of a properly chosen frequency is applied to the ADC under test. The low-pass filter ensures a spectrally pure input. A 1024-point record sampled at the maximum sampling rate is then taken and given to the computer, which calculates the DFT using an FFT algorithm. The spectral magnitude is plotted as a function of frequency.

Figure 15 shows the graphical outputs for the 5180 for full-scale sine wave input at 0.95MHz and 9.85MHz. As might be expected, the distortion increases with increasing frequency. Harmonic and spurious components are typically better than –60dBc below 1MHz and –54dBc at 9.85MHz. The latter spectrum at 9.85MHz is the frequency-domain representation for one of the most demanding tests of an ADC, called the envelope test which was described earlier.

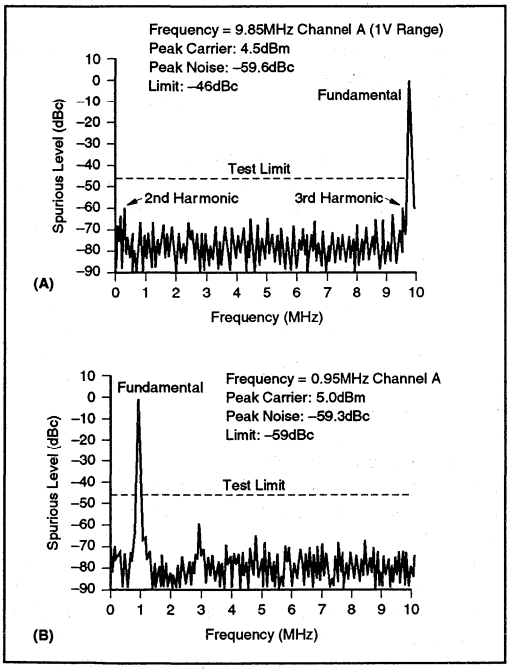


FIGURE 15. DFT Plots for the 5180A with Input Frequencies of 9.85MHz (a) and 0.95MHz (b). The low harmonic distortion indicates very low integral nonlinearity.

Figure 16 presents, for comparison, the test results for commercially available digitizers: a 20-megasample-per-second, 8-bit ADC and a 100-megasample-per-second, 10-bit ADC with a full-scale, 9.85MHz sine wave input, sampled at 20 megasamples-per-second. The numerous large harmonic components, both odd and even, are indicative of severe harmonic distortion errors resulting from integral nonlinearity in the transfer functions of both of these ADCs.

A rule of thumb has evolved that uses the DFT-based spectrum as a quick overview of an N-bit ADC's dynamic performance. If all harmonic and spurious components are at least 6N dB below the full-scale amplitude of the fundamental, then the ADC is performing satisfactorily, since each error component has a peak-to-peak amplitude smaller than an LSB. If, on the other hand, harmonic or spurious components are less than 6N dB down, or if the noise floor is elevated, then other tests can be performed that are better at isolating the particular integral and differential nonlinearity errors. In particular, the FFT test an be followed by the histogram test or the beat frequency test (or envelope test), as conditions warrant.

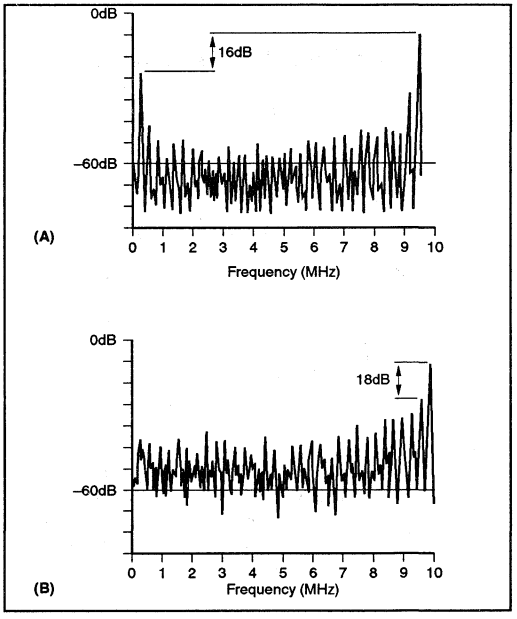


FIGURE 16. DFT Plots for a 20MHz, 8-Bit ADC (a) and a 100MHz, 8-Bit ADC (b). Full-scale input sine waves at 9.85MHz were sampled at a rate of 20MHz. The high levels of harmonic distortion indicate severe integral nonlinearities.

CONCLUSION

The four sine-wave-based ADC tests described provide information about the quality of any recorder. The tests may be used to isolate specific failures, even at high-speed and fine resolution (Figure 17). The tests are simple to run, requiring only a synthesized generator and an HP-IB computer.

ERROR	HISTORGRAM	DFT	SINE WAVE CURVE-FIT	BEST FREQUENCY TEST
Differential Nonlinearity	Yes—shows up as spikes	Yes—shows up as elevated noise floor	Yes—part of rms error	Yes
Missing Codes	Yes—shows up as bins with 0 counts	Yes—shows up as elevated noise floor	Yes—part of rms error	Yes
Integral Nonlinearity	Yes—(could be measured directly with a highly linear ramp waveform)	Yes—shows up as harmonics of fundamental aliased into baseband	Yes—part of rms error	Yes
Aperture Uncertainty	No—averaged out. Can be measured with "locked" historgram	Yes—shows up as elevated noise floor	Yes—part of rms error	No
Noise	No—averaged out. Can be measured with "locked" histogram	Yes—shows up as elevated noise floor	Yes—part of rms error	No
Bandwidth Errors	No	No	No	Yes—used to measure analog bandwidth
Gain Errors	Yes—shows up in peak-to-peak spread of distribution	No	No	No
Other Errors	Yes—shows up in offset of distribution average	No	No	No

FIGURE 17. Summary of the Errors Exposed by the Dynamic Tests.

REFERENCES

1. D.J. Packard, "Beat Frequency Testing of Real Time A/D Converters," Workshop on High Speed A/D Conversion, Portland, Oregon, February, 1980.
2. H.U. Koller, "New Criterion for Testing Analog-to-Digital Converters for Statistical Evaluation," *IEEE Transactions on Instrumentation and Measurement*, Vol. IM-22, pp. 214-17, September, 1973.
3. R. Potter, "Least-Squares Estimation of Sinusoidal Parameters from Measured Data," Hewlett-Packard internal memo, June, 1974.
4. L. Ochs, "Measurement and Enhancement of Waveform Digitizer Performance," IEEE International Convention, Boston, May, 1976.
5. R.N. Bracewell, *The Fourier Transform and Its Applications*, McGraw-Hill, New York, 1965.

BURR-BROWN® APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

INCREASING ADC603 INPUT RANGE

By R. Mark Stitt, (602) 746-7445

The ADC603 is a 10MHz, 12-bit analog-to-digital converter with a ±1.25V input range. Many applications call for a higher input range such as ±2.5V. A resistor divider can be used as an input attenuator to increase the input range. The OPA620 can be used to buffer the input attenuator for high-source-impedance applications. Suggested component values and measured performance results are shown in this bulletin.

Since the ADC603 has a high-impedance input, a simple voltage divider as shown in Figure 1 can be used to increase its voltage input range. The source impedance of the divider as seen by the ADC603 is $R_1 \parallel R_2$ (the parallel combination of R_1 and R_2). A divider source impedance of 50Ω is recommended since it has been shown to give consistently good results. If a higher divider input impedance is needed and adding a buffer is not viable, source impedances up to 500Ω should give satisfactory results. If hardware gain trim is needed, select the next higher 1% resistor value for R_1 and use a 10kΩ multi-turn trim pot in parallel with R_1 for gain trim.

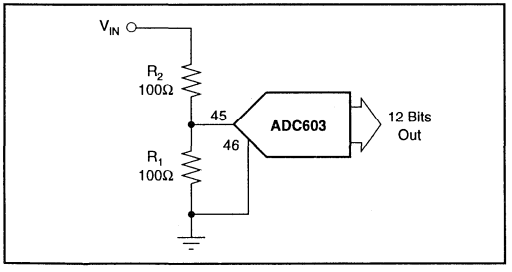


FIGURE 1. ADC603 12-Bit ADC with 2/1 Input Attenuator to Provide ±2.5V Input Range.

If an input impedance of 50Ω to the circuit is needed as a termination, add a third resistor as shown in Figure 2. The three-resistor approach improves accuracy by placing the majority of the termination power dissipation in the third resistor. This minimizes error-producing self heating in the precision divider network. Pay attention to the power rating for R_3. For a ±10V input, R_3 must be rated 2W.

If a high input impedance is needed, drive the divider with a unity-gain-connected OPA620 buffer amp as shown in Figure 3. The OPA620 can be used for inputs as high as ±3V.

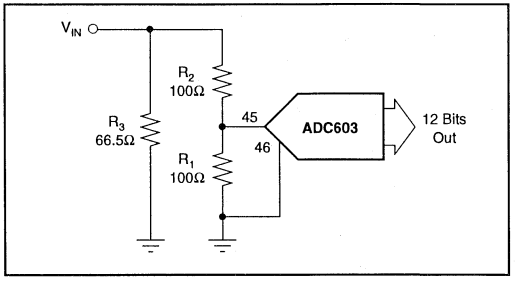


FIGURE 2. ADC603 12-Bit ADC with Three-Resistor 2/1 Input Attenuator to Provide ±2.5V Input Range and 50Ω Termination Impedance.

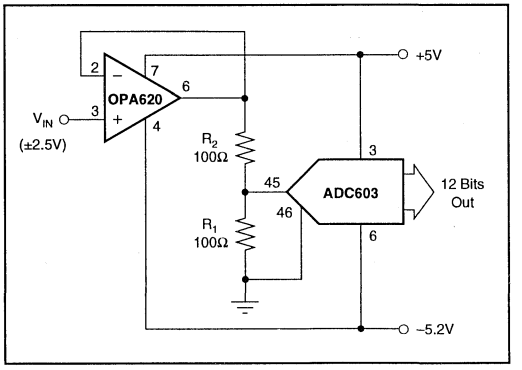


FIGURE 3. ADC603 12-Bit ADC with 2/1 Input Attenuator to Provide High Input Impedance ±2.5V Input Range.

Equations for determining recommended resistor values are:

$R_1 = 50\Omega \bullet N/(N - 1)$

$R_2 = (N - 1) \bullet R_1$

$R_3 = 50\Omega \bullet (R_1 + R_2)/(R_1 + R_2 - 50\Omega)$

Where:

R_1, R_2, R_3 are in Ω

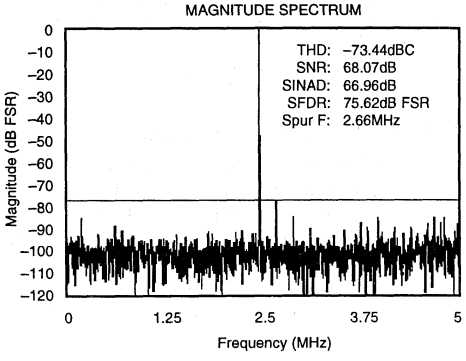
N = input divider ratio

The table below shows recommend resistor values for selected input ranges.

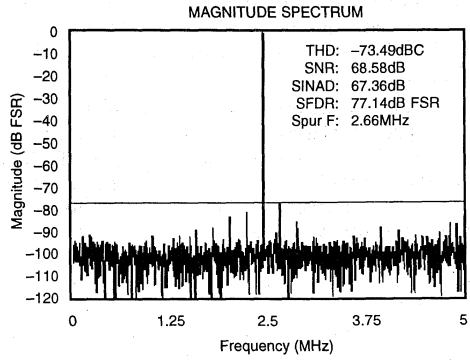
INPUT RANGE (V)	DIVIDER (1/N)	R_1 (Ω)	R_2 (Ω)	R_3 (Ω)
±2	1/1.6	133	80.6	64.9
±2.5	1/2	100	100	66.5
±3	1/2.4	86.6	121	66.5
±5	1/4	66.5	200	61.9
±10	1/8	56.2	397	56.2

TABLE I. Resistor Values for Selected Input Attenuators.

The spectral plots compare a standard ±1.25V input ADC603 to a ±2.5V input, OPA620 buffered ADC603 per Figure 3. In both cases, the circuit is sampling a 2.5MHz signal at 10MHz. The results show that the spurious-free dynamic range of the boosted circuit is as good as for the standard circuit. If anything, the boosted circuit has better performance (77dB vs 76dB). The ADC603 seems to perform slightly better when driven by the purely resistive 50Ω divider impedance instead of the complex impedance of the cable and signal generator.



Plot 1. Spectral plot of standard ADC603 sampling a ±1.25V, 2.5MHz input signal at 10MHz showing 75.6dB SFDR.



Plot 2. Spectral plot of increased input range (per Figure 3) ADC603 sampling a ±2.5V, 2.5MHz input signal at 10MHz showing 77.1dB SFDR.

FIGURE 4. Spectral Plots.

BURR-BROWN® APPLICATION BULLETIN

Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

TIPS FOR USING THE ADS78XX FAMILY OF A/D CONVERTERS

INHERENT OVERVOLTAGE PROTECTION

The input to each of the members of the ADS Family (ADS7804/05/06/07/08/09/10/19, so far) is a resistor divider network, converting the input signal to the range used internally. This resistor divider offers inherent overvoltage protection, which will often simplify analog circuitry.

In applications where the analog signal conditioning uses ±12V supplies (or higher), the ADS divider network eliminates potential problems if the op amp driving the ADS fails and drives the ADS input to the +12V rails. It also protects if the circuitry in front of the ADS is powered up before the ADS itself. Older ADCs on the market might fail under either of these conditions, requiring additional protection which can itself affect the accuracy and performance of the whole system.

In the "Absolute Maximum" section of the data sheets, we show that the input pins can go to ±25V. From our testing we know this is very conservative, but it is still much higher than the supplies commonly used for analog signal conditioning.

NOISE ON 16-BIT A/D CONVERTERS

Ground the input of a good 12-bit converter, convert a few thousand times, and you should see only 1-2 output codes (2 if the input is close to a transition). The same test on any 16-bit successive approximation (SAR) A/D will yield multiple codes due to noise. This is true for all 16-bit SAR A/Ds including ours.

Data sheets should indicate expected noise for DC inputs. We call it "Transition Noise", and show a typical value in the specification table. The ADS7807 data sheet shows a typical rms transition noise of 0.8LSBs. As a rule, you can multiply rms noise figures by 6 to approximate expected peak-to-peak noise, so the ADS7807 typical transition noise should be about 5LSBs. This means that if you ground the input and run a thousand conversions, you should see about 5 different output codes, which is in fact what we see. The worst-case transition is at the major-carry (0V for a ±10V range); we recently ran 30,000 conversions with the input to an ADS7807 grounded and in fact saw only 7 output codes (one of which occurred 0.03% of the time).

NOISE EFFECTS ON DNL AND INL

The previous discussion on noise raises the question of how Integral Linearity Error (ILE) or Differential Linearity Error (DLE) can be measured and guaranteed to levels tighter than the noise of the part. What does a maximum of +1.5LSB error mean when any signal conversion could output results +2 or +3LSBs different from the ideal, due to noise? The answer is fairly simple: to measure actual linearity of a specific 16-bit A/D, both we and our competition look below the noise floor of the parts.

The main tool for achieving this is averaging. For the ADS Family, when we are checking ILE, we put in a known voltage from a very stable reference D/A, perform 256 conversions, and average the results to determine the linearity of that point. Incidentally, when we say that ILE is ±3LSBs or ±1.5 LSBs max, we actually use tighter limits in our test program. The guardband insures that we take into account the absolute accuracy of our reference D/A (which is itself regularly calibrated) plus repeatability constraints on any one test system and variations between test systems.

This also raises the question of how much averaging is needed to guarantee a certain confidence in the A/D converter. For every doubling in the number of averages, transition noise will decrease by a factor of 1 over the square root of two. Averaging 64 conversion from an ADS7807 would result in transition noise adding ±1/10 of an LSB of uncertainty (one σ) to the specified INL and DNL.

BURR-BROWN®
APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

CDAC ARCHITECTURE PLUS RESISTOR DIVIDER GIVES ADC574 PINOUT WITH SAMPLING, LOW POWER, NEW INPUT RANGES

George Hill (602) 746-7283

Modern successive-approximation analog-to-digital converter ICs are replacing older current-mode D/A structures with capacitor arrays, called CDACs (for Capacitor D/A). This change makes it easier to combine the analog components of the converter with the digital elements in standard CMOS structures. Additionally, the capacitor input structure adds inherent sampling to the A/D, at a time when more and more A/D applications are involved in signal processing.

This application note compares basic current-mode successive approximation A/Ds with CDAC-based architectures, and shows how adding a resistor divider network to the CDAC input permits the Burr-Brown ADS574 and ADS774 to fit existing ADC574 sockets. It then goes on to describe some new analog input voltage ranges available on these parts due to the resistor network and CDAC approach.

The ADS574 and ADS774 plug into ADC574/674/774 sockets and handle all of their standard input ranges (0V to 10V, ±5V, ±10V, and 0V to 20V), as discussed in their full data sheets. They can operate from standard ±15V and +5V supplies, or from a single +5V supply. The input divider structure makes it possible to take advantage of this +5V supply operation to build complete data acquisition systems that run from a single +5V supply, with several different input ranges pin-selectable.

TRADITIONAL ADC574 INPUT STRUCTURE

Let's start by taking a look at the input ranges on the traditional ADC574, the most widely used 12-bit A/D in the world. Figure 1 shows the standard input divider network and comparator/current D/A structure used to implement the front end of this successive approximation A/D.

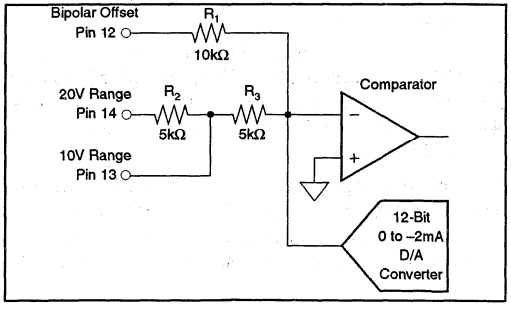


FIGURE 1. Traditional ADC574 Input Structure.

These three pins allow the selection of four different analog input ranges: 0V to +10V, 0V to +20V, ±5V, and ±10V. The simplicity of this circuit takes advantage of the virtual ground at the negative input to the comparator at the end of the successive approximation process, when the negative input to the comparator is very close to 0V.

The internal current D/A in the ADC574 has a unipolar output of 0mA to –2mA, so that it can balance out the 0mA to 2mA generated by full scale analog inputs (20V across 10kΩ or 10V across 5kΩ.) By grounding pin 12, a unipolar 0V to 20V input range is achieved by driving pin 14 and leaving pin 13 unconnected. Reversing pins 13 and 14 sets up the ADC574 for a 0V to 10V input range.

Connecting pin 12 to the 10V, reference provided on an ADC574 injects an offset that allows pins 13 or 14 to handle bipolar input ranges of ±5V or ±10V, respectively. The current injected by the reference at pin 12 adds to the input current generated by the analog input signal to insure that the unipolar current flow from the internal current D/A need only be unipolar.

During conversion, the analog signal conditioning in a system must hold the input stable (using a sample/hold amplifier or processing slow signals such as thermocouples.) The successive approximation logic tests the current D/A in various settings until the current sinked into the D/A balances the current generated by the analog input signal (plus the current from the Bipolar Offset resistor in bipolar ranges) to within ±1/2 LSB.

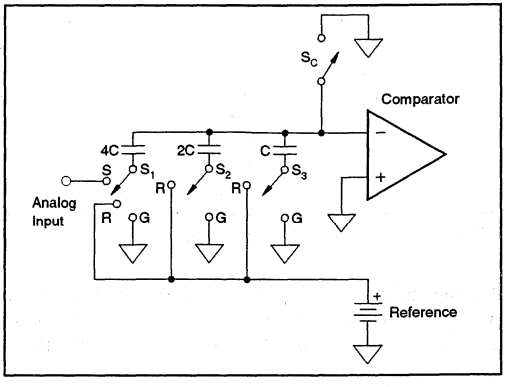


FIGURE 2. Simplified 3-bit Switched Capacitor Array A/D.

BASIC SWITCHED CAPACITOR ARRAY A/D

By comparison, Figure 2 shows a typical input structure for a switched capacitor array used to implement a successive approximation A/D in CMOS. For simplification, a 3-bit converter is shown in Figure 2. When not converting, switch S_1 (to the MSB capacitor) is in the "S" position so that the charge on the MSB capacitor is proportional to the voltage level of the analog input signal. Switches S_2 and S_3 are in the "G" position, and switch S_C is closed, setting the comparator input offset to zero. A convert command opens switches S_1 and S_C, to trap a charge on the MSB capacitor and to float the comparator input. During the conversion, switches S_1, S_2 and S_3 are successively tested in various "R" and "G" positions to find the combination that sets the comparator input closest to 0V, thus balancing the charge.

For our discussion, the critical condition occurs during the sampling phase, when the analog charge proportional to the analog input voltage is captured. The analog input is driving a capacitor, effectively an extremely high impedance. This is just the opposite of driving a virtual ground, which is where the comparator input in traditional ADC574s is at the end of the conversion process.

ADS574 INPUT STRUCTURE

The desire to use a CDAC architecture to develop an A/D that can drop into ADC574 sockets was a major design challenge. Figure 3 shows the resistor divider network that meshes the analog input ranges of the standard ADC574 with a CDAC to produce the ADS574, a single-supply, sampling A/D that plugs into most existing ADC574 sockets with no changes required to either hardware or software.

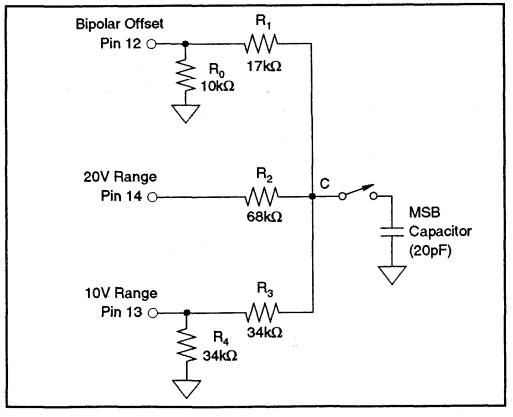


FIGURE 3. ADS574 Input Structure.

The full-scale voltage range for the MSB input capacitor on the ADS574 was designed to be 0V to +3.33V. This meant that the input resistor divider network had to provide the standard ADC574 input ranges using the same three pins, and also scale the voltage at the MSB capacitor to the 0V to 3.33V range. The on-chip laser-trimmed nichrome input resistors solve the problem of handling 20V analog signals, unipolar or bipolar, in a converter using a single +5V supply and ground as its rails.

The 5V supply means that the ADS574 does not provide a 10V reference, but instead provides a 2.5V reference output. The Bipolar Offset input, pin 12, had to be designed for this 2.5V reference, but also had to be designed to ensure that standard ADC574 offset adjust trim circuits produce similar trim results and range. This offset trim compatibility is the primary role of the 10kΩ resistor R_0 at pin 12.

For unipolar input ranges without offset trim circuits, standard ADC574s have pin 12 connected to analog common, which the ADS574 emulates. In the standard ADC574, R_1 in Figure 1 is essentially out of the equation for the input divider network as the comparator input approaches 0V during the successive approximation process. In the ADS574, R_1 in Figure 3 always plays a significant role.

For the 0V to 20V unipolar input range on the ADS574, as on the standard ADC574, pin 12 is grounded, pin 13 is left open, and the analog input is applied to pin 14. Since the input to the MSB capacitor on the ADS574 is very much higher than the input resistors, only R_1, R_2, R_3 and R_4 in Figure 3 determine the voltage at C for a given input voltage at pin 14. (The 10kΩ R_0 is grounded at both ends, and can thus be ignored.)

An analog input at pin 14 is divided by 6 at point C as follows:

Equation 1

$$V_C = \frac{(R3 + R4) \parallel R1}{R2 + [(R3 + R4) \parallel R1]} \cdot V_{IN}$$

$$V_C = 1/6\ V_{IN}$$

This matches a 0V to 20V input range at pin 14 to the 0V to 3.33V range required by the ADS574 internally.

In the unipolar 0V to 10V range, pin 12 is again connected to ground, and pin 14 is unconnected. This case is simpler to analyze, since neither R_2 nor R_4 have any effect on the voltage at C. In this case, the analog input at pin 13 is divided by 3 at point C.

The bipolar input ranges are also more complicated on the ADS574 than on standard ADC574s. The ADS574 uses the same external trimpots or fixed resistors already present in ADC574 sockets for bipolar offset, but works with the internal 2.5V reference.

For the ±10V input range without external offset trim, standard ADC574s have pin 12 connected to the +10V reference (internal or external) through a 50Ω resistor. Pin 13 is again left unconnected, and the analog signal to be

digitized is input at pin 14. The ADS574 uses the same input connections. As above, the input to the MSB capacitor on the ADS574 has very much higher impedance than the resistor divider network. Thus, in Figure 3, R_1, R_2, R_3, R_4, plus the reference voltage at pin 12, determine the voltage at C for a given input voltage at pin 14 (assuming the reference source impedance is much lower than R_1 and R_0).

An analog input voltage at pin 14 is divided and offset at point C as follows:

Equation 2

$$\frac{V_{IN} - V_C}{R_2} = \frac{V_C}{R_3 + R_4} + \frac{V_C - 2.5}{R_1}$$

Solving for V_C, the voltage at point C, in terms of V_{IN}, the voltage at pin 14, gives:

Equation 3

$$V_C = 1/6\ V_{IN} + 1.67$$

For a –10V input at pin 14, point C is again 0V, and a +10V input at pin 14 generates 3.33V at point C. The reference input at pin 12 sources current when the analog input at pin 14 is less than 1.67V, and sinks current when it is greater than 1.67V.

For the bipolar ±5V input range without offset trim, pin 12 is again connected to the reference (internal or external) through a 50Ω resistor on both the traditional ADC574 and the ADS574. In this case, pin 14 is left unconnected, so that R_2 has no effect on the voltage at point C. R_4 also has no effect. The voltage at point C is simply:

Equation 4

$$V_C = 1/3\ V_{IN} + 1.67$$

A –5V input at pin 13 generates 0V at point C, a 0V input generates 1.67V (half-scale), and +5V generates 3.33V (full-scale.)

NEW INPUT RANGES ALLOWED BY THE ADS574[1]

Because of the widespread use of the traditional ADC574, there exists large amounts of software and digital interface hardware built around this pinout. The ADS574 input structure lets this existing software and hardware be easily applied in systems requiring different analog input ranges. Since the ADS574 can operate from a single +5V supply, perhaps the most interesting optional input range is 0V to +5V. Figure 4 shows how to achieve this range. The analog input signal is driven, through a fixed 50Ω resistor, into pin 12 (the Bipolar Offset pin), with pin 14 (the 20V Range Input) grounded, and pin 13 (the 10V Range Input) unconnected. The input signal at pin 12 is divided by the network of $R_1 + (R_2 \parallel (R_3 + R_4))$. Point C is at the internal full-scale 3.33V when 5V is input at pin 12, and is 0V when 0V is input at pin 12. Using the ADS574 connected as shown in Figure 4 would allow building a complete sampling A/D system running off a single +5V supply, limited only by how close other analog input circuitry can get to ground or the supply.

Tests in the lab using the connections shown in Figure 4, and the other circuits shown below where pin 12 is used as an input, confirm the operation of these circuits, although with slight degradation in linearity. The ADS574 in these modes maintains 12-bit differential linearity, with No Missing Codes at the 12-bit level, but integral linearity is at the 10- to 11-bit level. The degradation from ideal performance has been traced to a circuit design that was required to maximize compatibility in existing ADC574 sockets. This circuit can easily be modified to enhance performance in these input ranges, if needed.

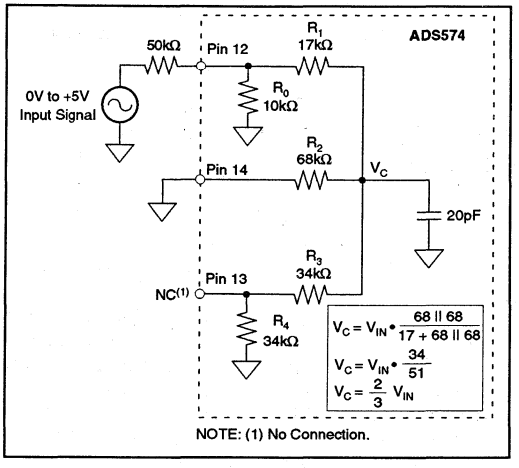


FIGURE 4. Connections for 0V to +5V Input Range.

Some operational amplifiers capable of running off a single +5V supply can swing closer to 0V than to the +5V supply. Figure 5 shows how to configure the ADS574 for a 0V to +3.33V input range to better utilize the dynamic range of such amplifiers. By connecting pins 12, 13 and 14 all to the input signal, there is no divider network between the input and point C, so that the input voltage will also be the voltage at point C. (Once again, this is based on the very high input impedance of the 20pF MSB capacitor internal to the ADS574.)

For bipolar signals in systems with supply voltages limited to ±5V, the connections in Figure 6 can be used to handle a ±2.5V input signal. The analog input signal is applied to pin 12, with pin 14 left unconnected. Connecting pin 13 to the

NOTE: (1) All of the input ranges described here are also available on the ADS774, since the input resistor divider network has the same ratios. The input impedance will be lower, but the ranges will be the same.

+5V supply offsets the voltage at point C generated by an input signal at pin 12 so that the voltage range at point C is again the 0V to 3.33V required internally. Obviously, any ripple or variation on the +5V supply line will feed straight through the divider network, and be converted by the ADS574. For this approach to work, the +5V supply needs to be stable enough to maintain the system accuracy required. If there is a stable +5V reference available in the system, it could also be used to generate the bipolar offset, and perhaps even power the ADS574, which consumes only 100mW maximum.

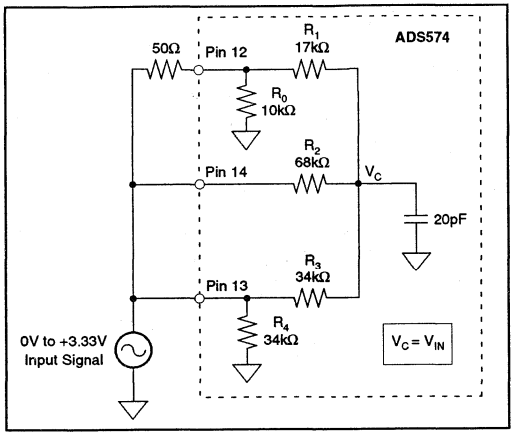


FIGURE 5. Connections for 0V to +3.33V Input Range.

For applications needing maximum integral linearity with a 0V to 5V input range, Figure 7 shows the optimal connections. This avoids the slight degradation of integral linearity mentioned above when pin 12 is used as an input pin, but sacrifices about 35% of the A/Ds output codes (the codes for inputs from 5V to 7.778V.) Using a K-grade ADS574 in this configuration will yield better than 11-bit resolution (2633 codes) and integral linearity from 0V to 5V, since it has ±1/2LSB integral linearly over the 0V to +7.778V input range.

The ADS574 input structure was optimized for compatibility with ADC574 sockets, and was not designed or characterized for these additional input ranges. However, the simplicity of the input resistor divider network makes it straight-forward to see how they work. For all of these additional input ranges, the standard trim circuitry for gain adjust (not discussed above but described in the ADS574 data sheet) can still be used to adjust full-scale range. To trim offset error, it is probably advisable to trim elsewhere in the system. In most systems, there will be an op amp in front of the ADS574, and it should be simple to trim out the system offset by adjusting the offset of this amplifier.

CMOS VS BiCMOS

It should be noted that the CDAC architecture used in the ADS574 and ADS774 is not the only possible way to implement a monolithic sampling A/D in the standard ADC574 pinout. One alternative is the BiCMOS-based Analog Devices AD1674. Analog Devices chose to stick with the current-mode DAC for the A/D section of their sampling ADC574 replacement, and to add a true sample/hold amplifier to the front end of the converter. To accomplish this in a monolithic chip, they applied a BiCMOS process. Burr-Brown chose to use standard CMOS processing and a CDAC. The results of these two approaches are compared with each other and with the standard ADC574 and ADC774 in Table I.

Basically, the process chosen by Burr-Brown takes advantage of the power savings offered by CMOS, and turns out to allow new input ranges and the possibility of new data acquisition applications using a single +5V supply for the entire system. The only ADC574 compatibility concern is in systems where either an external 10V reference drives the A/D reference input, or where the internal 10V reference is used elsewhere. The Analog Devices AD1674 maintains the reference compatibility, but actually increases power consumption to achieve this (and to build a traditional sample/hold amplifier.)

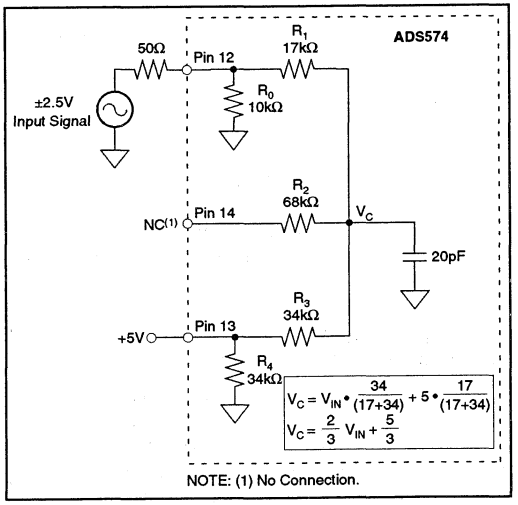


FIGURE 6. Connections for ±2.5V Input Range.

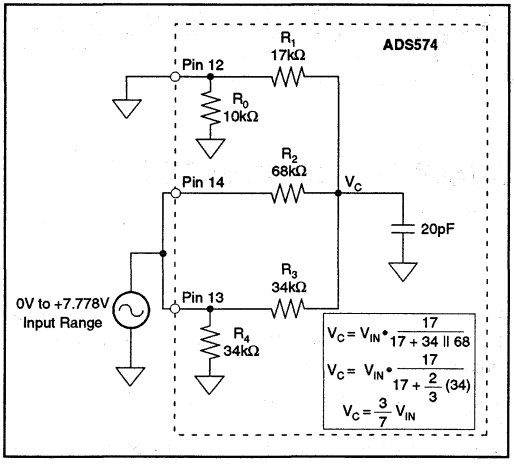


FIGURE 7. Connections for 0V to +7.778V Input Range.

	ADC574	ADS574	ADC774	ADS774	AD1674
Standard Input Ranges	0V to 10V, ±5V, 0V to 20V, ±10V	0V to 10V, ±5V, 0V to 20V, ±10V	0V to 10V, ±5V, 0V to 20V, ±10V	0V to 10V, ±5V, 0V to 20V, ±10V	0V to 10V, ±5V 0V to 20V, ±10V
New Input Ranges	None	0V to 7.778V, ±2.5V(1), 0V to 5V(1), 0V to 3.33V(1)	None	0V to 7.778V, ±2.5V(1), 0V to 5V(1) 0V to 3.33V(1)	None
Typ Input Impedance: 10V Ranges 20V Ranges	5kΩ 10kΩ	21kΩ 84kΩ	5kΩ 10kΩ	12kΩ 50kΩ	5kΩ 10kΩ
Min Input Impedance: 10V Ranges 20V Ranges	4.7kΩ 9.4kΩ	15kΩ 60kΩ	4.7kΩ 9.4kΩ	8.5kΩ 35kΩ	3kΩ 6kΩ
Max LSBs Integral Non-Linearity Error (J,K)	±1, ±1/2	±1, ±1/2	±1, ±1/2	±1, ±1/2	±1, ±1/2
No-Missing Codes Resolution	11-bits (Js)	12-bits	11-bits (Js)	12-bits	12-bits
Min Signal-to-(Noise + Distortion) Ratio with 10kHz Input (J/K Grades)	N/A	68/70dB	N/A	68/70 dB	69/70 dB
Max Conversion Time Over Temperature	25µs		8.5µs		
Max Acquisition and Conversion Time Over Temperature		25µs		8.5µs	10µs
Reference Output/Input	+10V	+2.5V	+10V	+2.5V	+10V
Power Supplies Required	±12 to 15V, +5V	+5V	±12 to 15V, +5V	+5V	±12 to 15V, +5V
Max Power Dissipation	450mW	100mW	450mW	120mW	575mW
Packages Available	0.6" DIPs and PLCC	0.6" and 0.3" DIPs, SOIC, Die	0.6" DIPs and PLCC	0.6" and 0.3" DIPs, SOIC, Die	0.6" DIPs Contact Factory for Surface Mount
Able to Emulate ADC574 Timing	Yes	Yes	Yes	Yes	No
Able to Fully Control S/H Timing	N/A	Yes	N/A	Yes	Yes
Able to Operate From Single +5V Supply	No	Yes	No	Yes	No
NOTE: (1) With slightly degraded integral linearity, as described in the text.					

TABLE I. Comparing Burr-Brown ADC574, ADC774, ADS574 and ADS774 with Analog Devices AD1674.

BURR-BROWN® APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

INTERLEAVING ANALOG-TO-DIGITAL CONVERTERS

by Jerry Horn, (602) 746-7413

It is tempting when pushing the limits of analog-to-digital conversion to consider interleaving two or more converters to increase the sample rate (Figure 1). However, such designs must take into consideration several possible sources of error.

The first consideration is the bandwidth of the converters. For example, if the bandwidth of the converters is just over half their sampling rate, then it would not do much good to interleave them. Fortunately, the bandwidth of most converters which currently "push the envelope" is often many times higher than their sample rate since these converters are often used in undersampling situations.

The next consideration is possible offset and gain errors between the converters. Figure 2 shows two interleaved converters digitizing a sine wave. Converter A has an offset problem and converter B a gain problem. The digitized codes represent not only the original sine wave but also an error signal. In the discrete digital domain, the error signal is seen to contain two sine frequencies—a frequency of half the sample rate (due to the offset error) and the other with a frequency of half the sample rate minus the frequency of the original input signal (due to the gain error).

The last consideration covered is the difference in INL (integral non-linearity) between the converters. INL represents the number of LSBs the output of a converter is from the expected output for a given input voltage. For example, if a converter would ideally put out a code of N for an input voltage M but actually puts out a code N+2, then the INL at that point is two.

It is not unusual for a high-speed converter to have an INL of one or two LSBs over a significant part of its input voltage range. For interleaving converters, the output codes could differ by as much as two times the maximum INL (say two to four codes) for the same input voltage. This could cause errors in the output codes which resemble the gain and offset problems discussed earlier, and may drastically reduce the number of effective bits of the digitizing system.

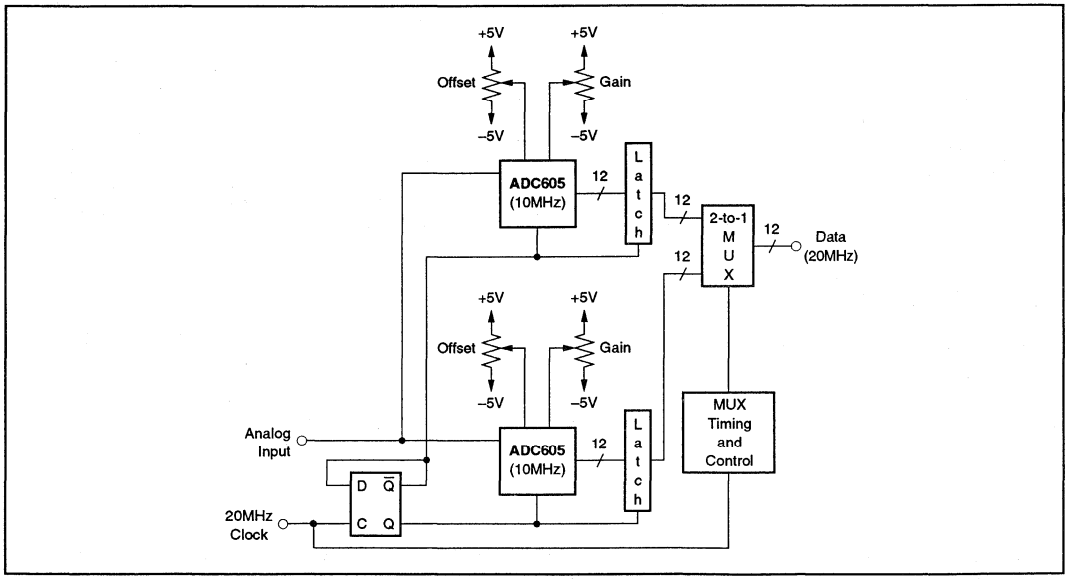


FIGURE 1. Interleaving Two ADS605s (10MHz, 12-Bit, ADCs) in Effort to Achieve a 20MHz, 12-bit Digitizing Rate.

With careful design, many of these problems can be reduced. Select ADCs with a wide enough bandwidth. Find ones that have offset and gain adjust circuitry built in or add this externally. ADCs which need external references may work well because the same reference can be provided to all the converters (but be careful of board layout). Unfortunately in this case, the trend has been to include internal references.

Reducing the errors even further is also possible, but quickly becomes increasingly complicated and costly. Correcting INL problems will almost certainly involve some form of post digital signal processing. Correcting in the time domain will involve lengthy calibration of the converters and storing correction tables. Correcting in the frequency domain will involve computationally intensive mathematical algorithms.

On the practical side, an interleaving digitizing system will suffer some performance penalty. The amount of degradation depends on how well the converters are matched and/or how much digital signal processing the designer is willing to do. Contact Burr-Brown Applications Engineering for more information on this subject.

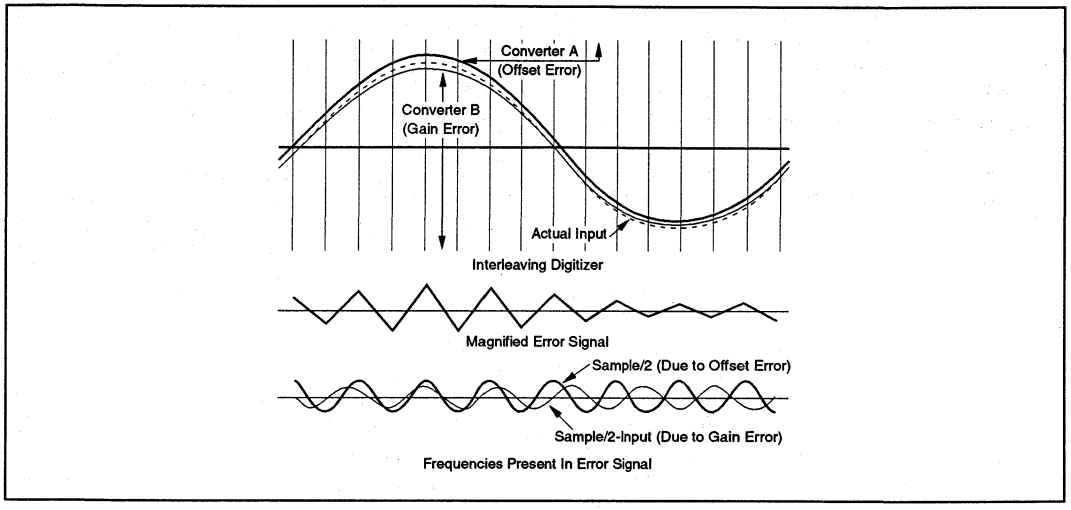


FIGURE 2. Gain and Offset Errors in the Converters Create False Signals in the Digitized Data.

BURR-BROWN®
APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

ANALOG-TO-DIGITAL CONVERTER GROUNDING PRACTICES EFFECT SYSTEM PERFORMANCE

Obtaining optimum performance from a high-resolution analog-to-digital converter (ADC) depends upon many factors. Power supply decoupling and good grounding practices are essential to maintaining accuracy in ADCs.

Poor grounding technique may manifest itself in many different ways such as excessive noise, or signal crosstalk in the system. A more difficult problem to track down is that of poor differential linearity error (DLE) in the converter. This is difficult because poor DLE may result from settling time problems inside the ADC, from the circuitry driving the ADC having too high an output impedance at the converter's operating frequency, from poor grounding techniques or other sources.

Figure 1 is a DLE plot of a ADCTH (12-bit, 8µs conversion time ADC) in a specific printed circuit board. This histogram plots deviation from ideal differential linearity against specific codes output from the converter. The circuit shown in Figure 1 has a DLE of about ±0.4LSB. This meets the specification of the ADC774, but is less than optimum.

The cause of the DLE performance is the grounding scheme used in this application. The part was "grounded" using recommendations made in most of our ADC data sheets: connect the analog and digital grounds together at the ADC.

What went wrong is that the analog and digital commons were connected together at the ADC, but that "ground" was then returned through a long trace on the PCB to the system ground. This means that the "ground" the ADC actually saw had a fair amount of resistance and inductance, as shown in Figure 3.

Returning the analog and digital common of the same ADC to a single ground plane underneath the converter (Figure 3) reduced this inductance and resistance considerably, and thus made the ADC "see" a much lower impedance; a more optimum ground. The results of this improved grounding technique are shown in Figure 2. The new board exhibits a DLE of only about ±0.1LSB, much closer to what the ADC774 typically does.

In general, using ground planes is the best way to set up grounding systems for high-resolution ADCs, so that the ADC ground return paths are as low an impedance as possible. Where the use of ground planes is not possible, using wide, short traces for ground returns is recommended to keep the ground impedance low. As this example shows, poor grounding can affect system performance in ways that don't readily indicate that a grounding problem may exist.

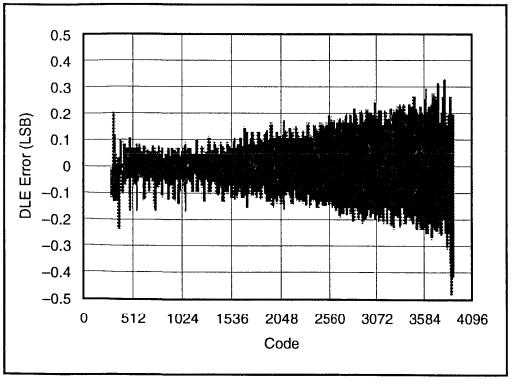


FIGURE 1. ADC774 Board DLE with Poor Ground.

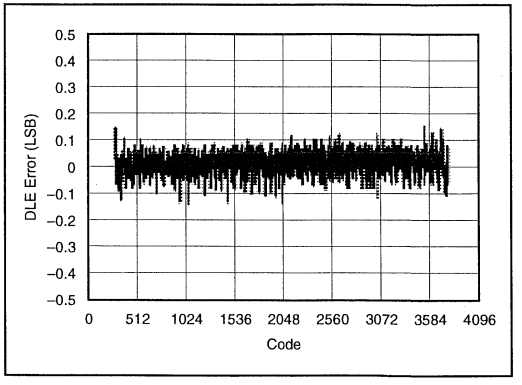


FIGURE 2. ADC774 Board DLE with Improved Ground.

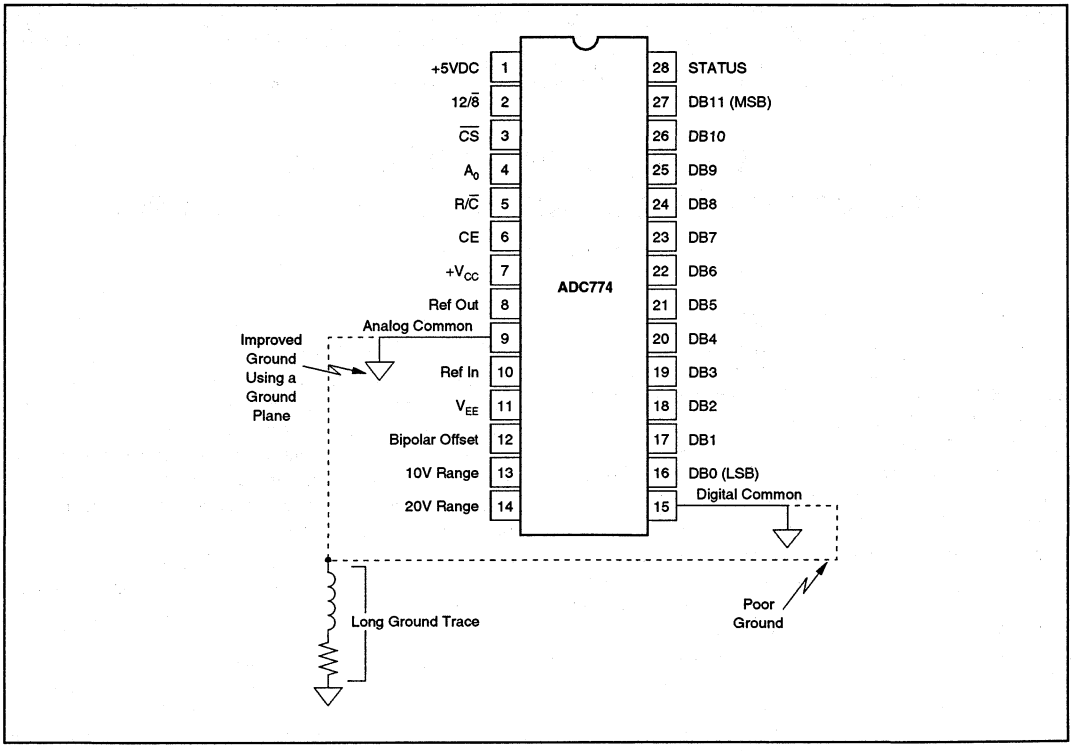


FIGURE 3. Ground Impedance is High Due to Long Circuit Trace. By Using Ground Plane, DLE is Improved.

BURR-BROWN®
APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

COMPLETE TEMPERATURE DATA ACQUISITION SYSTEM FROM A SINGLE +5V SUPPLY

by George Hill, (602) 746-7283

The CMOS ADS574 and ADS774 are drop-in replacements for industry standard ADC574 analog-to-digital converters, offering lower power and the capability to operate from a single +5V supply. The switched capacitor array architecture (CDAC), with the input resistor divider network to provide ADC574 input ranges, also allow the new parts to handle additional input ranges, including a 0V to 5V range. This can be used to build a complete temperature data acquisition system using a single +5V supply.

Figure 1 shows the input resistor divider network on the ADS574, and how it can be configured for a 0V to 5V input range. Pin 12 is normally the bipolar offset pin on standard ADC574s, and serves the same function for ±5V and ±10V input ranges on the ADS574. However, when connected as shown, pin 12 on the ADS574 can also be used as an analog input. In this mode, the ADS574 maintains its differential linearity of 12-bit "No-Missing-Codes", and integral linearity is typically better than 0.1%, or 10-bits. The slight change in linearity is due to internal circuitry designed to maximize compatibility of the ADS574 used in existing ADC574 sockets.

Figure 2 shows the circuit for a complete high accuracy temperature measurement system using the 0V to 5V input range on the ADS574. The RTD sensor shown has a resistance of 100Ω at 0°C, and is rated for use from –200°C to 660°C. Over this range, the resistance of the RTD will vary from about 18Ω to about 333Ω.

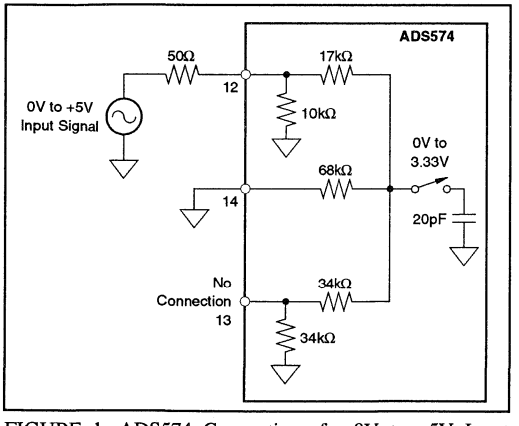


FIGURE 1. ADS574 Connections for 0V to +5V Input Range.

Amplifiers A_1 and A_2 (the two op amps inside a single OPA1013) are used to generate a stable 1mA current source to excite the RTD. The 2.5V reference output of the ADS574 is used to derive this current source, so that the entire system will be ratiometric. As the reference in the ADS574 changes over temperature or time, it will affect both the gain of the A/D and the current source.

RTDs in industrial process controls are often far removed from the electronics. One thousand feet of 22-gauge copper has 16Ω of resistance (shown as R_W in Figure 2), and this varies with temperature. The circuit around A_3 (half of a second OPA1013) uses a third wire from the remote RTD to remove most of the effect of the two R_W drops in series with the RTD. The 100kΩ resistors are much larger than R_W, minimizing inaccuracies due to currents flowing through them.

Amplifier A_4 is used in a gain of 12.207V/V, so that a 0.1Ω change in the value of the RTD (changing the positive input to A_4 by 100µV) corresponds to one LSB change in the output of the ADS574. 0V and 5V full scale inputs to the ADS574 would result from 0Ω and 409.6Ω RTD values (and hence 0mV and 409.6mV at A_4's input.) Choosing this range not only sets one LSB equal to a 0.1Ω change, but also keeps A_3 and A_4 from ever operating near their 0V and 5V rails. The RTD never gets below about 18Ω or above about 330Ω, which gives 18mV to 330mV at the input to A_4 (and somewhat more at the input to A_3, due to the two R_W drops.)

As used in Figure 2, the ADS574 will switch to the hold mode and start a conversion immediately when a convert command is received (a falling edge on pin 5.) Pin 28 will output a HIGH during conversion, and a falling edge output on pin 28 can be used to read the data from the conversion. Since digital processing will normally be done to linearize the output of the RTD for maximum accuracy, the same process can also be used to calibrate out gain and offset errors in the circuit, and any effects from the approximations used in the feedback around A_3.

This linearization will also restore the integral linearity of the ADS574 mentioned above, since the differential linearity remains at the 12-bit level.

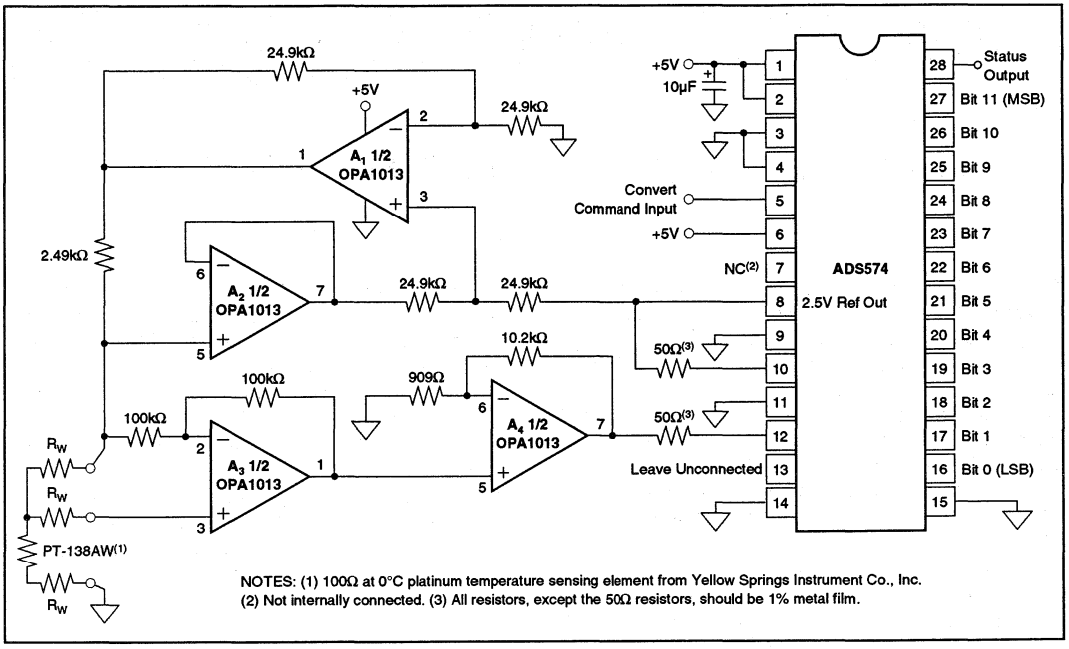


FIGURE 2. Complete Single-Supply Temperature Measurement System Using 3-Wire RTD Connection.

BURR-BROWN® APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

USING DSP101 WITH MULTIPLEXED ANALOG INPUTS

The DSP101 and DSP102 sampling analog-to-digital converters have all the interface logic to connect directly to popular digital signal processor ICs from ADI, AT&T, Motorola, and Texas Instruments. A unique "tag" input allows additional serial data to be appended to the serial data stream that is sent to the DSP processor. When the DSP101[1] is coupled with an analog multiplexer, this tag feature can be used to construct a low cost multiple input A/D that will send a channel identification number along with that channel's conversion results. The channel ID can then be used by the DSP processor to separate the different inputs.

The DSP101 uses an internal data pipeline architecture to synchronize the data from the Successive Approximation Register (SAR) analog-to-digital converter to the data clock of the DSP processor IC. The block diagram of the DSP101 (Figure 1) shows how data moves through the part and how the tag bits are appended. The serial data from the SAR is clocked into a shift register and held by a latch. On the next convert command, the data is then loaded into an output shift register and clocked out to the DSP processor IC, synchronous to the bit transfer clock. As the serial data is clocked out to the DSP processor IC, serial data inputted to TAG is clocked into the output shift register. Figure 2 shows how the serial tag information is appended after the 18th bit of data.

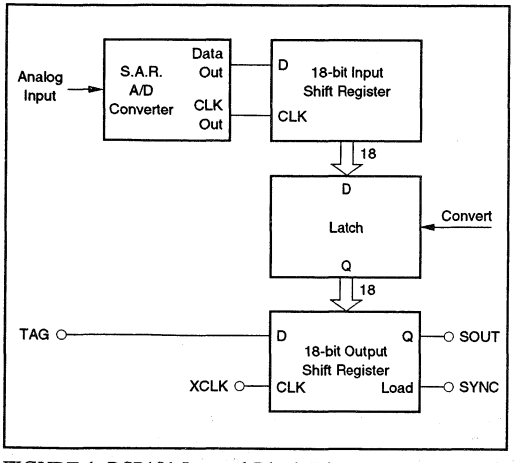


FIGURE 1. DSP101 Internal Block Diagram.

The schematic of Figure 3 shows a complete eight-channel analog input system. A 74HC163 counter is used to provide the scan sequence to a Burr-Brown MPC508A analog multiplexer. In order to allow the MPC508A enough time to switch to the next channel and settle before the DSP101 begins its conversion, a 74HC221 one shot is used to produce a 3ms delay for the DSP101 convert command input.

To avoid introducing distortion to the signal, the input to the DSP101 must be driven by a low impedance source. Due to the high output impedance of the MPC508A, an OPA627 in a unity gain configuration is used as a buffer for the DSP101 input.

Since the DSP101 has an internal data pipeline delay of one sample, a 74HC574 D-type latch is used to delay the tag bits by one sample also. This delay causes the channel identification tag to be appended directly to that channel's conversion results. Since the channel scanning shown in the schematic is sequential, this delay latch could be left out and the DSP processor software modified to recognize an N-1 channel ID. However, for systems using non-sequential scan lists, this delay latch would be essential to maintain the data and channel ID integrity.

The 74HC166 synchronous loading shift register is used so that the rising edge of the bit clock, in conjunction with the SYNC output of the DSP101, loads the tag data into the shift register in a predictable manner. The tag data is then clocked into the DSP101 by the bit clock, while conversion data is clocked out the other end of the shift register.

This circuit was constructed on Burr-Brown's DEM-DSP102/202 demonstration fixture. Software for recognizing channel tags and sorting the data was written for Burr-Brown's ZPB34 DSP board for the IBM PC/AT. This board is based on the AT&T WE® DSP32C 32-bit floating point digital signal processor.

Since the SYNC output of the DSP101 that is used to load the latches in this circuit is active low for AT&T DSP processors, the circuit must be modified for use with DSP processors from Texas Instruments, Motorola, and ADI. For these processors, tie the SSF pin of the DSP101 high, and use a 74HC04 hex inverter to invert the SYNC line input to the 74HC574 and 74HC166.

NOTE: (1) This discussion applies to both the DSP101 and the dual DSP102, but for simplicity we will talk only about the DSP101.

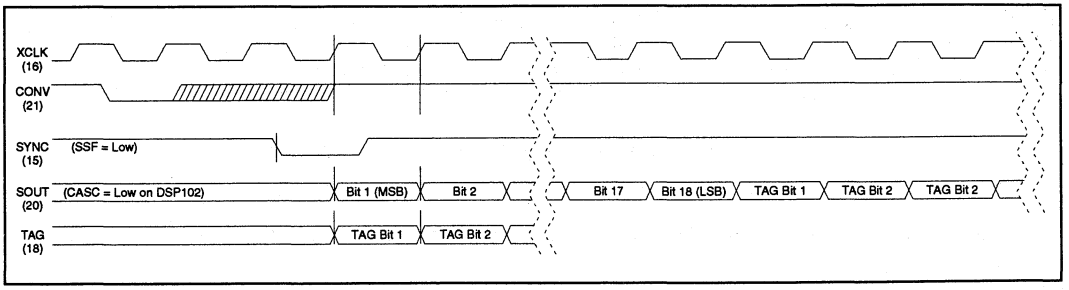


FIGURE 2. DSP101/102 SOUT Data Format with TAG Information. (See DSP101 data sheet for full timing information.)

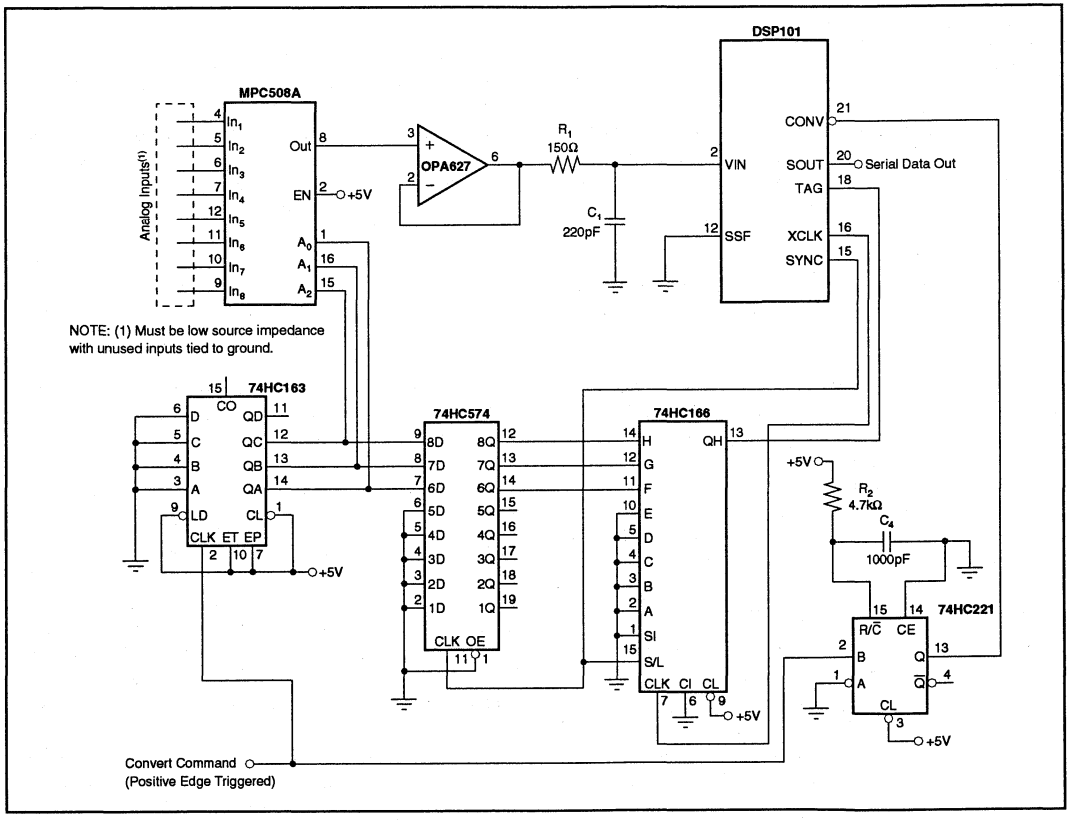


FIGURE 3. A Complete Eight-Channel Analog Input System Using the DSP101 and the MPC508A.

For Immediate Assistance, Contact Your Local Salesperson

BURR-BROWN® APPLICATION BULLETIN

Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

WHAT DESIGNERS SHOULD KNOW ABOUT DATA CONVERTER DRIFT

Understanding the Components of Worst-Case Degradation Can Help in Avoiding Overspecification

Exactly how inaccurate will a change in temperature make an analog-to-digital or digital-to-analog converter? As designers are well aware, a 12-bit device may provide a much lower accuracy at its operating-temperature extremes, perhaps only to 9 or even 8 bits. But for lack of more precise knowledge, many play it safe (and expensive) and overspecify.

Yet it is fairly simple to determine a converter's absolute worst-case degradation from its various drift specifications. Considering these specifications separately and examining their bases will help to unravel the labyrinth of converter drift and show how to go about calculating the actual worst-case drift error for most devices.

Accuracy drift for a D/A converter or a successive-approximation A/D converter has three primary components: its gain, offset, and nonlinearity temperature coefficients. Instead of calling out the gain and offset drifts separately, some manufacturers specify a full-scale drift, which takes both into account. Another important specification in many applications is differential nonlinearity, which reflects the equality (or rather, the inequality) of the analog steps between adjacent digital codes. But, since this parameter is really describing only the distribution of the linearity error, its temperature coefficient does not contribute to the converter's worst-case accuracy drift.

EXAMINING THE COMPONENTS OF DRIFT

The transfer function of a D/A converter will illustrate how the different kinds of drift degrade accuracy.

In a bipolar D/A converter, which produces both positive and negative analog voltages, offset drift changes all the output voltages by an equal amount, moving the entire transfer function up or down from the ideal in parallel to it (Figure 1a). The drift of the converter's voltage reference is the main cause of this error—which may also be called the minus-full-scale drift, since it occurs even when all the input bits are logic 0 or off. In a unipolar unit, the offset drift is usually much smaller, being due mostly to drift in the offset voltage of the output operational amplifier and secondarily to leakage in the current switches.

Unlike offset drift, gain drift rotates the transfer function (Figure 1b). In a bipolar unit it does so around minus full scale (all bits off), and in a unipolar unit it does so around zero (again all bits off). The gain drift affects each output voltage by the same percentage (not the same amount), tipping the transfer function at an angle to the ideal. In general, about 70% of this drift is caused by the drift of the converter's voltage reference.

Obviously, then, reference drift is a major contributor to total inaccuracy due to gain and offset drift. A positive temperature coefficient for the reference causes the transfer function to rotate about zero, as shown in Figure 1c for a bipolar converter. Since the gain and bipolar offset drifts due to the reference will always be opposite in direction, the worst-case accuracy drift may be less than half the sum of the individual drift specifications. In a unipolar converter, the gain and offset drifts may well add together, but the unipolar offset drift is usually insignificant compared to the magnitude of the gain drift, so it is not so important a factor.

Full-scale drift describes the change in the output voltage when all bits are on. For a unipolar converter, it is simply the sum of the offset and gain drifts. In contrast, for a bipolar converter, the full-scale drift is the sum of half the reference drift, the gain drift exclusive of the reference, and the offset drift exclusive of the reference.

POOR TRACKING CAUSES LINEARITY DRIFT

Finally, linearity drift reflects the shift in the analog output voltage from the straight line drawn between the output value when all the bits are off (minus full scale) and the output value when all the bits are on (plus full scale). This error is caused by the varying temperature coefficients of the ratio resistances of the converter's current-weighting (scaling) resistor, as well as the ratio drifts of the base-emitter voltages and betas of its transistor current switches.

Since the change in linearity with temperature depends on how closely various parameters track each other, and not on absolute parameters values, it is fairly easy to control with present-day hybrid and monolithic technologies. As a result, linearity drift is usually much smaller than either the gain or offset drift. Moreover, it is generally guaranteed to be within some maximum limit over the converter's full operating temperature range.

Another specification that is important in some applications is bipolar zero drift, which reflects the change in the output voltage of a bipolar converter at midscale, when only the most significant bit is on and all other bits are off. This drift error at zero is not affected by reference drift at all, but is caused mainly by poor tracking in the converter's scaling resistors and current switches. Therefore, it appears as a

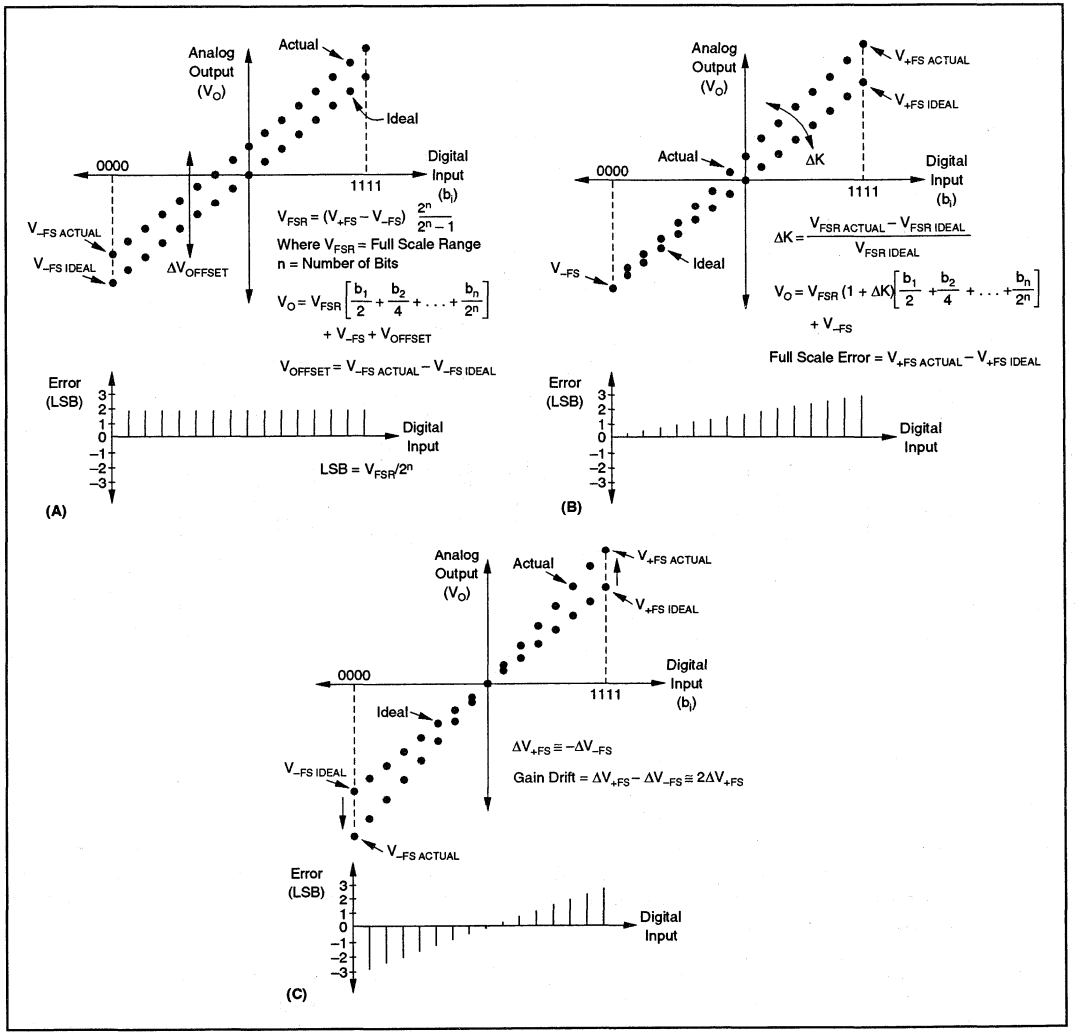


FIGURE 1. Effects of Drift. For a bipolar D/A converter, offset drift (a) moves the unit's transfer function up or down, whereas gain drift (b) rotates is about digital zero. Both of these errors are chiefly due to reference drift (c), which causes a rotation about analog zero.

random variation about zero, and it has a worst-case magnitude equal to the offset drift exclusive of the reference plus half the gain drift exclusive of the reference.

To understand more fully how these drift errors are generated, consider the simplified schematic (Figure 2) of a typical 12-bit bipolar D/A converter. Circuit operation is fairly simple. The reference current flows through reference transistor Q_C, producing a voltage drop across resistor R_C. Since the base of Q_C is connected to the bases of all the other transistor current switches, the same potential is also generated across resistors R_1 through R_{12}. The multiple emitters of the transistors cause current density to be the same for each of these binarily weighted current sources, thereby providing good matching and tracking of the transistors' V_{BE} and β.

TRACKING ERRORS TEND TO CANCEL

Now suppose that, because of temperature or aging, the value of every resistor on network RN_1 increases by 1%. Since the reference current remains constant, the voltage across these resistors also increases by 1%, so the output current and the output voltage are unchanged. If, instead, the value of all the resistors on network RN_2 increase by 1%, the

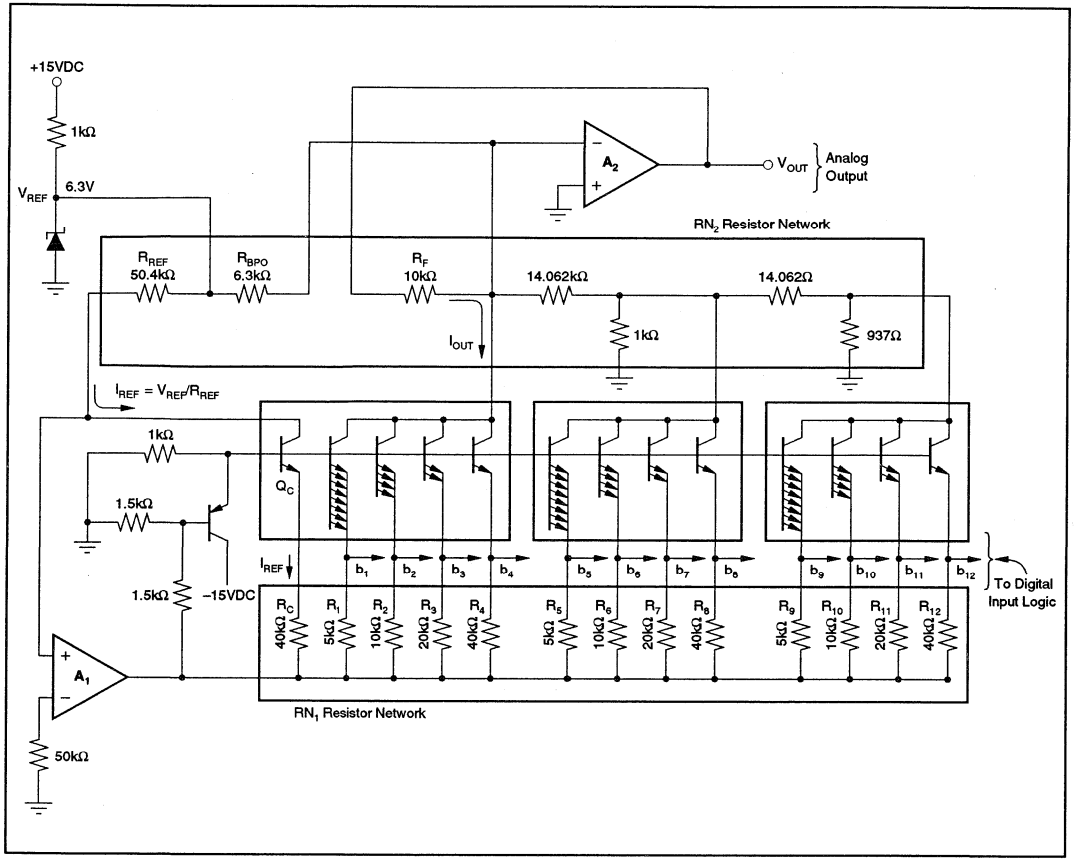


FIGURE 2. Typical D/A Circuit. In general, the circuit design for a D/A converter largely compensates for tracking errors in the resistor networks and transistor current switches. By far the dominant error source is the drift of the zener diode that makes up the reference.

reference current decreases by 1%, reducing the voltage across R_C by 1% and causing the output current to drop by 1%. However, since the value of the feedback resistor, R_F is now 1% higher, the output voltage, which is equal to $I_{OUT}R_F$, does not change.

The converter compensates for variations in the transistor V_{BE} and β in the same manner. Although the individual resistors on RN_1 and RN_2 may have temperature coefficients as high as ±50 parts per million per degree Celsius, the tracking of these resistors, and therefore their contribution to drift in linearity and gains, is typically as little as 1 to 2 ppm/°C. In fact, the only error sources for which the circuit does not compensate are the drifts in offset voltage and offset current of amplifiers, A_1 and A_2, as well as the drift of the zener reference diode. By far, the dominant error source is the drift of this zener, while the offsets of A_1 contribute to the gain drift exclusive of the reference, and the offsets of A_2 contribute to offset drift exclusive of the reference.

THE EFFECT OF REFERENCE DRIFT

To evaluate the effect of variations in the reference voltage on the overall accuracy of the converter requires determining the variation in output voltage for a change in ambient temperature. A good first-order approximation is to assume that all other drift errors — those due to tracking errors and random variations — are zero.

Writing the node equation for the summing junction at the inverting input of amplifier A_2 yields:

$$\frac{V_{OUT}}{R_F} + \frac{V_{REF}}{R_{BPO}} - \frac{V_{REF}}{R_{REF}} K\left[\frac{b_1}{2} + \frac{b_2}{4} + \ldots + \frac{b_n}{2^n}\right] = 0$$

where K is a gain constant, and b_1 through b_n represent the digital bits, which are either 1 or 0, depending on whether a bit is on or off. This equation may be used to determine the output voltage for any digital input.

At minus full scale, with $B_1 = b_2 ... = b_n = 0$, the output voltage becomes:

$$V_{OUT} = V_{-FS} = -\left[\frac{R_F}{R_{BPO}}\right]V_{REF}$$

At bipolar zero ($b_1 = 1$, $b_2 = b_3 = ... = b_n = 0$), the output voltage for an ideal converter is equal to zero:

$$V_{OUT} = V_{BPZ} = 0 = \left[\frac{R_F}{2R_{REF}}K - \frac{R_F}{R_{BPO}}\right]V_{REF}$$

At plus full scale, with $b_1 = b_2 = ... = b_n = 1$, the output voltage becomes:

$$V_{OUT} = V_{+FS} = \left[\frac{R_F}{R_{REF}}K - \frac{R_F}{R_{BPO}}\right]V_{REF}$$

Solving the equation for V_{BPZ} for gain constant K yields:

$$K = \frac{R_F}{R_{BPO}}\frac{2R_{REF}}{R_F} = \frac{2R_{REF}}{R_{BPO}}$$

Substituting this expression for K in the appropriate equations, the variation in output voltage for a change in reference caused by temperature may be computed. At minus full scale, this drift is:

$$\frac{\Delta V_{-FS}}{\Delta T} = -\frac{R_F}{R_{BPO}}\frac{\Delta V_{REF}}{\Delta T}$$

where ΔT is the change in ambient temperature. As mentioned previously, drift error at midscale is caused by tracking errors, not by variations in the reference, so:

$$\frac{\Delta V_{BPZ}}{\Delta T} = 0$$

At plus full scale, the change in the output becomes:

$$\frac{\Delta V_{+FS}}{\Delta T} = \frac{R_F}{R_{BPO}}\quad\frac{\Delta V_{REF}}{\Delta T}$$

Therefore, the drift in the output voltage due to reference variations at minus full scale (or the bipolar offset drift) will be equal in magnitude but opposite in direction to that at plus full scale. Each of these drift errors amounts to half the reference drift. The gain drift due to reference variations may be written as:

$$\left(\Delta V_{+FS} - \Delta V_{-FS}\right) / \Delta T$$

which is equal to the reference drift. It should be noted that the gain and reference drifts are specified in ppm/°C, while the full-scale and offset drifts are in ppm of full-scale range (FSR) per °C.

COMPUTING THE WORST-CASE ERROR

These results may now be used to find the worst-case total accuracy drift error for the typical converter of Figure 2. Suppose the maximum temperature coefficient of the device's internal reference is ±20ppm/°C, resulting in a gain drift of ±20ppm/°C, a plus-full-scale drift of ±10ppm of FSR/°C, and a bipolar offset drift of ±10ppm of FSR/°C. The maximum gain drift exclusive of the reference is ±10ppm/°C, and the offset drift exclusive of the reference is ±5ppm of FSR/°C.

The worst-case error occurs at plus full scale. To compute it, the errors due to the reference as well as those exclusive of the reference that are due to random variations must be taken into account. Therefore, the only contributors to the worst-case full-scale accuracy drift are the plus-full-scale drift due to the reference, and the random errors of the offset drift and the gain drift exclusive of the reference. Summing these together yields a worst-case full-scale accuracy drift of ±25ppm of FSR/°C or ± 0.0025% of FSR/°C.

The converter is a 12-bit device having a linearity error of ±1/2 least significant bit, or ±0.01%. Also, for its operating temperature range of 0°C to 70°C, the maximum excursion from room temperature (25°C) will be 45°C. Assuming that gain and offset errors are adjusted to zero at room temperature, the total accuracy error may be computed as the sum of the linearity error and the full-scale accuracy error:

worst-case total accuracy error = (linearity error)
+ (full-scale accuracy error)
= (±0.01%) + (±0.0025%/°C) (45°C)
= ±0.12%

which is about 9-bit accuracy. The accuracy for many 12-bit D/A converters will typically be twice as good as this with most devices providing 10-bit accuracy.

All of the drift relationships and causes examined in this article also apply to a successive-approximation A/D converter, which uses a D/A converter as one if its circuit blocks, as shown in Figure 3. In the equations, simply substitute V_{IN} for V_{OUT} and R_{IN} for R_F. Also, in the A/D converter, comparator drift, rather than op amp drift, contributes to the device's unipolar offset drift.

Reprinted from *Electronics*, November 10, 1977; Copyright ©McGraw-Hill, Inc., 1977

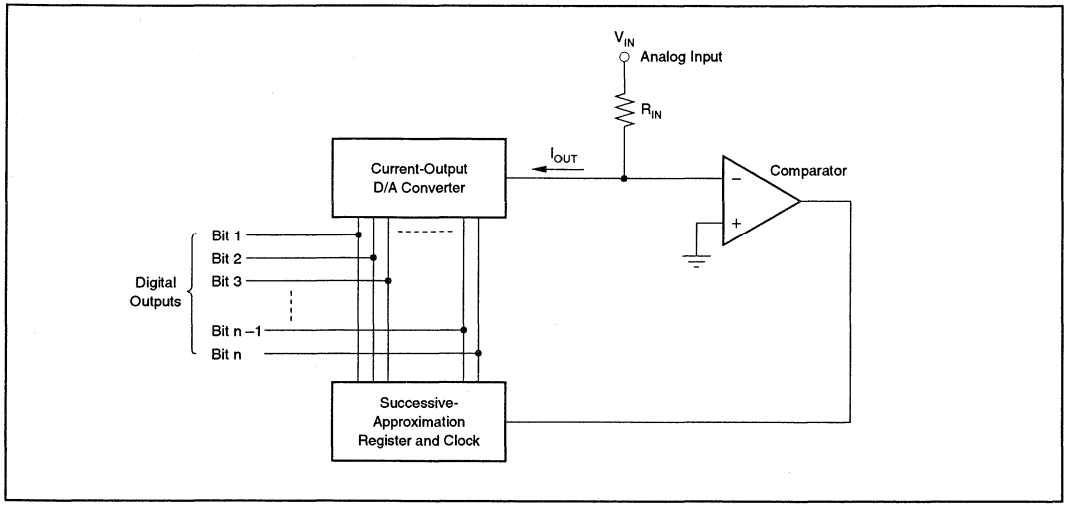


FIGURE 3. A/D Converter. All of the relationships that apply to the drift errors in a D/A converter also hold for a successive approximation A/D converter, since this component includes a current-output D/A converter as one of its circuit blocks, as shown here.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

BURR-BROWN® APPLICATION BULLETIN

Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

SUPERPOSITION: THE HIDDEN DAC LINEARITY ERROR

As More DACs Become Available With Resolutions of 12 Bits and Greater, Users Should Know the Causes and Effects of Superposition Error on Relative and Absolute Accuracy and What to Do to Minimize It.

A digital-to-analog converter (DAC) translates digital signals to analog signals. For example, a 12-bit DAC takes a 12-bit binary number, called an input code, and converts it into one of 4,096 analog output voltages or currents. When the contribution to the output voltage or current of each individual bit is independent of any other, it means that the device exhibits no superposition error or that "superposition holds." For a DAC with little or no superposition error, the linearity error for any given code will relate to the linearity error at some different code. This allows you to determine the worst case linearity error, and the digital code where that error occurs, with a very simple test.[1]

However, if the DAC under test has excessive superposition error, this simple test will give erroneous results; therefore, you must test all digital codes to determine the worst case error and code. Superposition error, or bit interaction, often is significant in converters with a resolution of 12 to 16 bits. If the error becomes large enough, a DAC may fail to meet a 1/2LSB linearity error or relative accuracy specification even with each individual bit adjusted perfectly. This specification becomes important in many applications such as automatic test equipment or precision voltage standards where the absolute value of the output voltage must remain within specified limits after calibration of offset and gain errors.

For a DAC with low superposition, the following equation determines the output voltage, if we assume that the offset and gain errors have been removed:

$$V_O = V_{FS}\begin{bmatrix} b_1(1/2+\varepsilon_1)+b_2(1/4+\varepsilon_2)+\ldots \\ +b_n(1/2^n+\varepsilon_n)\end{bmatrix} \quad (1)$$

where $\varepsilon i \times V_{FS}$ equals the linearity error associated with the i^{th} bit and b_i, equals the value (0 or 1) of the i^{th} bit of the DAC input code. Since the analog output error with all input code bits off (000...000) and all input bits on (111...111) has been adjusted to 0, the summation of all the bit errors,

$$(\varepsilon_1+\varepsilon_2+\varepsilon_3\ldots\varepsilon_n)\text{or}\left(\sum_{i=1}^{n}\varepsilon_i\right) \quad (2)$$

becomes zero. This means that the errors are symmetrical or, in other words, for every possible input code there exists an equal and opposite error associated with the one's complement of that code. The linearity error (sometimes called relative accuracy, integral linearity, nonlinearity or endpoint linearity) is defined as the maximum error magnitude that occurs.

Now consider the relationship between the individual bit errors (ε_i) and the linearity error. There exists some digital input code (b_1, b_2 . . . b_n) that yields the maximum linearity error (E_{MAX}) and the one's complement of this code (b_1, b_2...b_n), that must yield an error of the same magnitude but in the opposite direction ($-E_{MAX}$). The relative magnitude and polarities of the errors determine which actual input code has the most linearity error. For the error to be maximum, all of the error terms must be additive and the following proves true:

$$\begin{aligned} |E_{MAX}|+|-E_{MAX}| &= |b_1\varepsilon_1+b_2\varepsilon_2+\ldots \\ &\quad +b_n\varepsilon_n|+|\overline{b}_1\varepsilon_1+\overline{b}_2\varepsilon_2+\ldots+\overline{b}_n\varepsilon_n| \\ 2|E_{MAX}| &= (b_1+\overline{b}_1)|\varepsilon_1|+(b_2+\overline{b}_2)|\varepsilon_2|+\ldots \\ &\quad +(b_n+\overline{b}_n)|\varepsilon_n| \end{aligned} \quad (3)$$

but $b_i + b_i = 1$, making the maximum linearity error:

$$|E_{MAX}| = 1/2\left[|\varepsilon_1|+|\varepsilon_2|+\ldots+|\varepsilon_n|\right] \quad (4)$$

This result proves interesting because it relates the maximum linearity error to the individual bit errors; therefore, you can evaluate a DAC by simply measuring the output error associated with n digital input codes instead of all of the 2^n possible combinations.[2,3]

Stated another way, the sum of the positive bit errors should equal in magnitude the sum of the negative bit errors when the gain and offset errors have been removed. Any difference in these magnitudes indicates the presence of a superposition error. If this difference proves greater than approximately 1/10 of an LSB (JDEC standard for superposition error), further testing may become necessary to determine the accuracy of the DAC. However, a superposition error of more than 1/10LSB does not by itself imply that a DAC cannot meet a linearity specification of, say, ±1/2LSB; it simply means that you must conduct a more elaborate test to determine the worst case linearity error and digital input code where that error occurs.

A 3-BIT DAC

An example illustrating the relationship between linearity error and the individual bit errors for a 3-bit DAC appears in Figure 1a. Any deviation in the DAC output from the straight line drawn between all bits off and all bits on indicates a linearity error. With the superposition error less than 1/10LSB, the error pattern will appear as symmetrical around midscale as indicated.

Figure 1b shows a transfer characteristic for a 3-bit DAC which exhibits superposition error. Note that, in this example, the symmetrical error pattern around midscale no longer exists. You must consider the difference between the electrical sum and the algebraic sum of the bit errors when determining whether to use a more comprehensive test.

The data in Table I came from a 12-bit hybrid DAC. Note that, for this test, the full scale voltage was increased to 10.2375V, making the ideal bit weights, starting at the LSB, equal to 2.5mV, 5.0mV, 10.0mV... 2.560V, and finally 5.12V for the MSB. You can memorize these numbers easily and calculate the error voltages quickly by inspection. The difference between the algebraic sum of the positive bit errors (320µV) and negative bit errors (–310µV) equals only 10µV, which indicates a low superposition error. Thus, the maximum linearity error becomes 1/2 x (320 + 310) = 315µV.

The data in Table II came from a monolithic bipolar 12-bit DAC. Note that the difference here between the positive bit errors (+550µV) and the negative bit error (–1,650µV) equals –1.1mV or almost 1/2LSB. In this situation, superposition does not hold and you cannot say anything definite about linearity with the data available.

TESTING ALL INPUT CODES

When the short-cut method of measuring linearity error does not prove sufficient, you can develop a high speed measurement circuit capable of testing all 2^n code combinations. A simple schematic of this type of tester appears in Figure 2. The binary counter has n + 1 stages to provide a binary count from 0 to $2^n - 1$ and to reset the counters at the end of the count. The reference DAC and the x 10 error amplifier must have combined settling times to ±1/10LSB of less than 10µs since the system clock must operate at 20kHz to have a flicker-free display. For a 12-bit converter, a complete cycle takes 50µs x 4,096 counts or approximately 100ms. The output of the n^{th} counter stage also displays on the scope to indicate the midscale transition point, and offset and gain adjustment potentiometers are provided to zero the end points of the error display.

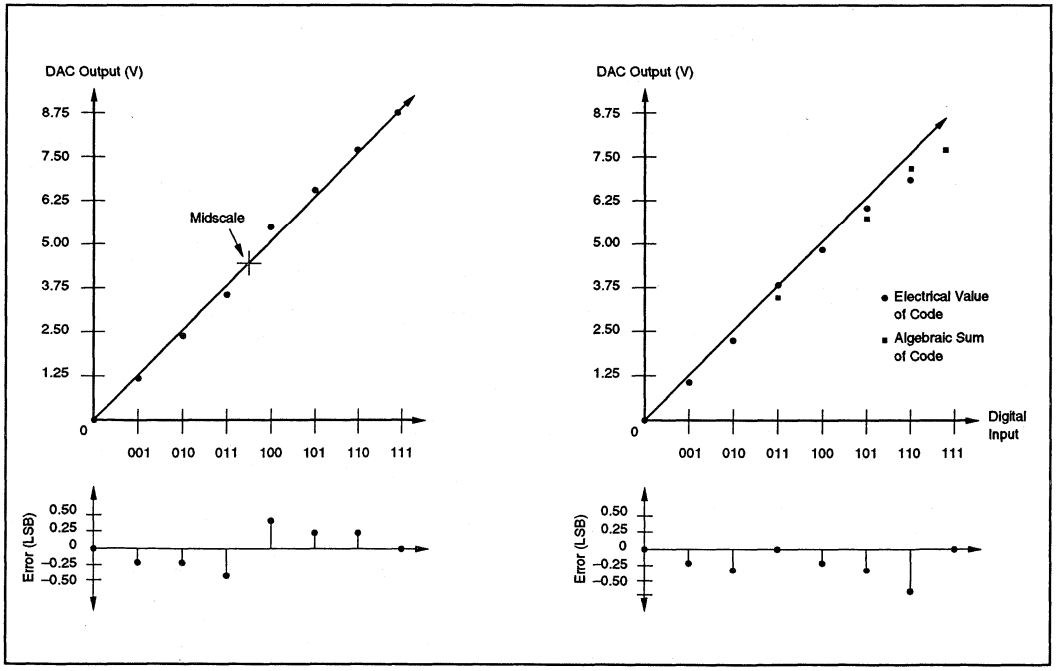


FIGURE 1. Both of These 3-Bit DAC Transfer Functions Exhibit Errors. Linearity error (a) exists for input codes 001, 010, 011, 100, 101, and 110; note the symmetry of the errors about midscale. Superposition errors (b) lack symmetry about midscale.

INPUT CODE	IDEAL OUTPUT (V)	ACTUAL OUTPUT(V)	ERROR(μV)
All Bits "On"	+10.23750	+10.23750	0
All Bits "Off"	0	0	0
Bit 1 (MSB)	5.12000	5.11995	–50
Bit 2	2.56000	2.55982	–180
Bit 3	1.28000	1.27994	–60
Bit 4	0.64000	0.63998	–20
Bit 5	0.32000	0.32004	+40
Bit 6	0.16000	0.16004	+40
Bit 7	0.08000	0.08004	+40
Bit 8	0.04000	0.04005	+50
Bit 9	0.02000	0.02010	+100
Bit 10	0.01000	0.01002	+20
Bit 11	0.00500	0.00502	+20
Bit 12 (LSB)	0.00250	0.00251	+10
Positive Sum			+320
Negative Sum			–310
Difference			+10

TABLE I. In This Data from a 12-Bit Hybrid DAC, the Full-Scale Voltage Was Increased to 10.2375V, Making the Ideal Bit Weights, Starting at the LSB, Equal to 2.5mV, 5.0mV, 10.0mV...2.560V and Finally 5.12V for the MSB. You can easily memorize these numbers and quickly calculate the error voltages by inspection.

INPUT CODE	IDEAL OUTPUT (V)	ACTUAL OUTPUT(V)	ERROR(μV)
All Bits "On"	+10.23750	+10.23750	0
All Bits "Off"	0	0	0
Bit 1 (MSB)	5.12000	5.11927	–730
Bit 2	2.56000	2.55928	–720
Bit 3	1.28000	1.27996	–40
Bit 4	0.64000	0.64013	+130
Bit 5	0.32000	0.32013	+130
Bit 6	0.16000	0.16003	+30
Bit 7	0.08000	0.07987	–130
Bit 8	0.04000	0.03997	–30
Bit 9	0.02000	0.02000	0
Bit 10	0.01000	0.01008	+80
Bit 11	0.00500	0.00512	+120
Bit 12 (LSB)	0.00250	0.00256	+60
Positive Sum			+550
Negative Sum			–1650
Difference			–1100

TABLE II. Note That the Difference Between the Positive Bit Errors (+550μV) and the Negative Bit Errors (–1,650μV) in This Data from a Monolithic Bipolar DAC, Equals –1.1mV or Almost 1/2LSB. In this situation, superposition does not hold and you cannot say anything definite about linearity with the amount of data available.

This tester works well for 8-, 9-, and 10-bit converters. For a 12-bit DAC, the 4,096 segments displayed on the CRT are spaced so close together that the switching transients create a wide band of noise making it difficult to tell if the converter meets its specification, especially with a linearity error near the ±1/2LSB limit. One way around this problem, if you assume that the errors contributed by the last four bits of the DAC are small, entails inhibiting these bits with the AND gates shown in Figure 2; this reduces the binary count to 256 and also gives each count 16 times longer for the glitches to settle out. You can make other improvements to this tester such as automatic offset and gain error nulling, a sample/hold deglitcher to remove the glitches at the error output and a go/no go window comparator to test the linearity error at each binary count.

The test circuit shown in Figure 2 and two different 12-bit DACs produced the oscilloscopic photographs in Figure 3. The offset and gain errors have been nulled at the left and right portions of the photographs, respectively; and the linearity error appears as the deviation from the horizontal center line of the scope, with the vertical sensitivity 1/2LSB per division. The digital input to the MSB indicates the mid-range and full-scale binary counts.

The DAC errors displayed in Figure 3a appear symmetrically about the center of the scope, indicating very little superposition error; while those in Figure 3b are almost all positive which indicates a moderate amount of superposition error. Figure 3b shows why some manufacturers specify linearity error as the maximum deviation from a best fit straight line rather than straight line through the end points. You can see, in this example, that a linearity error specification of ±1/2LSB proves easier to meet when using the best fit straight-line method. In a DAC with symmetrical error patterns, as shown in Figure 3a, a straight line through the end points becomes the same as a best fit straight line.

SOURCES OF SUPERPOSITION ERROR

Generally, superposition error in monolithic and hybrid converters results from the feedback resistor, R_f, changing in value as the output voltage varies from 0V to +10V. This apparent nonlinearity comes from the variable power dissipation that occurs in this resistor which can produce a temperature rise (self-heating) of as much as 1°C to 2°C in some DACs. This in turn changes the absolute value of the feedback resistor since it will have a temperature coefficient (TC) of between 50ppm/°C and 300ppm/°C for a thin-film material and over 1,000 ppm/°C for a monolithic diffused resistor. This problem generally does not occur in discrete data converters because the physical size of the feedback resistor is so large that the temperature rise, and therefore the resistance variation, remain extremely small. In a monolithic converter, however, with real estate at a premium, the mass of the feedback resistor is often so small the large temperature rise will occur for even small changes in power dissipation due to self-heating

To determine if the feedback resistor is at fault, substitute a low TC external resistor for the internal feedback resistor of the DAC and see if the nonlinearity disappears. The oscilloscope photograph in Figure 4 shows the results of using the test circuit shown in Figure 2, the same DAC whose transfer function appears in Figure 3b, with the internal feedback resistor being replaced by a low TC external resistor. Note that the DAC error is now almost evenly distributed about the center of the oscilloscope which indicates that the major cause of the superposition error has been removed. You cannot use an external feedback resistor, of course, in most

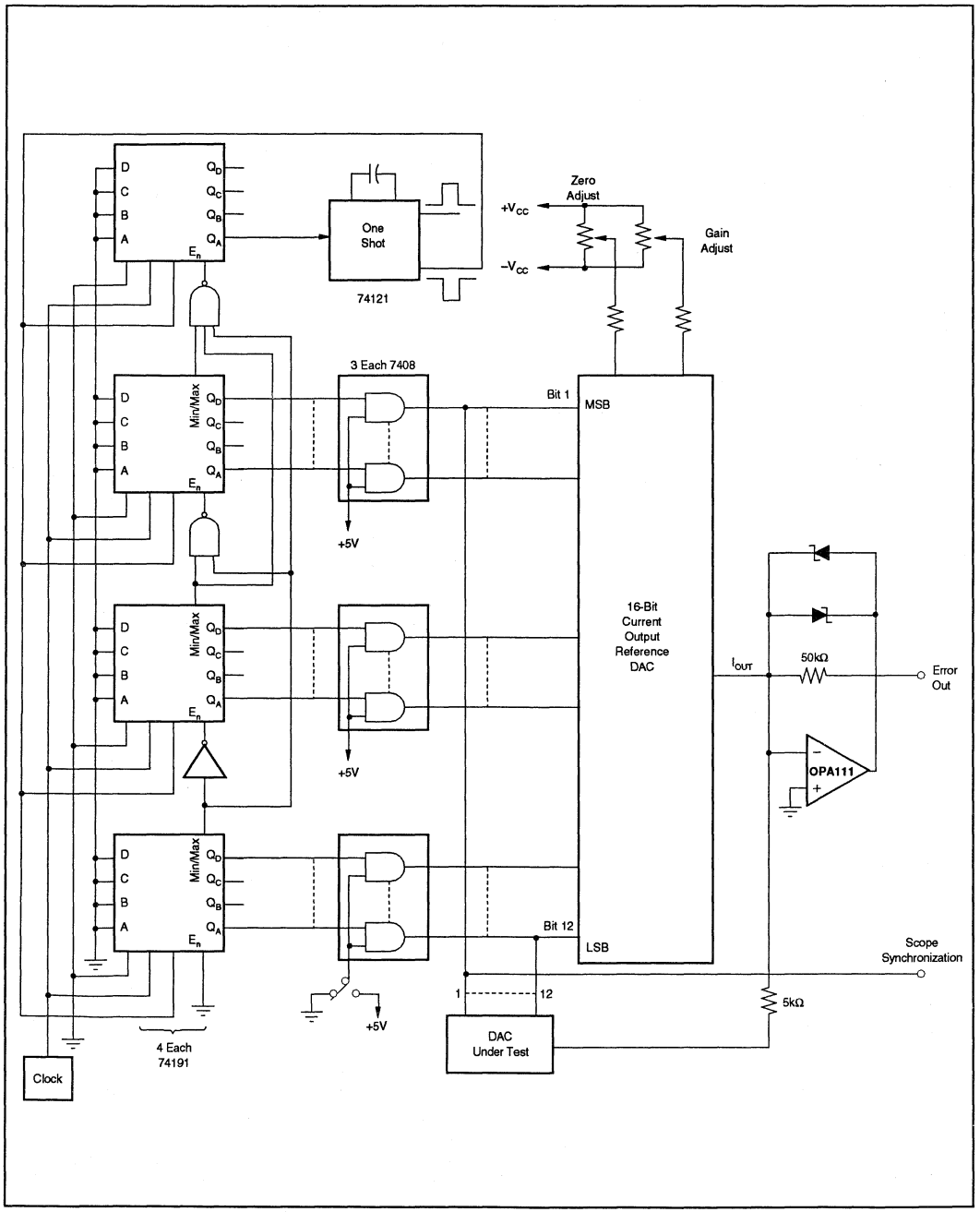


FIGURE 2. This Tester Works Well For 8-, 9-, and 10-Bit Converters. For a 12-bit DAC, the 4096 segments displayed on the CRT are spaced so close together that the switching transients create a wide band of noise making it difficult to tell if the converter meets its specification, especially with linearity error near the ±1/2LSB limit. One way around this problem, if you assume that the errors contributed by the last four bits of the DAC are small, entails inhibiting these bits with the AND gates shown.

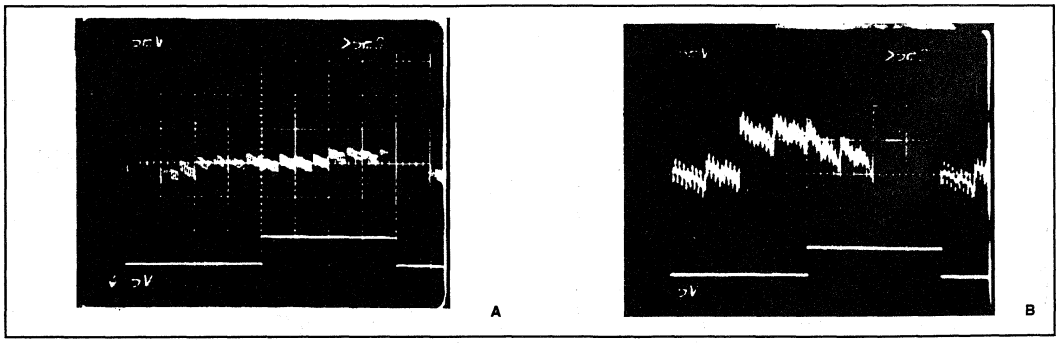


FIGURE 3. In These Scope Waveform Photographs Showing the Output of the Test Circuit in Figure 2, the Top Traces Indicate the Linearity Error, and the Bottom Traces Reflect the Status of the MSB of the Input Code. The hybrid DAC (a) exhibits little superposition error, while the asymmetry of the linearity error (b) about midscale shows superposition error for the monolithic bipolar DAC. The MSB transition marks the horizontal center.

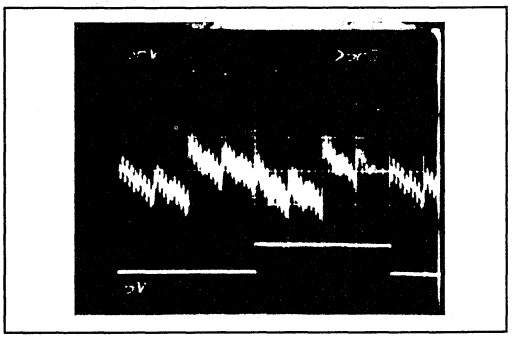


FIGURE 4. An External Feedback Resistor Can Decrease Superposition Error for the Monolithic Bipolar DAC Shown in Figure 3b.

practical applications because it will cause excessive gain drift since it will not track the internal diffused or thin-film reference resistor with variations in time and temperature.

Superposition error or bit interaction can occur in other ways—by temperature gradients on a monolithic chip which cause the magnitude of a bit output to be a function of the state of the other bit switches, or by feedback resistors which have an appreciable voltage coefficient of resistance (VCR), such as diffused resistors might. Again, the presence of superposition error does not mean a DAC will not meet its linearity specification, but you will need more extensive testing to verify if it does.

Superposition error, however, is by no means the only source of linearity error. Pay attention to your wiring whenever you use or test a DAC. When critical portions of a circuit share the same metallization path (e.g., a metallization path on a monolithic chip or in a wirebond; the contact resistance of a socket; or the wiring resistance of a test circuit), varying voltage drops caused by changing current levels can cause serious errors which could "drown out" any existing superposition error.

You can minimize the effect of wiring resistance (R_W) external to the DAC by paying careful attention to the grounding and connection scheme employed. Figure 5a shows a correct connection configuration that you can use with most commercially available DACs to yield maximum accuracy. You can reduce or eliminate the effects of various wiring and contact resistances, R_1, R_2, R_3 and R_4, as follows:

- R_1 appears in series with the feedback resistance and therefore introduces only a gain error that can be nulled during calibration.
- R_2 appears inside the output amplifier feedback loop and the loop gain will reduce its effect.
- R_3 appears in series with the load resistor and will cause an error in the voltage across R_L. One-half LSB error would result at full load for R_3 = 0.02Ω for a 16-bit DAC. Therefore, if possible, you should sense the output voltage in such a way as to include R_3. Figure 5b illustrates the optimum connection made possible by the ground sense pin available on some higher accuracy DACs. In the configuration shown, $R'_F = R_F$ and $R_B = R_{DAC}$. This causes rejection of any signal developed across R_3 as a common mode input, and R_3 will not affect the voltage across R_L. This configuration will also reject noise present on the system common.
- R_4 remains negligible in both circuits with ground connections made as shown.

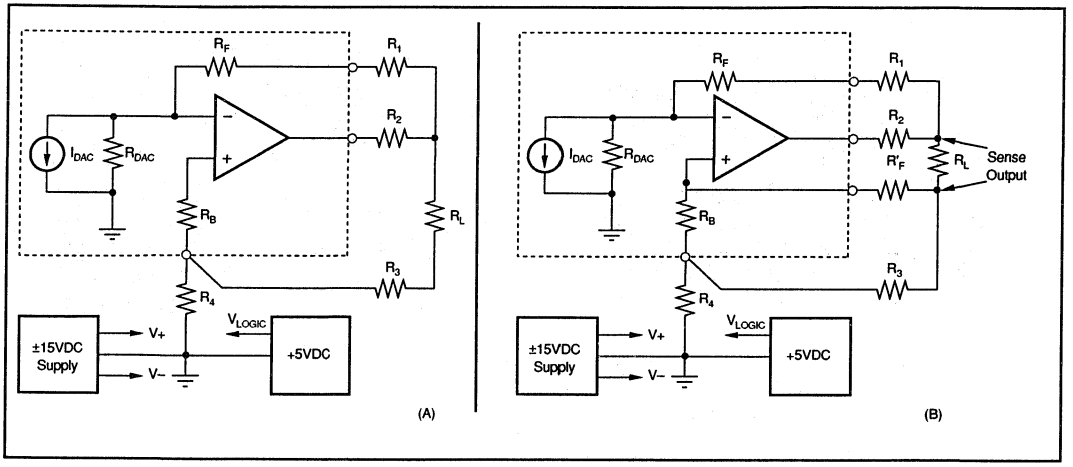


FIGURE 5. These Connection Diagrams Show How to Reduce the Effects of Wiring and Socket Resistance for a Typical DAC (a) and a High Accuracy DAC (b). Resistors R_1, R_2, R_3 and R_4 represent wiring and contact resistance.

REFERENCES

1. J. Naylor, "Testing Digital/Analog and Analog/Digital Converters," *IEEE Trans. on Circuits and Systems*, Vol. CAS-25, No. 7, July 1978.
2. T. Cate, "Tom Cate of Burr Brown Speaks Out on D/A Converter Specs," *EDN/EEE*, pp. 34-40, June 1, 1971.
3. P. Prazak, "Progammable Handheld Calculator Computes Digital-to-Analog Converter Errors," pp.122-127, *Computer Design*, June 1978.

BURR-BROWN® APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

PRINCIPLES OF DATA ACQUISITION AND CONVERSION

Data acquisition and conversion systems are used to acquire analog signals from one or more sources and convert these signals into digital form for analysis or transmission by end devices such as digital computers, recorders, or communications networks. The analog signal inputs to data acquisition systems are most often generated from sensors and transducers which convert real-world parameters such as pressure, temperature, stress or strain, flow, etc., into equivalent electrical signals. The electrically equivalent signals are then converted by the data acquisition system and are then utilized by the end devices in digital form. The ability of the electronic system to preserve signal accuracy and integrity is the main measure of the quality of the system.

The basic components required for the acquisition and conversion of analog signals into equivalent digital form are the following:

1. Analog Multiplexer and Signal Conditioning
2. Sample/Hold Amplifier
3. Analog-to-Digital Converter
4. Timing or Sequence Logic

Typically, today's data acquisition systems contain all the elements needed for data acquisition and conversion, except perhaps, for input filtering and signal conditioning prior to analog multiplexing. The analog signals are time multiplexed by the analog multiplier; the multiplexer output signal is then usually applied to a very-linear fast-settling differential amplifier and/or to a fast-settling low aperture sample/hold. The sample/hold is programmed to acquire and hold each multiplexed data sample which is converted into digital form by an A/D converter. The converted sample is then presented at the output of the A/D converter in parallel and serial digital form for further processing by the end devices.

SYSTEM SAMPLING RATE —

Error Considerations

The application and ultimate use of the converted data determines the required sampling and conversion rate of the data acquisition and conversion system. System sampling rate is determined, as shown in Figure 1, by the highest bandwidth channel, the number of data channels and the number of samples per cycle.

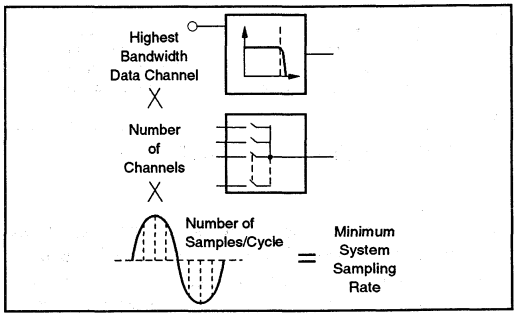


FIGURE 1. Determining Minimum System Sampling Rate.

Aliasing Error

From the Nyquist sampling theorem, a minimum of two samples per cycle of the data bandwidth is required in an ideal sampled data system to reproduce sampled data with no loss of information. Thus, the first consideration for determining system sampling rate is aliasing error, i.e., errors due to information being lost by not taking a sufficient number of samples per cycle of signal frequency.

Figure 2 illustrates aliasing error caused from an insufficient number of samples per cycle of data bandwidth.

How Many Samples per Cycle?

The answer to this question depends on the allowable average error tolerance, the method of reconstruction (if any), and the end use of the data. Regardless of the end use, the actual error of the discrete data samples will be equal to the throughput error of the data acquisition and conversion system plus any digital errors contributed by a digital computer or other digital end device.

For incremental devices such as stepping motors and switches, the average error of sampled digital data is not as important as it is for end devices that require continuous control signals. To illustrate average sampling error in sampled data

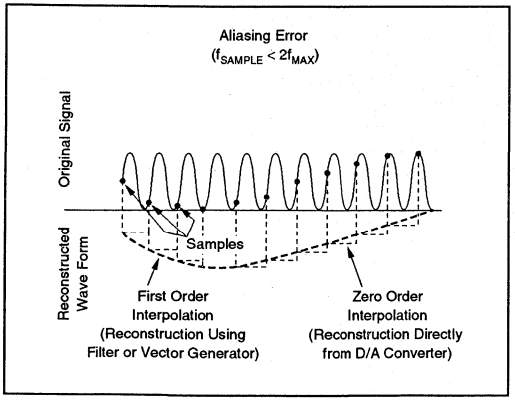


FIGURE 2. Aliasing Error vs Sampling Rate.

systems, consider the case where the minimum of 2 samples per cycle of sinusoidal data are taken, and the data is reconstructed directly from an unfiltered D/A converter (zero-order reconstruction). The average error between the reconstructed data and the original signal is one-half the difference in area for one-half cycle divided by π, or 32% for zero order data, and 14% for first order reconstruction. However, the instantaneous accuracy at each sample point is equal to the accuracy of the acquisition and conversion system, and in many applications, this may be sufficient for driving band-limited end devices. The average accuracy of sampled data can be improved by (1) increasing the number of samples per cycle; (2) presample filtering prior to multiplexing, or (3) filtering the D/A converter output.

The improvement in average accuracy of sampled data is dramatic with only a slight increase in the number of samples per cycle, as shown in Figure 4. The theoretical limit is the throughput accuracy of the acquisition and conversion system for continuous sampling.

For zero order reconstruction of data, it can be seen from Figure 4 that more than 10 samples per cycle of data bandwidth are required to reconstruct sampled data to average accuracies of 90% or better. A commonly used range is 7 to 10 samples per cycle.

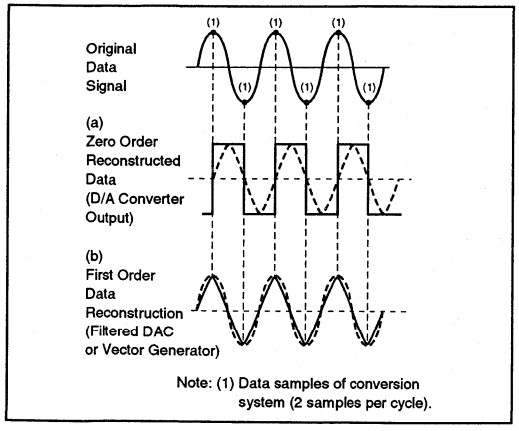


FIGURE 3. Reconstruction of Sampled Data Where $f_S = 2f_{MAX}$.

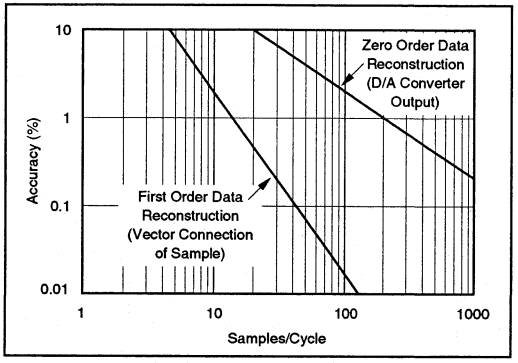


FIGURE 4. Reconstruction Accuracy vs Number of Samples Per Cycle.

Aperture Error

Aperture error is defined as the amplitude and time errors of the sampled data points due to the uncertainty of the dynamic data changes during sampling. In data acquisition and conversion systems, aperture error can be reduced or made insignificant either by the use of a sample/hold or with a very fast A/D converter.

For sinusoidal data, maximum aperture error occurs at the zero crossing where the greatest dv/dt occurs, and is expressed mathematically as:

$$\text{Aperture Error} = d\frac{(A \sin 2\pi ft)}{dt} \times t_A \times 100\%$$

$$= 2\pi f t_A \times 100\% \text{ max}$$

where f = maximum data frequency

t_A = aperture time of system (This can be the conversion time of the A/D converter with no sample/hold, or the aperture time of a sample/hold if one is in front of an A/D converter).

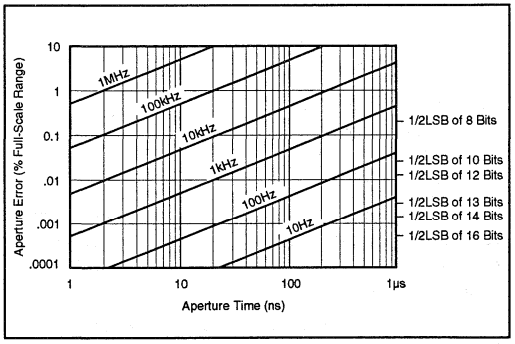


FIGURE 5. Aperture Error vs Aperture Time for Data Frequencies from 10Hz to 1MHz.

This expression is shown graphically in Figure 5 for frequencies of 10Hz to 1MHz with ±1/2LSB error highlighted for various n-bit resolution A/D converters. The need for a sample/hold becomes readily apparent when data frequencies of 10Hz or higher are sampled, because the A/D converter conversion speed must be 2µs or faster for aperture errors less than ±l/2LSB for 12-bit resolution, and high speed A/D converters are complicated and expensive when compared to slower A/D converters with a low aperture sample/hold.

A sample/ hold with an aperture time of 50ns to 60ns produces negligible aperture error for data frequencies up to 100Hz for 10- and 12-bit resolution A/ D converters, and is less than ±1/2LSB for 8-bit resolution for data frequencies near 5kHz. Use Figure 5 to determine your system aperture error for each data channel versus the desired resolution.

A FEW A/D CONVERTER POINTS

A brief discussion of A/D converter terminology will help the reader understand system resolution and accuracy a little better.

Accuracy

All analog values are presumed to exist at the input to the A/D converter. The A/D converter quantizes or encodes specific values of the analog input into equivalent digital codes as an output. These digital codes have an inherent uncertainty or *quantization error* of ±1/2LSB. That is, the quantized digital code represents an analog voltage that can be anywhere within ±1/2LSB from the mid-point between adjacent digital codes. An A/D converter can never be more accurate than the inherant ±1/2LSB quantizing error. Analog errors such as gain, offset, and linearity errors also affect A/D converter accuracy. Usually, gain and offset errors can be trimmed to zero, but *linearity error* is unadjustable because it is caused by the fixed-value ladder resistor network and network switch matching. Most quality A/D converters have less than ±1/2LSB linearity error. Another major error consideration is *differential linearity error.* The size of steps between adjacent transition points in an *ideal* A/D converter is one LSB. Differential linearity error is the difference between adjacent transition points in an actual A/D converter and an ideal one LSB step. This error must be less than one LSB in order to guarantee that there are no missing codes. An A/D converter with ±1/2LSB linearity error does not necessarily imply that there are no missing codes.

Selecting the Resolution

The number of bits in the A/D converter determines the resolution of the system. System resolution is determined by the channel(s) having the widest dynamic range and/or the channel(s) that require measurement of the smallest data increment. For example, assume a channel that measures pressure has a dynamic range of 4000psi that must be measured to the nearest pound. This will require an A/D converter with a minimum resolution of 4000 digital codes. A 12-bit A/D converter will provide a resolution of 2^{12} or 4096 codes—adequate for this requirement. The actual resolution of this channel will be 4000/4096 or 0.976psi.

The A/D converter can resolve this measurement to within ±0.488psi (±1/2LSB).

Resolution

The number of bits in an A/D converter determines the resolution of the data acquisition system. A/D converter resolution is defined as:

$$\text{Resolution} = \text{One LSB} = \frac{V_{FSR}}{2^n}, \text{ for binary A/D converters}$$

LSB = Least Significant Bit
V_{FSR} = Full Scale Input Voltage Range
where n = number of bits

The number of bits defines the number of digital codes and is 2^n discrete digital codes for A/D converters.

A/D Converter Resolution (Binary Code)		Value of 1LSB		Value of 1/2LSB	
Number of Bits (n)	Number Of Increments (2^n)	0 to +10V Range (mV)	±10V Range (mV)	0 to +10V Range (mV)	±10V Range (mV)
16	65536	0.152	0.305	0.076	0.152
12	4096	2.44	4.88	1.22	2.44
11	2048	4.88	9.77	2.44	4.88
10	1024	9.77	19.5	4.88	9.77
9	512	19.5	39.1	9.77	19.5
8	256	39.1	78.2	19.5	39.1

TABLE I. Relationship of A/D Converter LSB Values and Resolutions for Binary Codes.

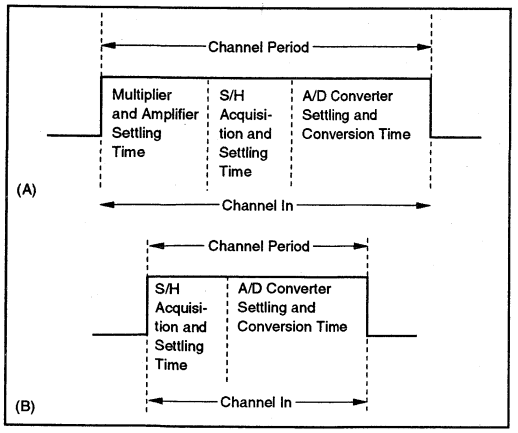


FIGURE 6. System Throughput Rate (a) Serial Multiplexing Programming (b) Overlap Multiplexing.

For this discussion, we will use binary successive-approximation A/D converters. Table I shows resolutions and LSB values for typical A/D converters.

INCREASING SYSTEM THROUGHPUT RATE

The throughput rate of the system is determined by the settling times required in the analog multiplexer and input amplifier, sample/hold acquisition time and A/D converter settling and conversion time.

Two methods that are commonly used in data acquisition systems are serial multiplexing (Figure 6a) and overlap multiplexing (Figure 6b). The multiplexer and amplifier settling time is eliminated by selecting the next sample (channel n + 1) while the held sample (channel n) is being converted. This requires a sample/hold with very low feedthrough error.

A wide range of throughput speeds can be achieved by "short cycling" the A/D converter to lower resolutions and by overlap multiplexing the data acquisition system.

SYSTEM THROUGHPUT ACCURACY

The most common method used to describe data acquisition and conversion system accuracy is to compute the root-sum squared (RSS) errors of the system components. The RSS error is a statistical value which is equivalent to the standard deviation (1σ), and represents the square root of the sum of the squares of the peak errors of each system component, including ADC quantization error:

$$\varepsilon_{RSS} = \sqrt{\varepsilon_{MUX}^2 + \varepsilon_{AMP}^2 + \varepsilon_{SH}^2 + \varepsilon_{ADC}^2}$$

where ε_{MUX} = analog multiplexer error
ε_{AMP} = input amplifier error
ε_{SH} = sample/hold error
ε_{ADC} = A/D converter error

The source irnpedance, data bandwidth, A/D converter resolution and system throughput rate affect these error calculations. To simplify, errors can be calculated by assuming the following:

1. Aperture error is negligible - i.e., less than 1/10LSB.
2. Source impedance is less than 1000Ω.
3. Signal range is ±10 volts.

PRACTICAL CONSIDERATIONS

No discussion of data acquisition systems would be complete without considering "real-world" issues faced by system designers. These are covered briefly. Each deserves fuller discussion on its own—but the various aspects of each are changing so quickly that any in-depth discussion is quickly outdated.

One consideration is the trade-off between a single A/D converter multiplexed between many analog signals and multiple converters, each dedicated to a single input. Currently, there are monolithic 12-bit A/D converters available with four or more multiplexed inputs and sample rates of 50 to 100kHz. For any system with bandwidths less than 1kHz per channel, these are ideal.

As the bandwidth approaches and exceeds 10kHz, more traditional data acquisition systems are needed.

Error Source	RESOLUTIONS		
	8 Bits	10 Bits	12 Bits
MUX Error	0.0025%	0.0025%	0.0025%
AMP Error	0.01%	0.01%	0.01%
S/H Error	0.01%	0.01%	0.01%
ADC Errors			
Analog	0.2%	0.05%	0.012%
Quantizing	0.2%	0.05%	0.012%
RSS Error	0.283%	0.072%	0.022%

TABLE III. System Error Contribution and RSS Error vs Resolution for a Typical Data Acquisition System.

SUMMARY

The criteria that determine the key parameters and performance requirements of a data acquisition and conversion system are:

1. Number of analog input channels
2. Amplitude of analog signals
3. Bandwidth of analog signals
4. Desired resolution of digital data
5. Practical considerations concerning power required, cost, and system design constraints.

Although this discussion did not treat all system criteria from a rigorous mathematical point of view, it does not identify and attempt to shed insight on the most important considerations from a practical viewpoint.

BURR-BROWN® APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

CODING SCHEMES USED WITH DATA CONVERTERS

Jason Albanus

With the recent proliferation of analog-to-digital converters (ADCs) and digital-to-analog converters (DACs), and the variety of digital coding schemes which they use, has come a need to understand these different coding schemes which converters use to talk to the "digital world". The purpose of this article is to describe the individual coding schemes used with ADCs and DACs manufactured by Burr-Brown, and explain their relationships.

Following this text is a list of abbreviations and definitions intended to clarify any questions regarding the nomenclature which has been used.

Throughout this guide, examples and tables given are for a 4-bit data converter. In unipolar and bipolar examples alike, the Full Scale Range (FSR) is 10V creating a V_{LSB} of 0.625V. For unipolar examples, minus full scale (–FS) is 0V and plus full scale (+FS) is 10V; for bipolar examples, –FS is –5V and +FS is +5V.

USB — UNIPOLAR STRAIGHT BINARY

The Unipolar Straight Binary coding is perhaps the simplest coding scheme to understand. As the name implies, it is a coding scheme which is used only for unipolar voltages.

When using USB coding, the digital count begins at all zeros (0000) at a V_{CODE} of 0V (V_{t+} = 0V + 1/2V_{LSB} and there is no V_{t-}). As the digital code increments, the analog voltage increases (one V_{LSB}) at a time, and the digital count ends (1111) at the positive full scale value. Table I shows how the USB codes correspond to analog voltages for a 4-bit digital system.

MNEMONIC	DIGITAL CODE	V_{t-}	V_{CODE}	V_{t+}
Zero	0000		0.000	0.3125
+1 V_{LSB}	0001	0.3125	0.625	0.9375
	0010	0.9375	1.250	1.5625
	0011	1.5625	1.875	2.1875
1/4 FSR	0100	2.1875	2.500	2.8125
	0101	2.8125	3.125	3.4375
	0110	3.4375	3.750	4.0625
	0111	4.0625	4.375	4.6875
1/2 FSR	1000	4.6875	5.000	5.3125
	1001	5.3125	5.625	5.9375
	1010	5.9375	6.250	6.5625
	1011	6.5625	6.875	7.1875
3/4 FSR	1100	7.1875	7.500	7.8125
	1101	7.8125	8.125	8.4375
	1110	8.4375	8.750	9.0625
+FS	1111	9.0625	9.375	

TABLE I. USB Coding Scheme.

Unipolar Straight Binary is the coding scheme used by the ADC7802 and ADS7803.

CSB — COMPLEMENTARY STRAIGHT BINARY

The Complementary Straight Binary coding scheme is the exact digital opposite (one's complement) of Unipolar Straight Binary. CSB coding, like its counterpart USB, is also restricted to unipolar systems.

When using CSB coding with a digital system, the digital count begins at all zeros (0000) at the positive full scale value. As the digital code increments, the analog voltage decreases one V_{LSB} at at time, until 0V is reached at a digital code of 1111. The relationship between CSB coding and its corresponding analog voltages can be seen in Table II.

MNEMONIC	DIGITAL CODE	V_{t-}	V_{CODE}	V_{t+}
Zero	1111		0.000	0.3125
+1V_{LSB}	1110	0.3125	0.625	0.9375
	1101	0.9375	1.250	1.5625
	1100	1.5625	1.875	2.1875
1/4 FSR	1011	2.1875	2.500	2.8125
	1010	2.8125	3.125	3.4375
	1001	3.4375	3.750	4.0625
	1000	4.0625	4.375	4.6875
1/2 FSR	0111	4.6875	5.000	5.3125
	0110	5.3125	5.625	5.9375
	0101	5.9375	6.250	6.5625
	0100	6.5625	6.875	7.1875
3/4 FSR	0011	7.1875	7.500	7.8125
	0010	7.8125	8.125	8.4375
	0001	8.4375	8.750	9.0625
+FS	0000	9.0625	9.375	

TABLE II. CSB Coding Scheme.

BOB — BIPOLAR OFFSET BINARY

Bipolar Offset Binary coding, as the name implies, is for use in bipolar systems (where the analog voltage can be positive and negative). This coding scheme is very similar to USB coding since, as the analog voltage increases, the digital count also increases.

BOB coding begins with digital zero (0000) at the negative full scale. By incrementing the digital count, the corresponding analog value will approach the positive full scale in one V_{LSB} steps, passing through bipolar zero on the way. This "zero crossing" occurs at a digital code of 1000 (see Table

III). The digital count continues to increase proportionally to the analog input until the positive full scale is reached at a full digital count (1111) as shown by Table III.

With BOB coding, the MSB can be considered a sign indicator whereas a logic "0" indicates a negative analog value, and a logic "1" indicates an analog value greater than or equal to BPZ.(1)

MNEMONIC	DIGITAL CODE	V_{t-}	V_{CODE}	V_{t+}
–FS	0000		–5.000	–4.6875
	0001	–4.6875	–4.375	–4.0625
	0010	–4.0625	–3.750	–3.4375
	0011	–3.4375	–3.125	–2.8125
1/2 –FS	0100	–2.8125	–2.500	–2.1875
	0101	–2.1875	–1.875	–1.5625
	0110	–1.5625	–1.250	–0.9375
BPZ – $1V_{LSB}$	0111	–0.9375	–0.625	–0.3125
BPZ	1000	–0.3125	0.000	+0.3125
BPZ + $1V_{LSB}$	1001	+0.3125	+0.625	+0.9375
	1010	+0.9375	+1.250	+1.5625
	1011	+1.5625	+1.875	+2.1875
1/2 +FS	1100	+2.1875	+2.500	+2.8125
	1101	+2.8125	+3.125	+3.4375
	1110	+3.4375	+3.750	+4.0625
+FS	1111	+4.0625	+4.375	

TABLE III. BOB Coding Scheme.

The ADS7800, a 12-bit, 333kHz, sampling analog-to-digital converter, utilizes the Bipolar Offset Binary output code to implement its ±5 and ±10V input ranges. The DAC780x series of digital-to-analog converters also use this scheme in each of their three different interface formats (serial, 8-bits

Complementary Offset Binary coding, like its counterpart BOB, is also for use in systems where the analog signal is bipolar. The relationship between COB and BOB is that each coding scheme is the one's complement (all bits inverted) of the other.

COB coding begins with digital zero (0000) at the positive full scale. By incrementing the digital count, the corresponding analog value will approach the negative full scale in one V_{LSB} steps, passing through bipolar zero on the way. This "zero crossing" occurs at a digital code of 0111 (see Table IV). As the digital count continues to increase, the analog signal goes more negative until the negative full scale is reached at a full digital count (1111) as shown by Table IV.

With COB coding, like BOB coding, the MSB can also be considered a sign indicator whereas a logic "1" indicates a negative analog value, and a logic "0" indicates an analog value greater than or equal to BPZ.(2)

MNEMONIC	DIGITAL CODE	V_{t-}	V_{CODE}	V_{t+}
–FS	1111		–5.000	–4.6875
	1110	–4.6875	–4.375	–4.0625
	1101	–4.0625	–3.750	–3.4375
	1100	–3.4375	–3.125	–2.8125
1/2 –FS	1011	–2.8125	–2.500	–2.1875
	1010	–2.1875	–1.875	–1.5625
	1001	–1.5625	–1.250	–0.9375
BPZ – $1V_{LSB}$	1000	–0.9375	–0.625	–0.3125
BPZ	0111	–0.3125	0.000	+0.3125
BPZ + $1V_{LSB}$	0110	+0.3125	+0.625	+0.9375
	0101	+0.9375	+1.250	+1.5625
	0100	+1.5625	+1.875	+2.1875
1/2 +FS	0011	+2.1875	+2.500	+2.8125
	0010	+2.8125	+3.125	+3.4375
	0001	+3.4375	+3.750	+4.0625
+FS	0000	+4.0625	+4.375	

TABLE IV. COB Coding Scheme.

BTC — BINARY TWO'S COMPLEMENT

Binary Two's Complement coding is the type of coding used by most microprocessor or math processor based systems for mathematical algorithms, and is also the coding scheme which the digital audio industry has decided to use as its standard.

Binary Two's Complement coding is also a scheme designed for bipolar analog signals. It is very similar to BOB, but does not appear so. The only difference between BOB and BTC is that the MSB has been inverted.

Unfortunately, BTC is not as straightforward as the schemes previously mentioned. The codes are not continuous from

count increments to its maximum positive code of 0111 as the analog voltage approaches and reaches its positive full scale value. The code then resumes at the negative full scale value at a digital code of 1000, and then approaches BPZ until a digital value of 1111 is reached at one LSB value below BPZ (see Table V).

With the BTC coding scheme, the MSB can also be considered a sign indicator. When the MSB is a logic "0" a positive value is indicated, and when the MSB is a logic "1" a negative value is indicated.(3)

This is the coding scheme which is used with Burr-Brown's DSP interface chips (DSP101/DSP102 analog input and DSP201/DSP202 analog output) designed for "zero chip interface" to most of the popular digital signal processors available today. Binary Two's Complement is also one of the codes utilized by the ADC603 and ADC614 high speed analog-to-digital converters, and, of course, all of Burr-Brown's PCM digital audio converters.

NOTE: (1) The V_{t+} transition to BPZ from a negative value (0111 to 1000) actually occurs at –0.3125V causing the MSB to go "positive" at a negative value. (2) The V_{t+} transition to BPZ from a negative value (1000 to 0111) actually occurs at –0.3125V causing the MSB to go "positive" at a negative value. (3) The V_{t+} transition to BPZ from a negative value (1111 to 0000) actually occurs at –0.3125V causing the MSB to go "positive" at a negative value.

MNEMONIC	DIGITAL CODE	V_{t-}	V_{CODE}	V_{t+}
–FS	1000		–5.000	–4.6875
	1001	–4.6875	–4.375	–4.0625
	1010	–4.0625	–3.750	–3.4375
	1011	–3.4375	–3.125	–2.8125
1/2 –FS	1100	–2.8125	–2.500	–2.1875
	1101	–2.1875	–1.875	–1.5625
	1110	–1.5625	–1.250	–0.9375
BPZ – $1V_{LSB}$	1111	–0.9375	–0.625	–0.3125
BPZ	0000	–0.3125	0.000	+0.3125
BPZ + $1V_{LSB}$	0001	+0.3125	+0.625	+0.9375
	0010	+0.9375	+1.250	+1.5625
	0011	+1.5625	+1.875	+2.1875
1/2 +FS	0100	+2.1875	+2.500	+2.8125
	0101	+2.8125	+3.125	+3.4375
	0110	+3.4375	+3.750	+4.0625
+FS	0111	+4.0625	+4.375	

TABLE V. BTC Coding Scheme.

MNEMONIC	DIGITAL CODE	V_{t-}	V_{CODE}	V_{t+}
–FS	0111		–5.000	–4.6875
	0110	–4.6875	–4.375	–4.0625
	0101	–4.0625	–3.750	–3.4375
	0100	–3.4375	–3.125	–2.8125
1/2 –FS	0011	–2.8125	–2.500	–2.1875
	0010	–2.1875	–1.875	–1.5625
	0001	–1.5625	–1.250	–0.9375
BPZ – $1V_{LSB}$	0000	–0.9375	–0.625	–0.3125
BPZ	1111	–0.3125	0.000	+0.3125
BPZ + $1V_{LSB}$	1110	+0.3125	+0.625	+0.9375
	1101	+0.9375	+1.250	+1.5625
	1100	+1.5625	+1.875	+2.1875
1/2 +FS	1011	+2.1875	+2.500	+2.8125
	1010	+2.8125	+3.125	+3.4375
	1001	+3.4375	+3.750	+4.0625
+FS	1000	+4.0625	+4.375	

TABLE VI. CTC Coding Scheme.

CTC — COMPLEMENTARY TWO'S COMPLEMENT

Complementary Two's Complement coding is also a scheme designed for bipolar analog signals. It is the one's complement of its counterpart BTC, and is also very similar to COB, although this relationship is not immediately obvious. The only difference between COB and CTC is that the MSB has been inverted.

With CTC coding, digital "zero" is at an analog voltage which is slightly less (1 LSB) than analog bipolar zero. As the digital count increments, the analog voltage becomes more negative until all of the bits are high except for the MSB (0111). At this point, the digital code corresponds to the analog negative full scale. The next step in incrementing

With Complementary Two's Complement coding, the MSB is also a sign indicator with its states of "0" and "1" representing negative and positive voltages, respectively.

This code is also used by Burr-Brown's high speed ADC603 and ADC614. These converters accomplish this dual code task by providing an input for code selection.

MANIPULATING BETWEEN VARIOUS CODES

The input and output codings used with ADCs and DACs is varied, and an individual converter may be capable of utilizing one or more coding scheme. However, with all of these schemes available, the desired scheme is not always readily available with the particular converter of interest. Do not fear, because converting one coding scheme to another, to match a particular system, is very easy as long as you wish to convert a bipolar scheme to another bipolar scheme; or a unipolar scheme into another unipolar scheme. The only devices required for any transformation are digital logic "inverters", however, some of the transformations can be achieved by using analog components.(4) The following section will be divided into sections depending on how the transformation is to be accomplished.

Inversion of all Bits

USB to CSB and CSB to USB
BOB to COB and COB to BOB
BTC to CTC and CTC to BTC

The CSB scheme is simply the USB code with all of the bits inverted (one's complement). This is also how to perform most of the transformation of BOB to COB, and BTC to

of –1V/V (see Figure 2). This op amp can be used on the input stage of an ADC or the output stage of a DAC. Some sample and hold amplifiers, such as the SHC5320, are configurable for a gain of –1V/V, providing very easy conversion between these codes in an analog-to-digital system. Remember that either $+1V_{LSB}$ or $-1V_{LSB}$ must be summed in with the analog value.

The bipolar transformations may be quite straightforward when done in the analog domain; however, to convert digitally, an individual logic "inverter" must be used on every data line, input or output (see Figure 1), as with the unipolar schemes.

The ADC603 and ADC614 allow both BTC and CTC coding schemes by providing an "Output Logic Invert" input pin. This flexibility allows these converters to be used in even more applications easier than if just one scheme had been implemented.

NOTE: (4) When converting bipolar digital schemes, regardless of whether the transformation is done digitally or in an analog fashion, a value of either $+1V_{LSB}$ or $-1V_{LSB}$ must be summed in with the analog value. This is due to the assymetric nature of the codes around bipolar zero (see definition of V_t). This addition of one V_{LSB} is relatively simple, since most data converters allow for an offset adjustment which can accomodate this.

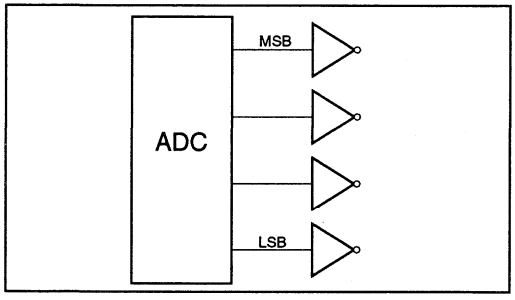


FIGURE 1. Digital Inversion of All Bits.

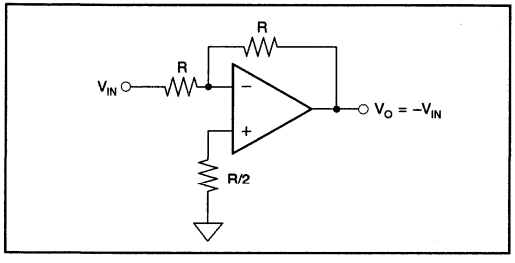


FIGURE 2. Analog Signal Inversion.

Inversion of the MSB

BOB to BTC and BTC to BOB
COB to CTC and CTC to COB

Manipulating the BOB scheme into BTC and manipulating COB into CTC requires much less hardware. To go from BOB to BTC, or COB to CTC (or vice versa) it is only necessary to invert the MSB (see Figure 3).

Burr-Brown's PCM78, a 16-bit ADC developed for digital audio applications allows BOB or BTC output schemes by providing a "BOB/BTC select" input. Open circuit or grounding of this pin provides for BTC and BOB respectively by controlling an internal inverter for the most significant bit.

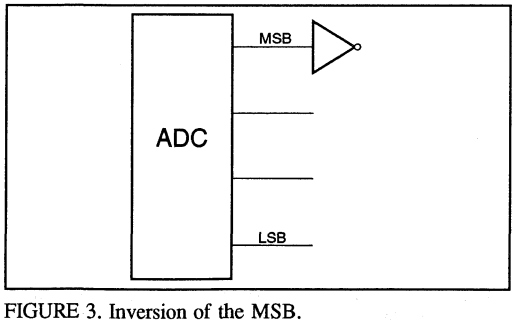


FIGURE 3. Inversion of the MSB.

Inversion of all bits except the MSB

BOB to CTC and CTC to BOB
BTC to COB and COB to BTC

Manipulation of BOB into CTC and BTC into COB requires inverting all bits except the MSB. This is also a difficult transformation to accomplish, since it would require a digital inverter for every bit except the most significant bit (see Figure 4).

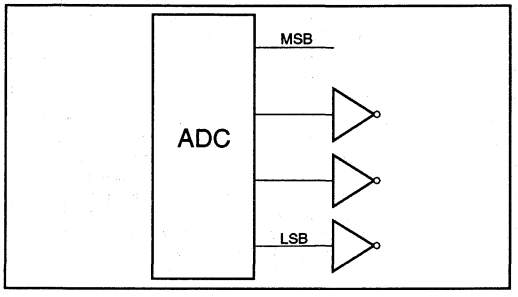


FIGURE 4. Inversion of All Bits Except the MSB.

DEFINITIONS

n	=	Number of bits in a particular digital system.
LSB	=	Least Significant Bit — The digital bit with the least analog "weight".
MSB	=	Most Significant Bit — The digital bit with the greatest analog "weight".
Increment	=	To increase a digital "count", or to count up, as in a code changing from 0000 to 0001.
Decrement	=	To decrease a digital "count", or to count down, as in a code changing from 0001 to 0000.
USB	=	Unipolar Straight Binary coding.
CSB	=	Complementary Straight Binary coding.
BOB	=	Bipolar Offset Binary coding.
COB	=	Complementary Offset Binary coding.
BTC	=	Binary Two's Complement coding.
CTC	=	Complementary Two's Complement coding.
FSR	=	Full Scale Range — The dynamic range of an analog signal.
BPZ	=	Bipolar Zero — An analog voltage of 0V.
V_{LSB}	=	Least Significant Bit Voltage — The value of voltage represented by one LSB. For digital-to-analog converters which provide a current output mode of operation, V_{LSB} actually refers to a voltage after a current-to-voltage conversion. Throughout the text, it is presumed that this current to voltage conversion has taken place. $V_{LSB} = FSR/2^n$ **(Equation 1)**

DEFINITIONS (CONT)

V_{CODE} = Code Voltage —The voltage corresponding to a particular digital code in an ideal converter. For digital-to-analog converters which provide a current output mode of operation, V_{CODE} actually referes to a voltage after a current-to-voltage conversion. Throughout the text, it is presumed that this current-to-voltage conversion has occurred.

V_{CODE} = (digital code)$_{10}$ * V_{LSB} **(Equation 2)**

For analog-to-digital converters, the code voltage is actually an analog range of voltages encompassed by $V_{CODE} \pm 1/2V_{LSB}$. This is due to the inherent quantization error of $\pm 1/2V_{LSB}$ that is present in the finite digital output of the ADC.

The value of (digital code)$_{10}$ * V_{LSB} will be used throughout this text to represent V_{CODE} unless otherwise stated.

+FS = Positive Full Scale —The most positive end of an analog signal's range which is represented by a digital code. A V_{CODE} equal to the positive full range (+FS) does not exist. The industry standard is that the most positive voltage corresponding to a digital code (maximum V_{CODE}) is the positive full scale voltage minus the voltage associated with one LSB (+FS – $1V_{LSB}$). The text "positive full scale" (or +FS) refers to this lesser, industry standard value. This +FS industry standard is primarily due to another industry standard in which 0V is a code voltage (see Equation 3) bounded by the absolute value of $\pm 1/2V_{LSB}$. In a unipolar system, this means that the analog voltage range represented by a digital code corresponding to BPZ is only $1/2V_{LSB}$. In bipolar systems, all digital codes have analog ranges of $1V_{LSB}$, and a digital code representing 0V is 0V $\pm 1/2V_{LSB}$ (see Equation 3 and Equation 4).

–FS = Negative Full Scale — The most negative end of an analog signal's range which is represented by a digital code.

V_t = Transition voltage — The voltage which corresponds to the actual change of a digital code in an ideal analog-to-digital converter. These voltages are the voltages at each end of the range of $V_{CODE} \pm 1/2V_{LSB}$.

$V_{t+} = V_{CODE} + 1/2V_{LSB}$ **(Equation 3)**

$V_{t-} = V_{CODE} - 1/2V_{LSB}$ **(Equation 4)**

For an ideal digital-to-analog converter, the output would be exactly V_{CODE}, and the transition voltage can be ignored.

BURR-BROWN® APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

INCREASING INA117 DIFFERENTIAL INPUT RANGE

By R. Mark Stitt (602) 746-7445

The INA117 is a monolithic difference amplifier with the unique ability to accept up to ±200V common-mode input signals while operating on standard ±15V power supplies. Because the gain of the INA117 is set at 1V/V, and because the output would saturate into the rails at about ±12V, the maximum specified differential input range is ±10V.

Since the common-mode input range is ±200V, it makes sense that some designers would also like to use the part for differential inputs greater than ±10V. Figure 1 shows the recommended circuit. Adding resistors to the input may seem simpler, but there are some problems with that approach.

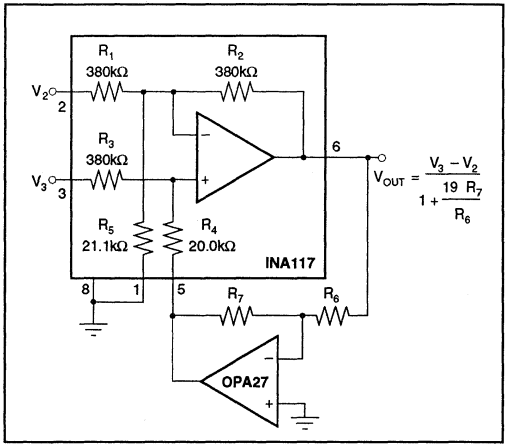


FIGURE 1. INA117 with Increased Differential Input Range.

The performance of the INA117 depends on extremely precise resistor matching (0.005% for 86dB CMR). Resistors added to the input must be adjusted to at least this accuracy to maintain high performance. Both gain error and CMR must be adjusted. Maintaining 86dB CMR over temperature requires 1ppm/°C resistor TCR tracking. Significant resistance added external to the INA117 would require the same performance.

By using the circuit shown in Figure 1, internal resistor matching is preserved, and the INA117 CMR and CMR drift with temperature are maintained. Gain can be set independently of CMR by adjusting the inverter resistors, R_6, R_7. Gain drift is preserved so long as R_6 and R_7 track with temperature. Furthermore, noise at the output is improved by the gain reduction factor whereas it is unchanged with the other approach.

To understand how the circuit works, consider the INA117 to be a four-input summing amplifier as shown in Figure 2.

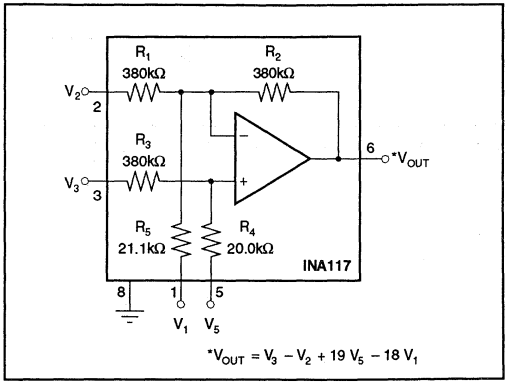


FIGURE 2. INA117 Shown as a Four-Input Summing Amplifier.

CMR is preserved and the gain is reduced if a small portion of the output signal is inverted and fed back to pin 5 with V_1 set to zero (V_1 grounded).

Where: $V_{OUT} = V_3 - V_2 + 19 \bullet V_5 - 18 \bullet V_1$

If, $V_5 = -V_{OUT} \bullet R_7/R_6$, then

$$V_{OUT} = \frac{V_3 - V_2}{1 + \frac{19 \bullet R_7}{R_6}}$$

SELECTED-GAIN EXAMPLES

GAIN[1] (V/V)	R_7 (kΩ)	R_6 (kΩ)
1/2	1.05	20.0
1/4	3.16	20.0
1/5	4.22	20.0

NOTE: (1) INA117 is not stable in Gain < 1/5.

If CMR adjustment is desired, add a 10Ω fixed resistor and a 20Ω pot as shown in Figure 3. Adjust CMR by shorting together pins 2 and 3 of the INA117 and driving them with a 500Hz square wave while observing the output on a scope. Using a square wave rather than a sine wave allows the AC signal to settle out so that the DC CMR can be seen. The CMR trim will change the gain slightly, so trim CMR first, then trim gain with R_6, R_7 if desired.

The INA117 is now available in three standard 8-pin packages: hermetic TO-99, plastic DIP, and the small surface-mount SOIC package.

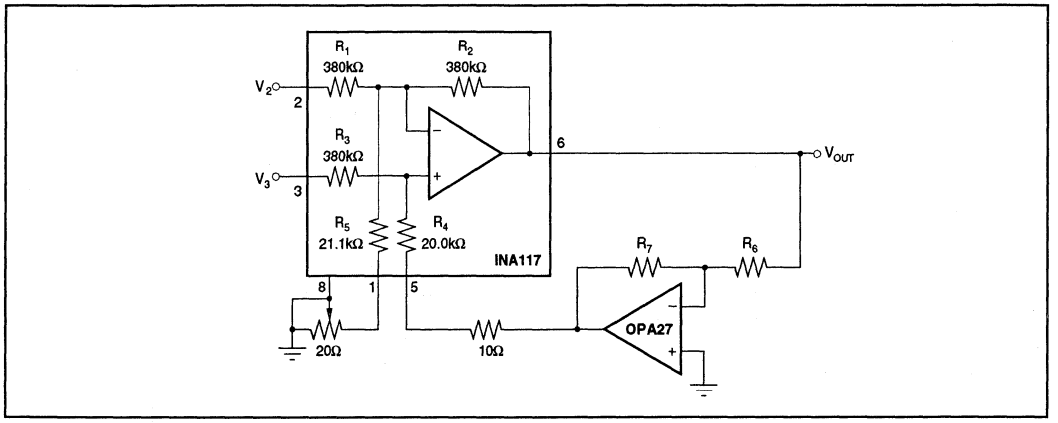


FIGURE 3. INA117 with Increased Differential Input Range with CMR Trim.

BURR-BROWN®
APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

AC COUPLING INSTRUMENTATION AND DIFFERENCE AMPLIFIERS

FEATURING CIRCUITS FOR:

INA117 ±200V DIFFERENCE AMPLIFIER • INA106-BASED ±100V DIFFERENCE AMPLIFIER • INA105 AND INA106 G = 1, 10 DIFFERENCE AMPLIFIERS • INA101, INA102, INA103, INA110, INA120 INSTRUMENTATION AMPLIFIERS

By R. Mark Stitt (602) 746-7445

The need to glean AC signals from DC in the presence of common-mode noise frequently occurs in signal conditioning applications. AC coupling to an instrumentation amplifier (IA) or difference amplifier can be used to accurately extract the AC signal while rejecting DC and common-mode noise.

Adding capacitors and resistors to AC couple the inputs of an instrumentation amplifier or difference amplifier seems like an obvious approach for AC coupling, but it has problems. The DC restoration circuits shown in this bulletin have the same transfer function but without the foibles.

Common-mode rejection of a difference amplifier depends on extremely precise matching of input source impedance. Adding RC networks to the inputs of either an IA or a difference amplifier can significantly degrade the CMR, especially for AC inputs. Even if the CMR is trimmed, maintaining performance over temperature can be a problem.

The DC restoration circuits shown solve this problem by placing a low-pass network in the feedback to the reference pin of the IA or difference amplifier. The low-pass pole translates into a high-pass function as referred to the input with f_{-3dB} = Gain/2•π•R•C. The Gain term refers to the Gain from the reference pin to the output of the IA or difference amplifier. The selection guide shows this Gain term as the "High-pass multiplier".

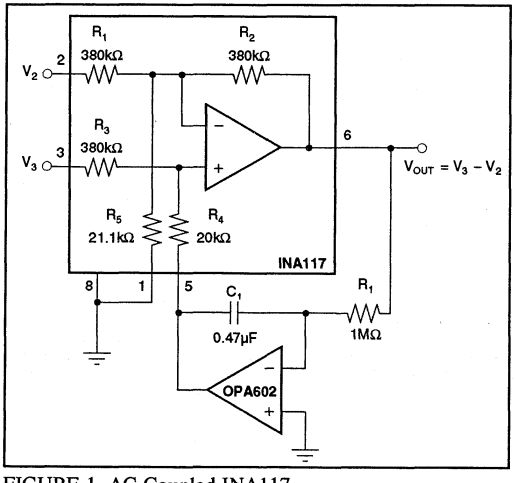


FIGURE 1. AC-Coupled INA117.

The DC-restored INA117 is shown in Figure 1. With the values shown, the high-pass zero is ≈6.5Hz.

The INA117BM has a CMR of 86dB min. If improved CMR is required for the DC restored INA117, use the circuit shown in Figure 2. Since the trim resistors are small, they will not degrade the stability or drift performance of the INA117.

The INA117 has a common-mode input range and differential offset range of up to ±200V. If a lower common-mode and differential offset range of ±100V is acceptable, the INA106 can be used for lower noise and twice the small signal bandwidth (400kHz vs 200kHz).

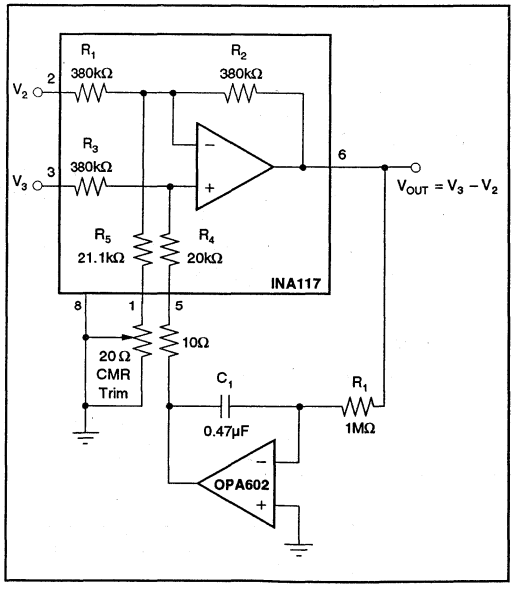


FIGURE 2. AC-Coupled INA117 with CMR Trim.

The simplest circuit for the DC-restored INA106 is shown in Figure 3. The INA106 is reversed from its normal Gain-of-10 configuration. The 100kΩ, 10kΩ resistors form a 11/1 voltage divider on the input so that ±100V at pins 1 and 5 are divided down to less than ±10V at the op amp inputs. The R_5, R_6 network provides the proper feedback Gain for an overall unity-gain transfer function. Since the precise resistor matching of the INA106 is disturbed by the R_5, R_6 network this circuit requires trims for both CMR and Gain.

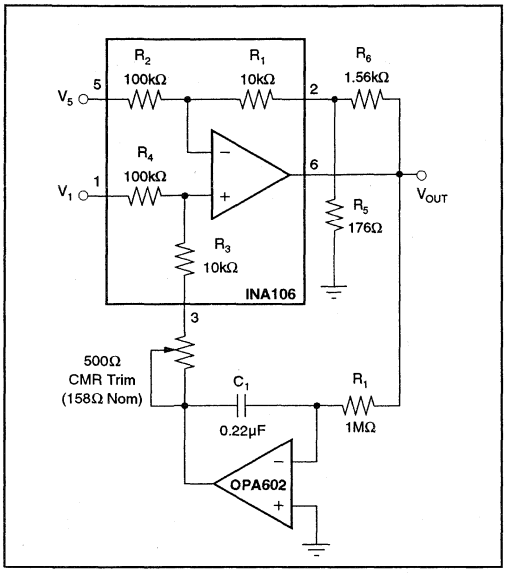


FIGURE 3. AC-Coupled ±100V Difference Amp Using the INA106.

Furthermore, Gain and CMR adjustments using R_5, R_6, and the 500Ω trim pot connected to pin 3 are interactive. The excellent CMR stability vs time and temperature of the INA106 is preserved since the added trim resistors are small.

If you want to use the INA106 for a ±100V DC-restored difference amplifier without any trims, use the circuit shown in Figure 4. Gain is set directly by the R_5, R_6 divider. The buffer amplifier, A_2, presents a low impedance to the feedback resistor in the INA106 to preserve resistor matching and CMR.

When using the DC restored ±100V difference amplifier shown in Figure 4, no trims are required for good CMR. However, the circuit shown in Figure 5 may be used to fine trim CMR if desired. Since the added trim resistors are small, they will not degrade the stability or drift of the INA106.

DC restoration can be used with any of the standard IAs shown in the table using the same technique as shown in Figure 6. Since all of these IAs use unity-Gain difference amplifiers, the high-pass multiplier is unity.

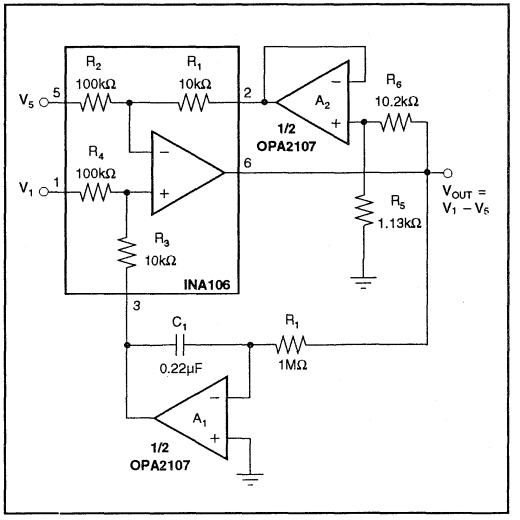


FIGURE 4. AC-Coupled ±100V Difference Amp Using the INA106 Requires No Trims.

SELECTION GUIDE

(AC-coupled difference and instrumentation amplifiers)

V_S = ±15V

MODEL	GAIN [V/V]	COMMON MODE INPUT RANGE [V]	DIFFERENTIAL OFFSET RANGE [V]	NOISE (RTI) [nV/√Hz]	BANDWIDTH (–3dB) [Hz]	HIGH PASS MULTIPLIER (See Text)
INA117	1	±200	±200	550	200k	19
INA106(1)	1	±100	±100	300	400k	10
INA105	1	±20	±10	60	1M	1
INA106	10	±11	±1	30	500k	1
INA101 INA102 INA103 INA110 INA120	(2)	±7 (3)	±10	1 (2)	6M (2)	1

NOTES (1) Reverse-connected, see figures 3,4, and 5. (2) Gain is adjustable from 1 to 1000+. Noise and bandwidth depend on Gain setting. INA103 has the lowest noise: 1nV/√Hz, Gain = 1000. INA103 has the highest bandwidth: 6MHz, Gain = 1. INA102 is low power (750µA max). INA110 has FET inputs (I_B = 50pA max). INA101 has lowest drift (.25µV/°C max). INA120 is a lower IQ INA101 with internal resistors for Gains of 1, 10, 100, and 1000. (3) Yes!, the common-mode input range of standard IAs is only about ±7V with ±10V V_{OUT}; see "Extended Common-Mode Instrument Amps", *Electronic Design*, December 22, 1988, pp 67, 68.

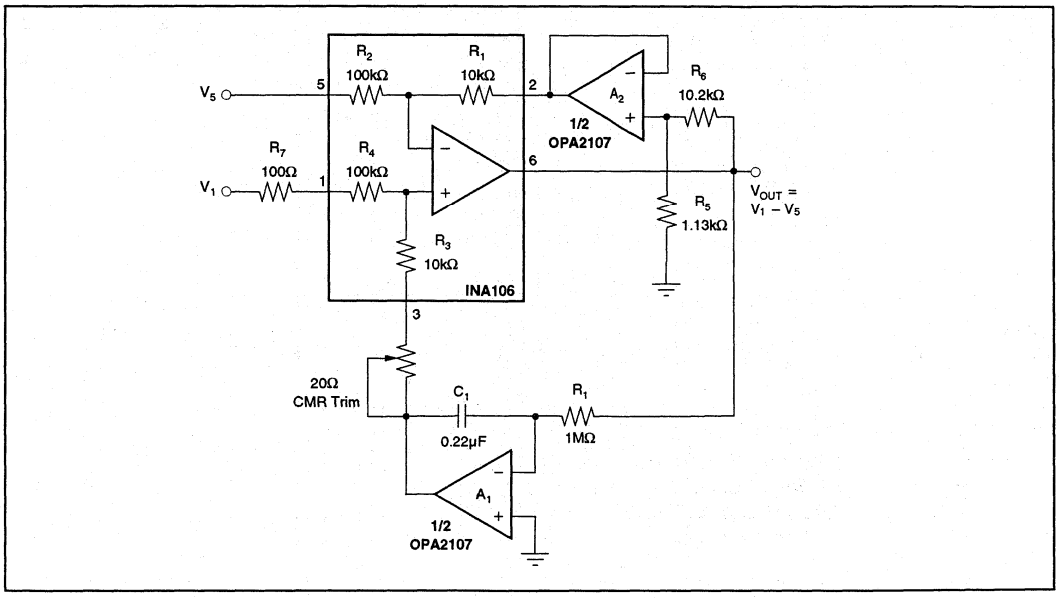


FIGURE 5. AC-Coupled ±100V Difference Amp Uses the INA106. Has CMR Trim.

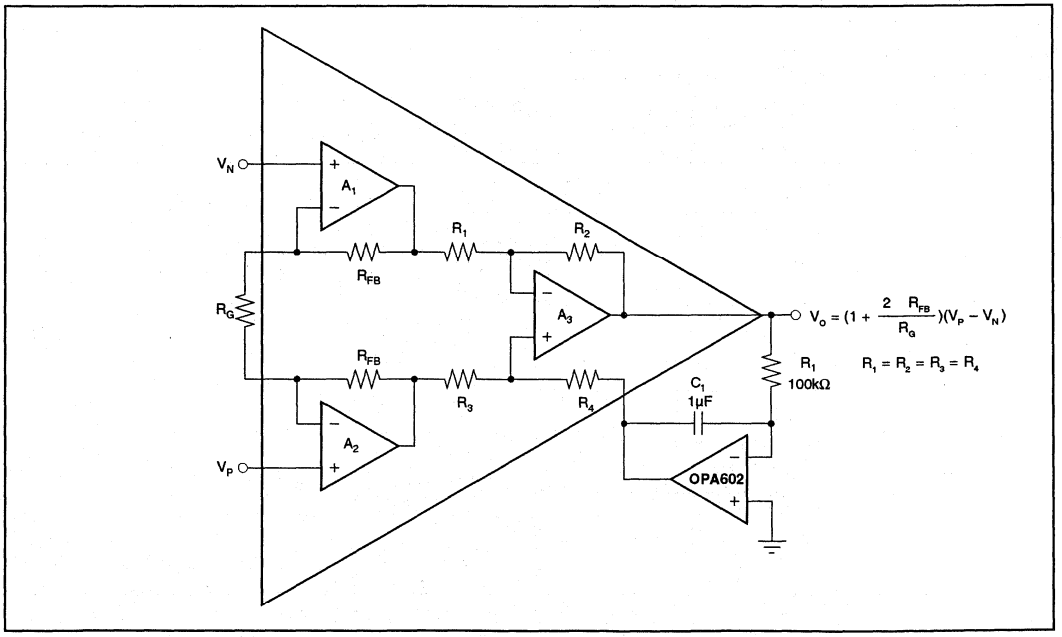


FIGURE 6. General AC-Coupled IA Circuit

BURR-BROWN® APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

±200V DIFFERENCE AMPLIFIER WITH COMMON-MODE VOLTAGE MONITOR

By Art Gass and R. Mark Stitt (602) 746-7445

The INA117 is a monolithic difference amplifier with the unique ability to accept up to ±200V common-mode input signals while operating on standard ±15V power supplies. Using on-chip high-voltage resistor dividers, the INA117 rejects common-mode signals up to ±200V and translates a 0V to ±10V differential input signal to a 0V to ±10V ground-referenced output signal.

In some applications it is also necessary to monitor the common-mode level of the input signal. A common-mode level monitor can be implemented with the addition of an external op amp or two. Even though standard signal level op amps are used, the circuit remains protected for momentary common-mode or differential overloads up to ±500V.

If precision is not required, the circuit shown in Figure 1 can be used to monitor the common-mode voltage with a maximum error of about ±5V. This implementation actually monitors the common-mode level of the INA117 noninverting input (pin 3). The circuit works by measuring the current in reference pins 1 and 5, which are normally connected to ground. Amplifier A_1 forces the reference pins to a virtual ground through feedback resistors $R_6 + R_7$. The normal operation of the INA117 is unaffected since its reference pins are connected to virtual ground. Resistors R_3 and R_4 in the INA117 form a voltage divider so that the top of R_4 is at $V_3/20$. Feedback of the op amp in the INA117 forces the voltage of its inverting input to be equal to its noninverting input so that the top of resistor R_5 is also at $V_3/20$. The common mode level of V_3 is therefore related to the current flowing out of pins 1 and 5.

$$I_{1+5} = (V_3/20)/(R_4 \parallel R_5)$$

If

$$R_6 + R_7 = R_4 \parallel R_5$$

then

$$A_{1\,OUT} = -V_3/20.$$

Where

I_{1+5} = total current flowing out of INA117 pins 1 and 5 [A]

$R_4 \parallel R_5$ = parallel combination of R_4 and R_5 [Ω]

$R_4 \parallel R_5 = (R_4 \cdot R_5)/(R_4+R_5)$, nominally 10.27kΩ

$A_{1\,OUT}$ = A_1 output voltage [V]

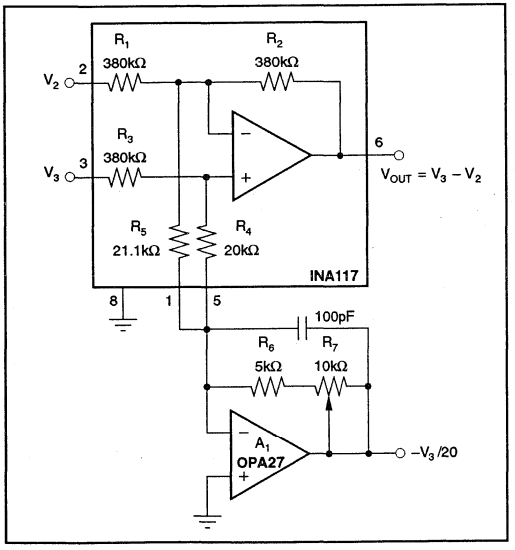


FIGURE 1. INA117 with V_3 Common-Mode Voltage Monitor.

The signal is scaled by 1/20 so the output of A_1 does not exceed its maximum of ±10V with common-mode inputs of ±200V. If smaller maximum common-mode voltages are to be monitored, the value of $R_6 + R_7$ can be increased for more gain.

Although the resistor ratios in the INA117 are accurately laser trimmed, the absolute resistor values can vary by as much as ±25%. For better accuracy, the circuit must be calibrated. To calibrate the gain, short pins 2 and 3 of the INA117 to ground, offset adjust A_1 for 0V at its output, connect pins 2 and 3 to a known V_{REF} (such as +10V or +100V), and adjust R_7 for an A_1 output of $-V_{REF}/20$.

By definition, the true common-mode input voltage of the INA117 is $(V_2 + V_3)/2$. The actual common-mode voltage can be monitored with the addition of a second op amp as shown in Figure 2. The second op amp is connected to sum the $-V_3/20$ output of A_1 at a gain of –1V/V with the $V_3 - V_2$ output of the INA117 at a gain of –1/40V/V to produce an output of $V_{CM}/20$.

Calibrate the Figure 2 circuit as before, adjusting R_7 for an A_2 output of $V_{REF}/20$. Then, ground pin 3 of the INA117, connect pin 2 to +10V and trim R_9 for 0.025V at the output of A_2. If resistors R_8, R_9, and R_{10} accurately ratio match, adjustment of R_9 is unnecessary.

Of course, if connection of additional components to the INA117 inputs is acceptable, the circuits shown in Figures 3 and 4 can be used to monitor the common-mode input voltage. With these circuits, calibration is not required if accuracy commensurate with the tolerance of R_6, R_7, and R_8 is acceptable. As before, either R_7 or R_8 can be omitted to monitor the common-mode voltage of just one input. If R_7 or R_8 is omitted, double the value of R_6.

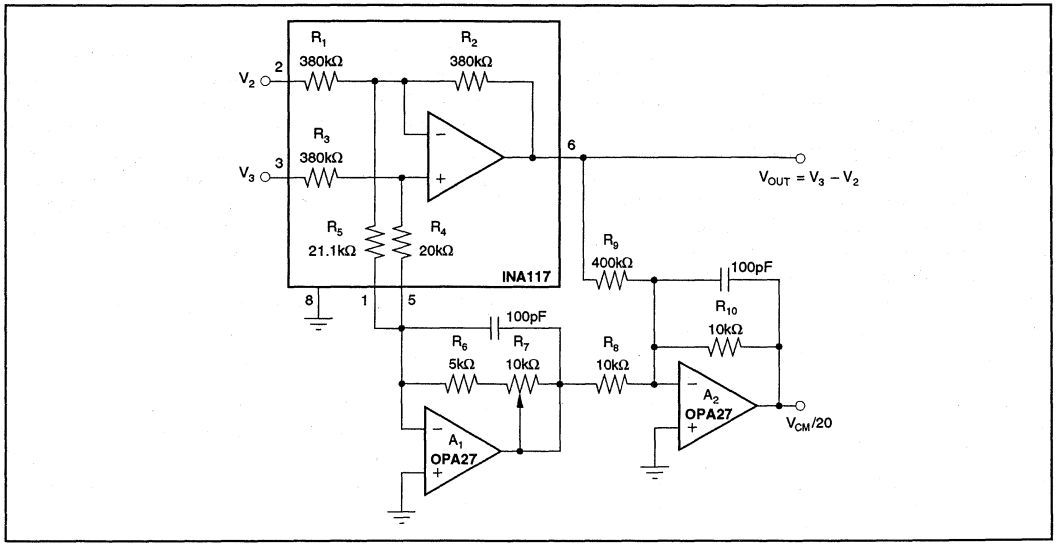


FIGURE 2. INA117 with True Common-Mode Voltage Monitor.

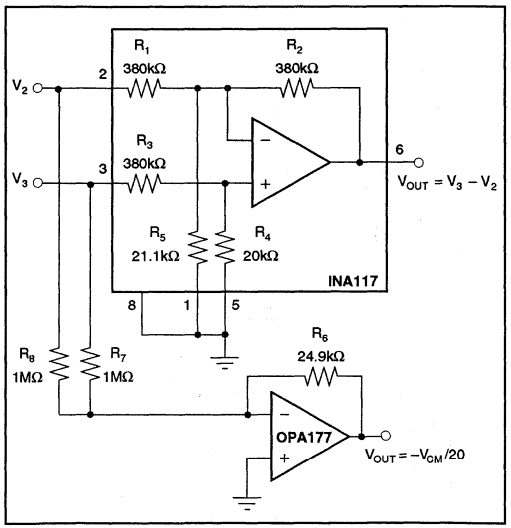


FIGURE 3. External CMV Monitor, Inverting.

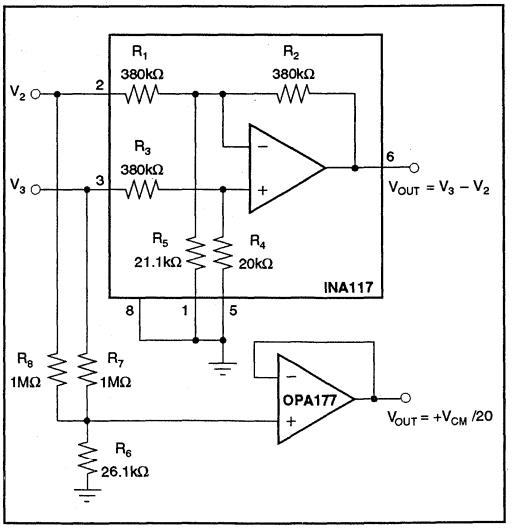


FIGURE 4. External CMV Monitor, Noninverting.

For Immediate Assistance, Contact Your Local Salesperson

BURR-BROWN®

APPLICATION BULLETIN

Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

INPUT OVERLOAD PROTECTION FOR THE RCV420 4–20MA CURRENT-LOOP RECEIVER

By R. Mark Stitt and David Kunst (602) 746-7445

Because of its immunity to noise, voltage drops, and line resistance, the 4–20mA current loop has become the standard for analog signal transmission in the process control industry. The RCV420 is the first one-chip solution for converting a 4–20mA signal into a precision 0–5V output. Although the on-chip current sensing resistor is designed to tolerate moderate overloads, it can be damaged by large overloads which can result from short circuits in the current loop. Complete input protection from short circuits to voltages of 50V or more can be afforded with the addition of the relatively simple circuitry shown in this bulletin.

The complete protected 4–20mA current loop receiver circuit is shown in Figure 1. The RCV420 is connected for a 0–5V output with a 4–20mA current sink input. For a 4–20mA current source input, connect the input to pin 3 instead of pin 1. An on-board precision +10.0V buried zener voltage reference in the RCV420 is used to offset the span (for 0V out with 4mA in) via pin 12. It can also be used for powering external circuitry such as the voltage dividers used to set the underrange/overrange comparator thresholds.

An LM193 dual voltage comparator is used to detect underrange and overrange conditions at the output of the RCV420. The LM193 is designed to operate from a single power supply with an input common-mode range to ground. In this application the LM193 is operated from a single +15V power supply for input common-mode range compatibility with the RCV420 output. The open-collector LM193 comparator outputs are connected through 10kΩ pull-up resistors to a +5V supply for compatibility with TTL and similar logic families.

The RCV420 has a gain of 0.3125V/mA and a 4mA span offset (a 4mA–20mA input produces a 0V–5V output). Under input open circuit conditions (0mA input), the output of the RCV420 goes to –1.25V. To level-shift the output up, for a minimum of 0V at the comparator inputs, it is summed with the 10.0V voltage reference through the 10kΩ, 1.27kΩ resistor network. The table below shows selected operating points for the RCV420 input/output and the comparator input.

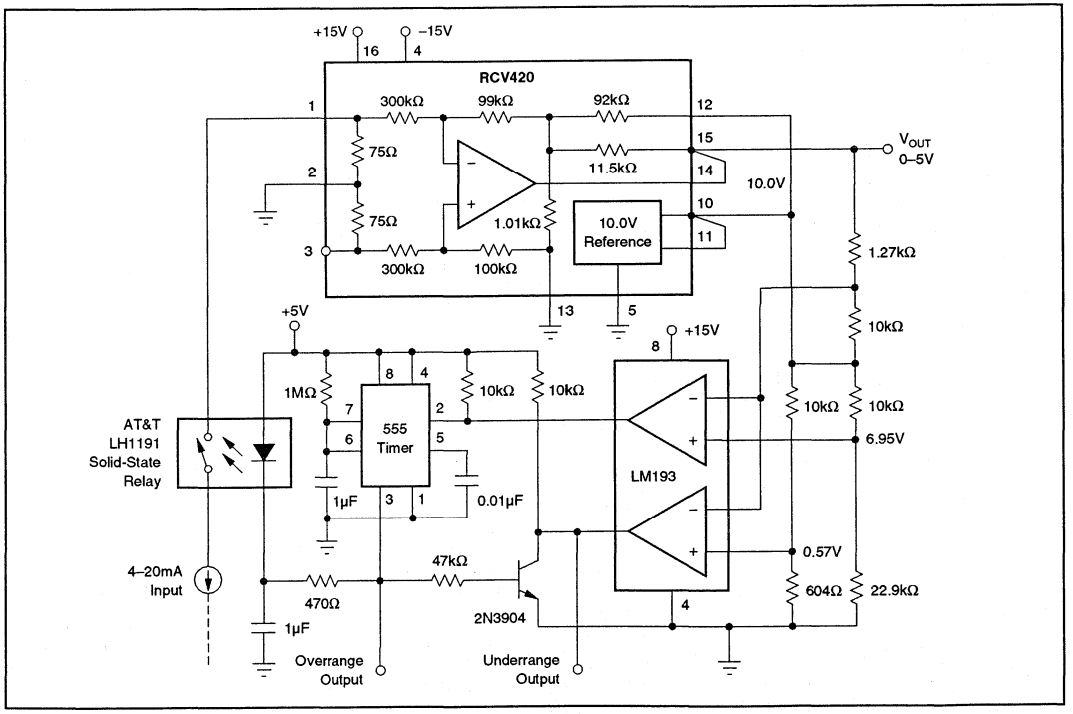


FIGURE 1. Input Protected RCV420.

SELECTED OPERATING POINTS FOR RCV420 AND COMPARATORS

RCV420 INPUT (mA)	RCV420 OUTPUT (V)	COMPARATOR INPUT (1) (V)
0	−1.250	+0.017
2	−0.625	+0.572
4	0.000	1.269
20	5.000	5.563
25	6.563	6.950
36	10.000	10.000

NOTE: (1) From the 10kΩ, 1.27kΩ summing network.

The underrange comparator threshold is set at 0.57V by the 10kΩ, 604Ω resistor divider connected to the 10.0V reference. The comparator output goes high when the input to the current loop receiver goes below 2mA. The underrange output is TTL compatible.

The overrange comparator threshold is set at 6.95V by the 10kΩ, 22.9kΩ resistor divider connected to the 10.0V reference. The output of the overrange comparator goes low when the input to the current loop receiver exceeds 25mA.
With a 36mA current loop input, the overrange comparator input is 10V. For a 36mA overload set-point, the overrange resistor divider can be eliminated by connecting the overload comparator input directly to the 10.0V reference output of the RCV420.

The overrange comparator is connected so its output will go low on overrange to trigger the ensuing active overload protection circuitry. If the overload protection circuitry is not used, the inputs to the comparator can be reversed so its output will go high on overload.

The current sense resistors within the RCV420 are rated for overloads of up to 40mA continuous and for momentary overloads of up to 0.25A with 0.1s maximum duration and 1% maximum duty cycle. Overloads within these limits will not damage or degrade the rated performance of the receiver. If the 75Ω sense resistor were shorted to 48V (a common current loop supply voltage), the overload current would be 0.64A producing an $I^2 \cdot R$ power dissipation in the resistor of 30.7W. With a package thermal resistance (θ_{JA}) of 70°C/W, this would result in a theoretical junction temperature rise in excess of 2000°C. The input resistor would fuse, destroying the device, before the package temperature actually reached 2000°C. For input short circuits up to 3V, the current is limited to a safe 40mA by the 75Ω sense resistor within the RCV420. To prevent possible damage, external means are required to protect the RCV420 sense resistors from input short circuits to potentials greater than 3V.

The least expensive input short circuit protection is a resistor connected in series with the current loop at the receiver input. Select the resistor so that the input current under short-circuit conditions will be limited to 40mA by the series combination of the protection resistor and the 75Ω current sense resistor internal to the RCV420. Short circuit protection to 48V requires a 1125Ω resistor.

$$R_{PROTECTION} = (V_S/0.040) - 75\ (\Omega)$$

The problem with using a series resistor for input overload protection is the added voltage drop in the input current loop. A 1125Ω protection resistor in series with the 75Ω internal current sense resistor would result in a 24V drop at 20mA full scale input. In most applications the additional 24V burden can not be tolerated.

Another input protection scheme which can be used when only a small series voltage drop can be tolerated is to use a 0.032A fast-acting fuse (such as Littlefuse 217000 series, type F) in series with the current loop. This fuse adds negligible voltage drop to the current loop, and blows in less than 0.1s with an overload of 128mA or more. The problem with a fuse is that it must be replaced when it blows, and the cost of maintenance can be very high.

The active protection scheme shown in this application overcomes the disadvantages of resistor and fuse protection. It uses a solid-state relay for current loop interruption. After an interrupt time delay designed to provide a safe 1% maximum overload duty-cycle, the circuit resets automatically. The LH1191 solid-state relay used has a maximum on resistance of 33Ω which adds less than 0.1V of burden to the current loop at 20mA full scale input. Low receiver burden allows longer field wiring (with higher resistance) for remote sensors, and extra compliance for "intrinsically safe" barriers or other series connected receivers.

The solid-state relay is ideal for the resetable protection task. It is inexpensive as compared to a mechanical relay (less than $1.00), and because it is solid-state, it will not "wear out" if cycled continuously. The LH1191 is a single-pole, normally open switch rated for 280V, 100mA outputs. Relay overload currents are clamped to 210mA by current limiting circuitry internal to the relay. An extended clamp condition, which increases relay temperature, results in a reduction of the internal current limit to preserve the relay's integrity.

Protection circuitry interrupt timing is provided by a 555 timer connected as a monostable multivibrator (one shot). Under normal conditions, the output of the one shot is low holding the solid-state relay on by forcing approximately 8mA through the LED as set by the series-connected 470Ω resistor. When more than 25mA flows into the current loop receiver, the overload comparator triggers the one shot. With the values shown, the one shot output goes high, turning off the LED and the solid-state relay for about one second. At the end of one second the circuit automatically resets turning the relay back on. If an overload still exists, the cycle repeats. The overload current applied to the RCV420 is limited to about 210mA by the current limit of the solid-state relay and the 75Ω sense resistor internal to the RCV420. The one second cycle time of the overload circuitry assures safe 1% maximum overload current duty-cycle. The input to the circuit can be shorted to a 50V power supply continuously without damaging or degrading the accuracy of the RCV420. A short life-test was performed on a prototype circuit. After 168 hours with the receiver input shorted to 50V, there was no detectable change in receiver accuracy within the 0.005% resolution of the test system.

Since the overload protection circuitry interrupts the current loop, a logic gate is needed to prevent a false indication of open circuit. The 2N3904 transistor is wire-ORed to the underrange comparator output, assuring it will go high only during actual underload conditions. The 1μF capacitor connected to the 470Ω relay drive resistor delays relay turn-on to prevent possible logic race conditions which could produce a false underrange output logic "sliver". The capacitor can be omitted if this is not a concern.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

BURR-BROWN® APPLICATION BULLETIN

Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

EXTENDING THE COMMON-MODE RANGE OF DIFFERENCE AMPLIFIERS

By R. Mark Stitt (602) 746-7445

Extending the common-mode range of difference amplifiers allows their use in a wider variety of reduced power-supply applications.

The INA117 has a specified common-mode input range of ±200V when operating on standard ±15V power supplies. At power-supply voltages above ±13V, the INA117 input range is limited to ±200V by the power capabilities of its internal input resistors. On reduced power supplies, the input range is limited by the common mode input range of the internal op amp.

The linear common-mode input range of the internal op amp extends to within 3V of its power supply voltage. For example, with a ±15V power supply, the common-mode input range of the internal op amp is ±12V. Because the INA117 internal resistor network divides the input by 20, the actual input range of the INA117 would be 20 • (±12V), or 240V, for ±15V power supplies. Similarly, reducing the power supply voltage to ±6V will limit the input common-mode voltage to ±60V.

There are two approaches to boosting the common-mode input range for reduced power supply applications: Offsetting the common-mode range by a fixed amount, and dynamically adjusting the common-mode range to follow the input common-mode signal.

OFFSETTING THE INPUT COMMON-MODE RANGE WITH A CONSTANT VOLTAGE

In many applications, the common-mode signal range is known and the common-mode input range of the difference amplifier can be adjusted to coincide with the required range. For example, the ±60V common-mode range of the INA117 operating on ±6V supplies could be shifted to range from +0V to +120V, or +50V to +170V.

To offset the common-mode range, the reference connection of the difference amplifier is connected to an offsetting voltage, V_X, instead of ground. With the reference connected to an offsetting potential, a second difference amplifier must be used to refer the output back to ground.

One way to offset the input voltage is to connect the reference pins 1 and 5 to the negative supply voltage as shown in Figure 1. Another possibility is to derive the offset voltage from a zener diode connected to the negative power supply as shown in Figure 2. In either case, the total common-mode range of the INA117 is unchanged and shifted by $-19 \cdot (V_X)$.

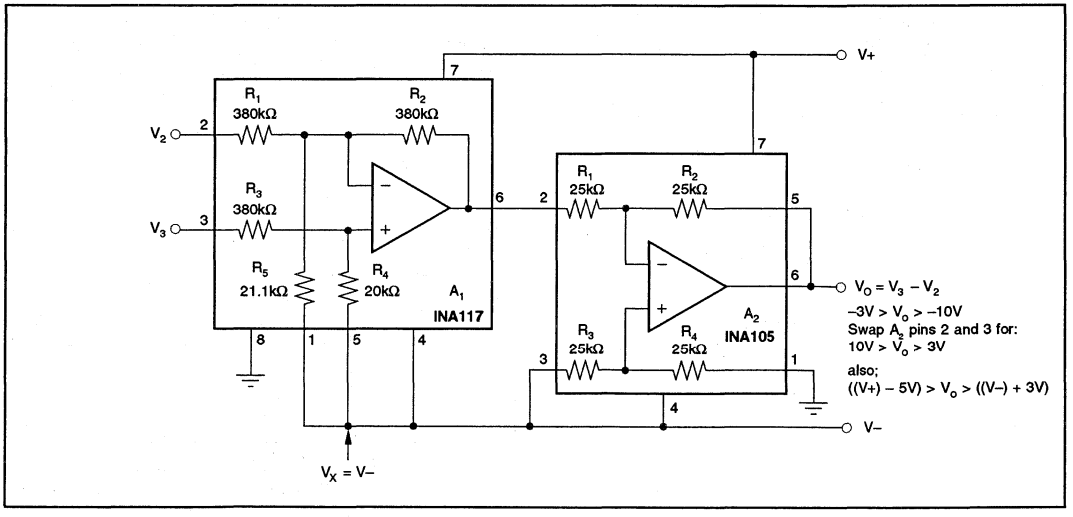


FIGURE 1. Offsetting the INA117 Common-Mode Input Range Using the Negative Power Supply as a Reference.

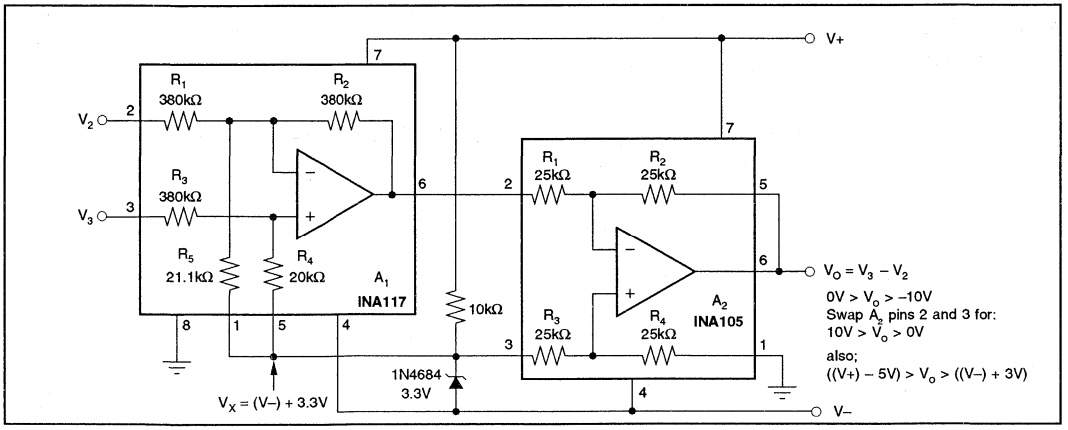


FIGURE 2. Offsetting the INA117 Common-Mode Input Range with a Zener Reference.

Since the input voltage can swing to within 3V of the power supply, the following relationships apply for the INA117:

$V_R = 20 \bullet [(V+) + |V-| - 6V]$

$V_L = 20 \bullet [(V-) + 3V] - 19 \bullet V_X$

$V_H = V_R - V_L$

Where

V_R = total common-mode range [V]

V_L = minimum common-mode signal [V]

V_H = maximum common-mode signal [V]

V+, V– = positive, negative power supply [V]

|V–| = absolute value of the negative power supply [V]

V_X = offset voltage (from ground) [V]

POWER SUPPLY	COMMON-MODE INPUT RANGE (V)		
	V_X = 0[1]	V_X = V–[2]	V_X = (V–) + 3.3[3]
±15V	–240 to +240[4]	45 to 525[4]	–18 to 462[4]
±12V	–180 to +180	48 to 408[4]	–15 to 345[4]
±9V	–120 to +120	51 to 291[4]	–12 to 228[4]
±6V	–60 to +60	54 to 174	–9 to 111

NOTES: (1) Reference connected to GND (normal operation). (2) Reference connected to V– (see Figure 1). (3) Reference connected to V– through 3.3V zener (see Figure 2). (4) Voltages greater than ±200V are shown for reference only. INA117 maximum rated operating voltage is ±200V.

TABLE I. INA117 Common-Mode Input Range for Selected Power Supplies and Reference Offsets.

The same principles can be applied to the INA105 difference amplifier as shown in Figures 3 and 4. With an allowable voltage swing to within 3V of the power supply, the following relationships apply for the INA105:

$V_R = 2 \bullet [(V+) + |V-| - 6V]$

$V_L = 2 \bullet [(V-) + 3V] - V_X$

ADJUSTING THE COMMON MODE RANGE DYNAMICALLY

Another way to boost the common-mode range of a difference amplifier is to drive the reference connection dynamically in response to changes in the input. A circuit to boost the input range of the INA117 is shown in Figure 5. A third amplifier, A_3, along with resistors R_7, R_8, and R_6 is used to derive, invert, and scale the input level presented to the reference connection.

The value for R_6 depends on the power supply voltages and op amp used for A_3. To maximize the common-mode range, R_6 should be selected so the output of A_3 is at its maximum swing limit when the inputs to the difference amplifier op amp are at 3V from the opposite power supply. The OPA1013 is a good choice for A_3 since its outputs are guaranteed to swing within 2V of the power supply rails.

Using the OPA1013 op amp for A_3, and considering the allowed swing to within 3V of the power supply voltage, the following relationships apply for the INA117.

$V_{CM} = \pm\{20 \bullet ((V+) - 3V) - 19 \bullet V_X\}$

$V_X = (V-) + 2V$

$R_6 = -0.5M\Omega \bullet V_X/V_{CM}$

Where:

V_{CM} = common-mode input range [V]

R_6 = value of R_6 [Ω]

POWER SUPPLY (V)	V_{CM} (V)	R_6 (kΩ)
±15	±487[1]	13.3
±12	±370[1]	13.7
±9	±253[1]	13.7
±6	±136	14.7

NOTES: (1) Voltages above ±200V are shown for reference only. INA117 maximum rated operating voltage is ±200V.

TABLE II. INA117 Common-Mode Input Range for Selected Power Supplies Using Figure 5 Circuit.

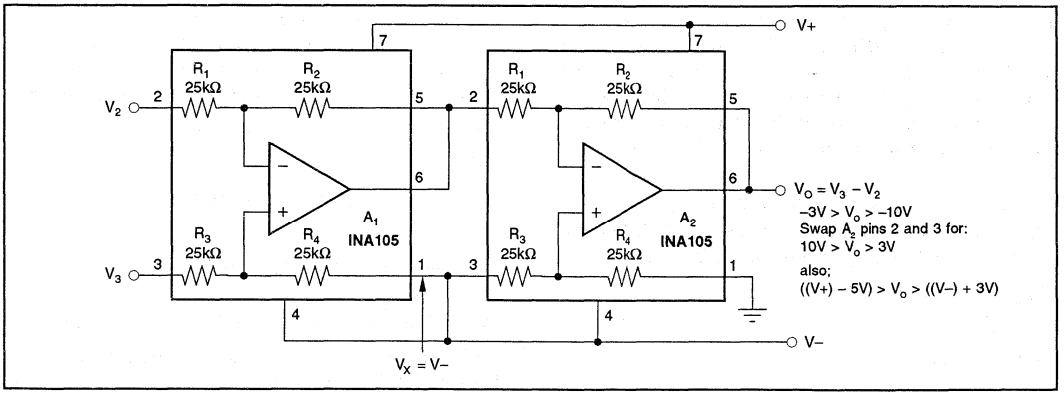


FIGURE 3. Offsetting the INA105 Common-Mode Input Range Using the Negative Power Supply as a Reference.

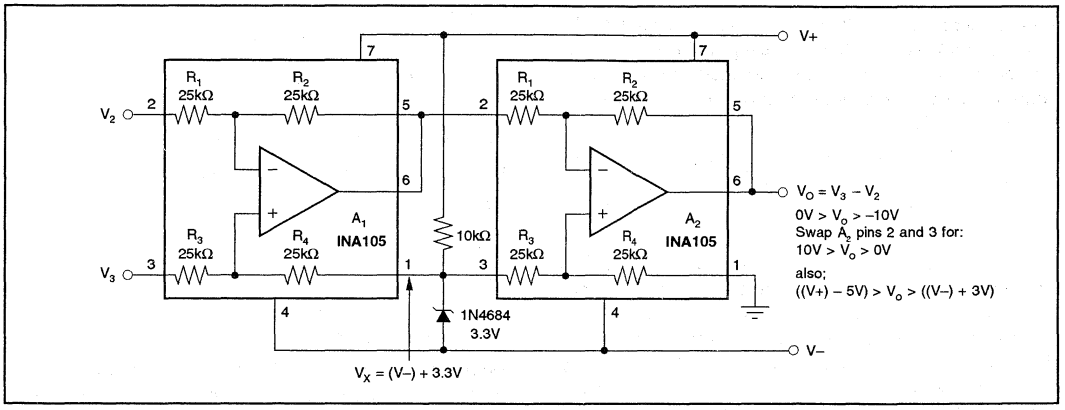


FIGURE 4. Offsetting the INA105 Common-Mode Input Range with a Zener Reference.

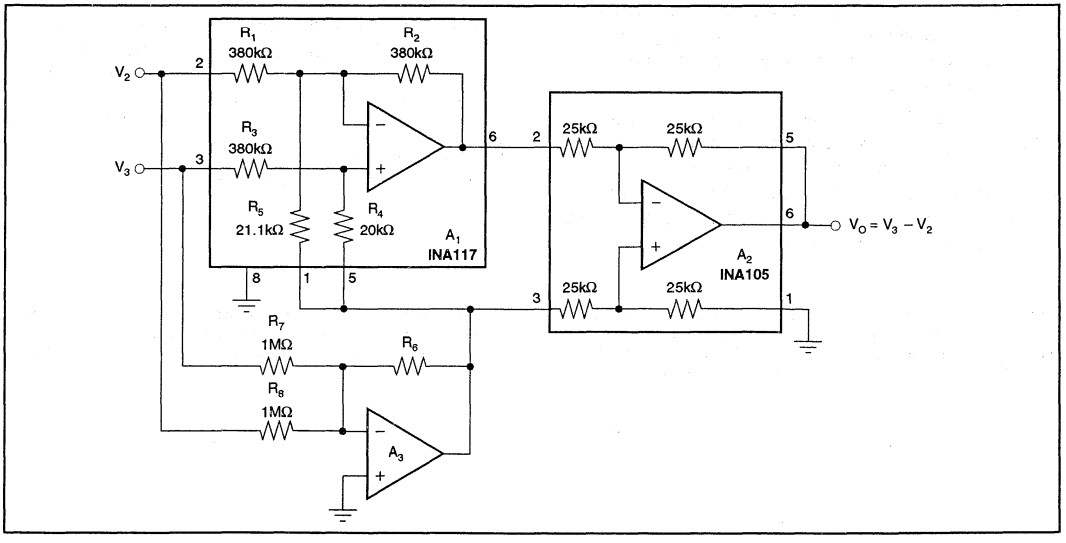


FIGURE 5. Boosting the INA117 Common-Mode Input Range Dynamically.

In the circuit of Figure 5, the true common-mode signal drives the INA117 reference, V_X. Often it is adequate to drive the reference in response to the common-mode signal at just one input pin (either pin 2 or 3). In this case one common-mode sense resistor (either R_7 or R_8) can be omitted. The value of the feedback resistor, R_6, must then be doubled.

The same principles can be applied to the INA105 difference amplifier as shown in Figure 6. Using the same 3V, 2V rules, the following relationships apply for the INA105.

$$V_{CM} = \pm\{2 \bullet ((V+) - 3V) - V_X\}$$

$$V_X = (V-) + 2V$$

$$R_6 = -0.5M\Omega \bullet V_X/V_{CM}$$

OUTPUT RANGE LIMITATIONS

Keep in mind that with any of these techniques, the common-mode range refers to the input of the difference amp only. To make use of the extended common-mode range, the output swing limitations of the difference amp must also be observed.

The output of the INA117 or INA105 is guaranteed to swing at least ±10V on ±15V power supplies. However, a negative output can actually swing to within 3V of the negative power supply (to –12V on ±15V supplies).

With zero differential input voltage to the difference amplifier, the output will be at zero volts with respect to the reference connection, V_X. The circuits in Figure 1 or 3 will not work with zero differential input. Since the difference amp reference pin is connected to V–, the output of the difference amp would saturate to its negative swing limit in an attempt to swing to V–. For the circuit to work, the differential input must be at least 3V so that the output of the difference amplifier is at 3V from V–. The input to the difference amplifier can be either +3V or –3V and the input connections (pins 2 and 3) can be interchanged to provide the

If bipolar output swing is required, offset from the rail must be large enough to accommodate the common-mode offset as well as the output swing. When using the Figure 5 or 6 circuit, the V_X terms in the equations must be replaced by:

$[(V-) + 3V + V_{SW}]$ for negative swings

and by

$[(V+) - 5V - V_{SW}]$ for positive swings

Where:

V_{SW} = difference amp output swing relative to reference, V_X.

(V_{SW} = difference amp differential input since the gain = 1)

The boosted common-mode range for positive inputs is different than for negative inputs due to the differences in the difference amplifier output swing limitations:

For positive common-mode inputs:

$$V_{CMH} = 20 \bullet ((V+) - 3V) - 19 \bullet V_{XH}$$

$$R_{6H} = -0.5M\Omega \bullet V_{XH}/V_{CMH}$$

$$V_{XH} = [(V-) + 3V + V_{SW}]$$

For negative common-mode inputs:

$$V_{CML} = 20 \bullet ((V-) + 3V) - 19 \bullet V_{XL}$$

$$R_{6L} = -0.5M\Omega \bullet V_{XL}/V_{CMH}$$

$$V_{XL} = [(V+) - 5V - V_{SW}]$$

Where:

V_{CMH} = highest common-mode input voltage [V]

V_{CML} = lowest common-mode input voltage [V]

Since only one value for R6 can be used, the smaller value must be selected if the common-mode input is bipolar. The total common-mode swing is limited by this value.

Reducing the difference amplifier output swing increases the possible common-mode input range. If a higher output swing is needed, add gain after the difference amplifier as

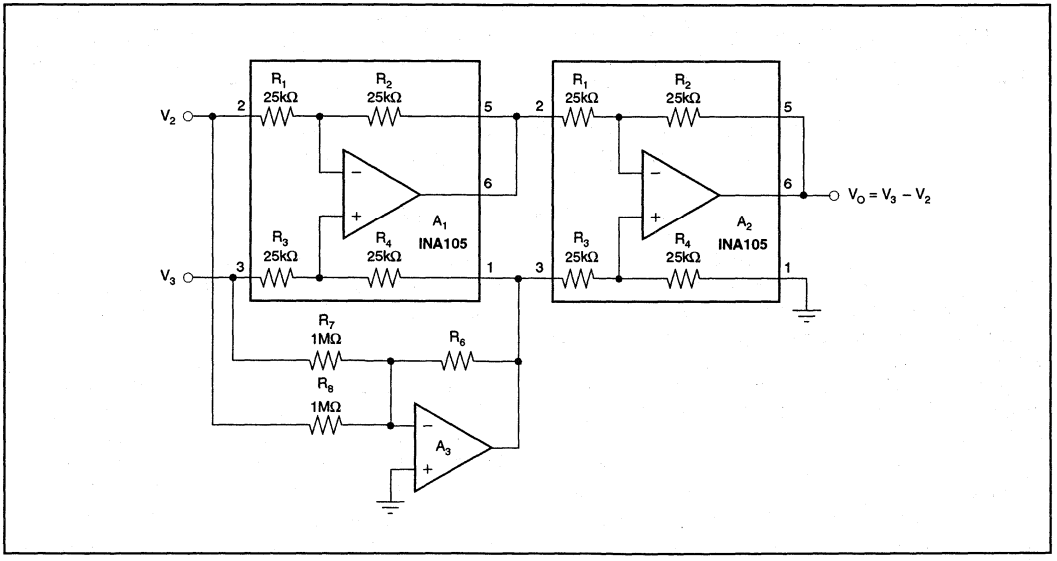


FIGURE 6. Boosting the INA105 Common-Mode Input Range Dynamically.

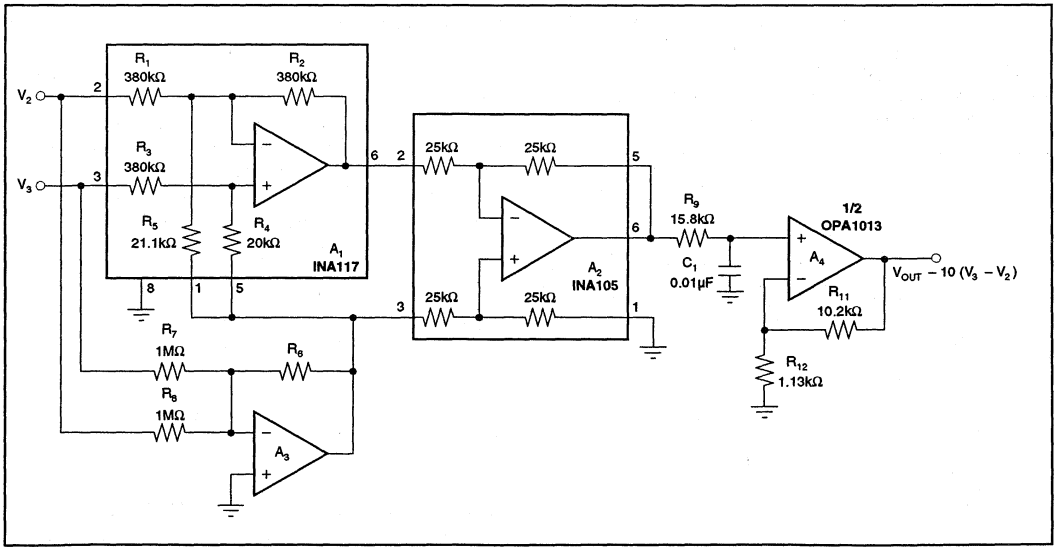


FIGURE 7. Boosted Common-Mode Input Range INA117 with Noise Filtering and Added Gain after the 2nd Difference Amplifier to Further Extend INA117 Common-Mode Input Range.

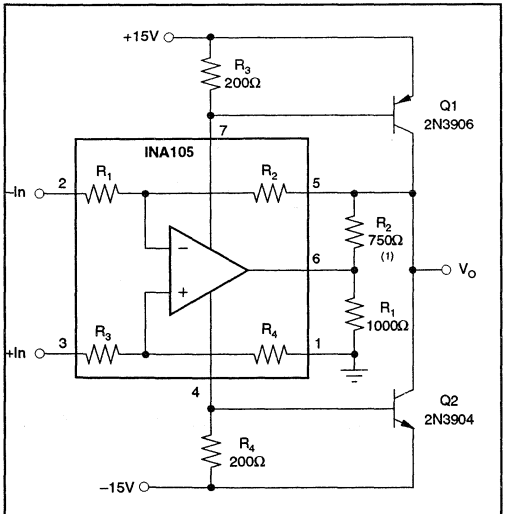
BURR-BROWN®
APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

BOOST AMPLIFIER OUTPUT SWING WITH SIMPLE MODIFICATION

By R. Mark Stitt and Rod Burt (602) 746-7445

In many applications it is desirable for the output of an amplifier to swing close to its power supply rails. Most amplifiers only guarantee an output swing of ±10V to ±12V when operating on standard ±15V power supplies. With the addition of four resistors and a pair of garden-variety transistors, the INA105 or INA106 difference amplifiers can be modified to provide nearly a full ±15V output swing on ±15V supplies.

Figure 1 shows the modified circuit for the INA105. The combined INA105 quiescent current and output current flowing from its power-supply pins drives external transistors Q_1 and Q_2 through base-emitter connected resistors R_3 and R_4. Q_1 and Q_2 are arranged as common-emitter amplifiers in a gain of approximately 1.7V/V (1 + 750Ω/1kΩ) so that the INA105's output only needs to swing about ±9V for a ±15V swing at the buffer output. Figure 4 shows the boosted INA105 driving a 1kΩ load to within a fraction of a volt of its ±15V power supplies. Figure 4 is a multiple exposure scope photo showing the composite amplifier output and the power-supply voltages.

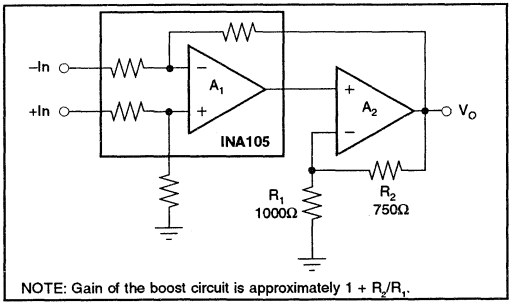


NOTES: (1) R_2 = 750Ω for INA105. R_2 = 1kΩ for INA106 on ±12V to ±18V power supplies. R_2 = 2kΩ for INA106 on ±8V to ±18V power supplies.

FIGURE 1. External Transistors Q_1 and Q_2 Add Output Boost so the Difference Amplifier Can Drive Loads Close to Its Power-Supply Rails.

Even though there is gain in the feedback of the INA105, the circuit is stable as shown by the small-signal response of the amplifier as seen in the scope photo, Figure 5. Since a unity-gain difference amplifier operates in a noise gain of two, gain can be added in its feedback loop without causing instability with the following restrictions: 1) the added gain is less than 2V/V, 2) the op amp in the difference amplifier is unity gain stable, and 3) the phase shift added by the gain buffer is low at the unity gain frequency of the op amp. All stability requirements are met when using the INA105.

To understand the details of the composite amplifier, consider the block diagram, Figure 2. Resistors R_1 and R_2 set the gain of the buffer amplifier A_2. The buffer amplifier is a current-feedback op amp formed from the output transistors in the INA105 and the external transistors, Q_1 and Q_2. The current feedback amplifier gives wide bandwidth and low phase shift. Figure 3 shows one of two complementary current-feedback amplifiers formed from the NPN output transistor in the INA105 and the external PNP transistor, Q_1. This current-feedback amplifier section is active for positive swings of the composite amplifier output. A complementary current-feedback amplifier, using external transistor Q_2, is active for negative output swings of the composite amp.



NOTE: Gain of the boost circuit is approximately 1 + R_2/R_1.

FIGURE 2. Block Diagram Showing Boost Circuit Feedback Arrangement.

Because the maximum gain in the feedback of an INA105 is limited to 2V/V, the boosted circuit works best with power supplies of ±12V or more. The INA105 doesn't have enough output swing on lower supplies to drive a gain-of-2 buffer to the power supply rails. For boosted output swing on lower supplies, consider the INA106 gain-of-10 difference amplifier. Although the op amp in the INA106 is not unity gain stable, the INA106 is stable with added gain in its feedback of up to 3V/V. This allows full output boost on lower voltage supplies. Scope photograph Figure 6 shows the boosted

INA106 driving a 1kΩ load to within a fraction of a volt on ±8V supplies. Figure 6 is a multiple exposure scope photo showing the composite amplifier output and the power-supply voltages. Scope photograph Figure 7, shows the small signal response of the INA106 with a gain-of-3 feedback buffer.

A word of caution: To obtain the boosted output swing, output protection circuitry was eliminated. There is no current limit in the output buffer. A short circuit at the output may destroy the external output transistors. Still, this simple modification is an effective means to obtain wide output swing.

So long as the stated stability requirements are observed, this technique can be applied to other op amp circuits.

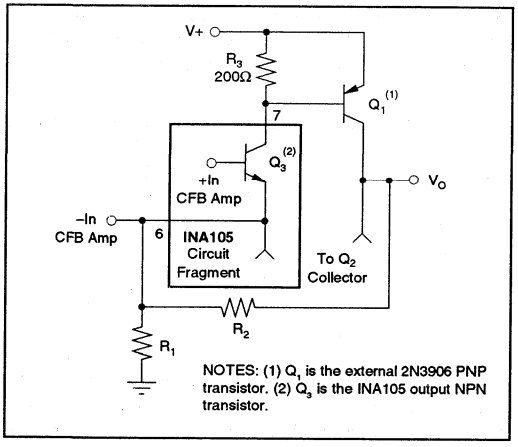


FIGURE 3. Circuit Detail Showing One-Half of the Symmetrical Current-Feedback Amplifier Output Stage, A_2 in Figure 2.

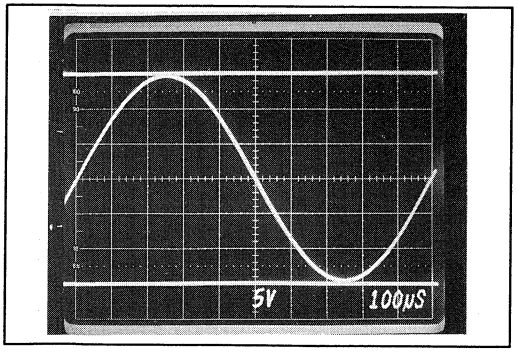


FIGURE 4. Triple Exposure Showing ±15V Power Supplies and Composite Amplifier Output Driving 1kΩ Load.

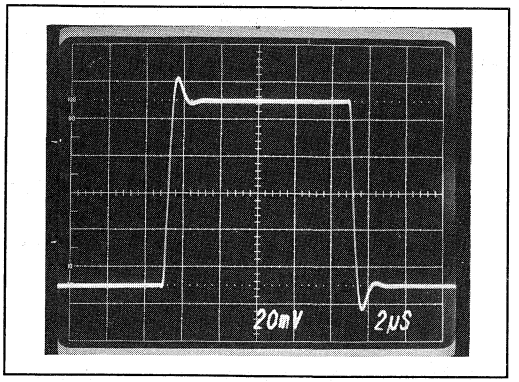


FIGURE 5. Small-Signal Response of Composite Amplifier Using INA105 and Buffer Amplifier with 750Ω, 1kΩ Feedback Resistors.

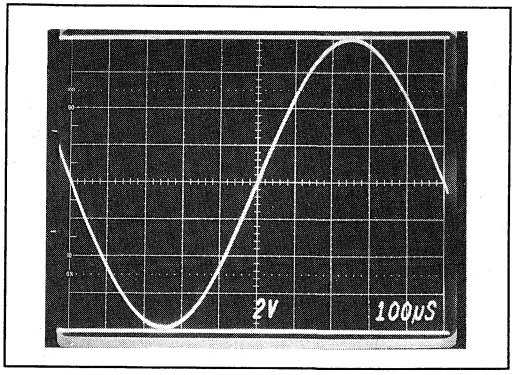


FIGURE 6. Triple Exposure Showing ±8V Power Supplies and Composite Amplifier Output Driving 1kΩ Load.

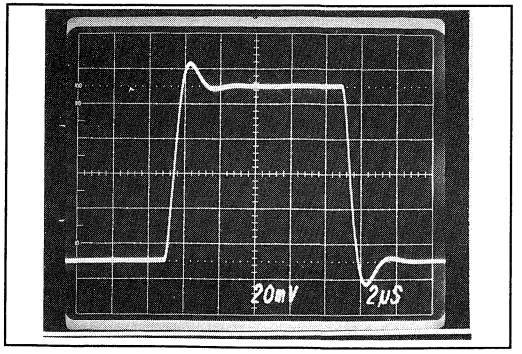


FIGURE 7. Small-Signal Response of Composite Amplifier Using INA106 and Buffer Amplifier with 3kΩ, 1kΩ Feedback Resistors.

For Immediate Assistance, Contact Your Local Salesperson

BURR-BROWN® **APPLICATION BULLETIN**

Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

0 TO 20mA RECEIVER USING RCV420

By David Kunst and R. Mark Stitt (602) 746-7445

Many industrial current-loop applications call for conversion of a 0 to 20mA input current into 0 to 5V output. The RCV420 is intended primarily as a complete solution for precise 4 to 20mA to 0 to 5V conversion. But, with the addition of one or two external 1% resistors, the RCV420 can also accurately convert a 0 to 20mA input into a 0 to 5V output.

The recommended hook-up for 0-20mA/0-5V conversion is shown in Figure 1. To reduce the gain from 5V/16mA to 5V/20mA, the internal 75Ω sense resistor is paralleled with a 301Ω, 1% external resistor connected between pins 1 and 2.

Even though the external paralleling resistor has a 1% tolerance, the worst-case gain error of the current-to-voltage conversion will be only 0.5%. This is because the parallel combination of an external 301Ω resistor and the internal 75Ω resistor is dominated by the internal resistor.

A tighter tolerance on the external paralleling resistor would not significantly improve the gain accuracy. This is because the internal 75Ω sense resistor also has a tolerance of 1%.

The high gain accuracy of the RCV420 transfer function comes from a fine laser trim of the internal amplifier's gain which compensates for any error in the 75Ω internal sense resistor. So even if the sense resistor were replaced by a resistor of exact value, the gain error could be as much as 1%.

For best common-mode rejection performance, a second 301Ω external resistor should be connected between pins 2 and 3 in parallel with the other internal 75Ω sense resistor. Without it, 86dB CMR would be degraded to about 80dB. If high CMR is not needed, the second resistor shown can be omitted.

To eliminate the offset, used for 4-20mA/0-5V conversion, the "Ref In" (pin 12) must be connected to ground instead of to the 10V reference. The "Ref Out" and "Ref Feedback" (pins 10 and 11) should still be connected together to prevent the reference circuitry from locking-up. Even though the 10.0V reference is not used for span offsetting, it is a precision reference which may be useful for other circuitry.

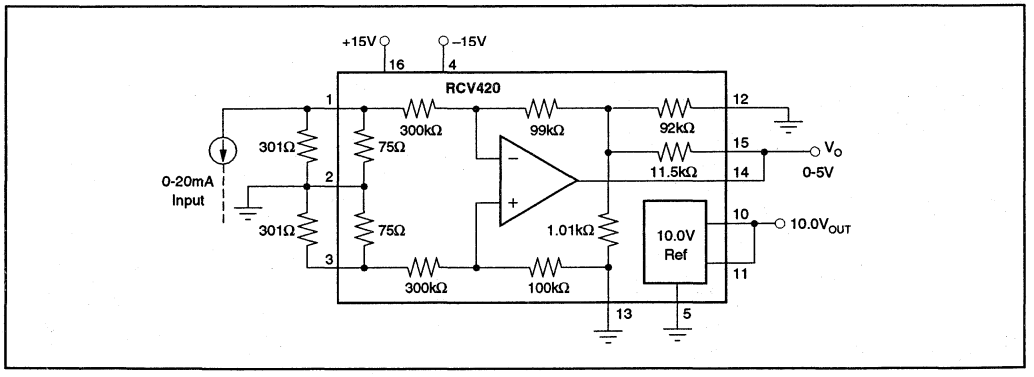


FIGURE 1. 0-20mA/0-5V Receiver Using RCV420.

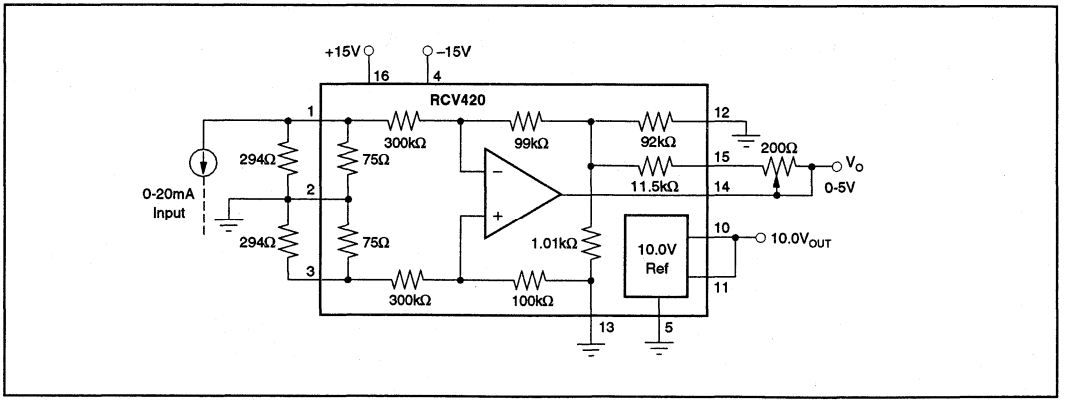


FIGURE 2. Gain Trimmable 0-20mA/0-5V Receiver Using RCV420.

If better gain accuracy is required, use the gain trim circuit shown in Figure 2. This circuit uses a slightly lower value external resistor in parallel with the internal 75Ω sense resistor and a potentiomenter in the feedback for fine trim of gain. Because of its small value, and the action of the "T" network feedback arrangement, the effect of the gain adjust pot on CMR is negligible.

Of course, any mix of input/output polarity can be obtained by connecting the current source input to either pin 1 or 3.

INPUT CURRENT	OUTPUT VOLTAGE	INPUT CONNECTION
0 to 20mA	0 to 5V	Pin 1
0 to –20mA	0 to –5V	Pin 1
0 to 20mA	0 to –5V	Pin 3
0 to –20mA	0 to 5V	Pin 3

Gain-reduction paralleling-resistors for selected gains are shown in the table below.

INPUT RANGE	OUTPUT RANGE	PARALLELING-RESISTOR
0 to 20mA	0 to 5V	301Ω
0 to 50mA	0 to 5V	35.7Ω

In general, to determine the value of the external paralleling resistor:

$$R_{EXT} = \frac{75\Omega}{\frac{I_{IN}}{16mA} - 1}$$

Where:
R_{EXT} = External paralleling resistor (Ω)
I_{IN} = Input current range (mA)

BURR-BROWN® APPLICATION BULLETIN

Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

BOOST INSTRUMENT AMP CMR WITH COMMON-MODE DRIVEN SUPPLIES

By R. Mark Stitt (602) 746-7445

Ever-increasing demands are being placed on instrumentation amplifier (IA) performance. When standard IAs can not deliver the required performance, consider this enhanced version. Dramatic performance improvements can be achieved by operating the input amplifiers of a classical three-op-amp IA from common-mode driven sub-regulated power supplies.

Instrumentation amplifiers are designed to amplify low-level differential signals while rejecting unwanted common-mode signals. One of the most important specifications is common-mode rejection (CMR)—the ability to reject common mode signals. AC CMR is especially important since the common-mode signals are inevitably dynamic—commonly ranging from 60Hz power-line interference to switching-power-supply noise at tens to hundreds of kHz. With common-mode driven sub-regulated supplies, both the AC and DC CMR of the IA can be dramatically improved. Improved AC and DC power supply noise rejection is an added bonus.

At the high gains often required, input offset voltage drift can also be a critical specification. In some applications, the low input offset voltage drift of chopper stabilized op amps might provide the best solution. But, since many of these chopper stabilized op amps are built using low voltage CMOS processes, they can not be operated on standard ±15V power supplies. Operating the chopper stabilized op amps from common-mode-driven, sub-regulated ±5V supplies allows them to be used without restriction in ±15V systems.

THE THREE OP AMP IA

To understand how the technique works, first consider the operation of the three op amp IA shown in Figure 1A. The design consists of an input gain stage driving a difference amplifier.

The difference amplifier consists of op amp A_3 and ratio matched resistors R_1 through R_4. If the resistor ratios R_2/R_1 exactly match R_4/R_3 the difference amplifier will amplify differential signals by a gain of R_2/R_1 while rejecting common-mode signals. The CMR of the difference amplifier will almost certainly be limited by resistor mismatch when a high-performance op amp is used for A_3. A unity-gain difference amplifier requires a difficult 0.01% resistor match for CMR of 86dB.

Since the slightest input source impedance mismatch would degrade the resistor matching of the difference amplifier, a differential input, differential output gain-stage (A_1, A_2, R_{FB1}, R_{FB2}, and R_G) is used ahead of the difference amplifier. The low output-impedance of the of the gain stage preserves difference amplifier resistor matching and maintains the CMR of the difference amplifier. The input amplifiers also provide high input impedance and additional gain.

When designing a high CMR instrumentation amplifier, it is important to use a differential input, differential output amplifier using a single gain-set resistor (see Figure 1A). In the Figure 1A circuit, CMR is independent of resistor matching. Resistor mismatches degrade CMR in the two gain-set-resistor differential in/out amplifier (see Figure 1B).

To understand why CMR is independent of resistor matching in the single gain-set resistor amplifier, consider the Figure 1A circuit. With a common-mode input signal, and no differential input signal, the voltage between V_N and V_P does not change. Therefore the voltage across R_G remains constant and, since no current flows in the op amp inputs, there is no current change in R_{FB1} or R_{FB2}, and the differential output voltage, V_1-V_2, does not change. Ideally then, with a perfect difference amplifier, the common-mode gain is zero and the CMRR is ∞.

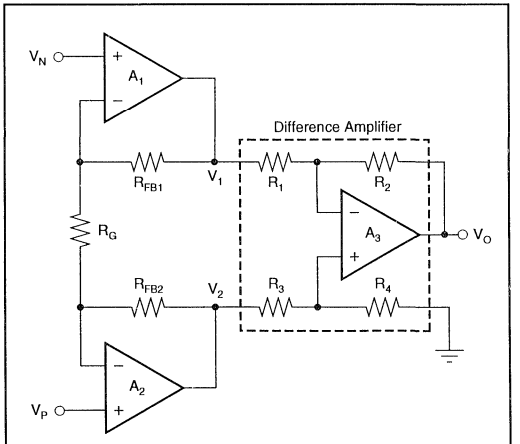


FIGURE 1A. The Three Op-Amp Instrumentation Amplifier.

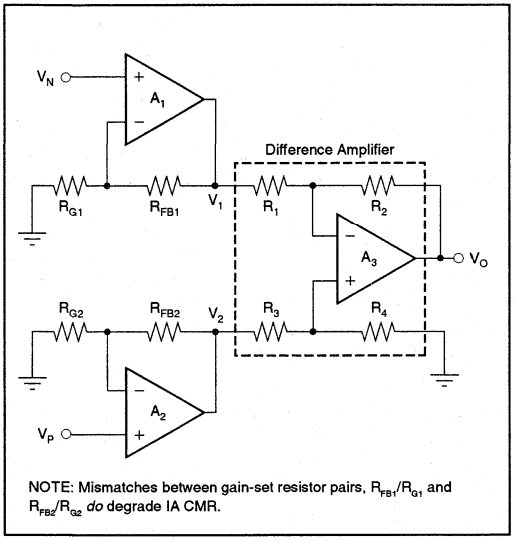


FIGURE 1B. The *Wrong* Way to Make a Three Op-Amp Instrumentation Amplifier.

In the Figure 1B circuit, CMR *does* depend on resistor matching. Common-mode signals will cause different common-mode currents to flow through R_{G1} and R_{G2} if their values are not matched. Then, if the ratio of R_{FB1}/R_{G1} is not exactly equal to the ratio of R_{FB2}/R_{G2}, there *will* be common-mode gain and the CMRR of the instrumentation amplifier *will* be degraded.

Mathematically, for the two circuits:

$$G_{DIFF} = (V_1 - V_2)/(V_N - V_P)$$
$$G_{CM} = (V_1 - V_2)/V_{CM}$$

For the single gain-set resistor circuit, Figure 1A:

$$G_{DIFF} = (R_{FB1} + R_{FB2} + R_G)/R_G$$

If $R_{FB1} = R_{FB2} = R_{FB}$, this becomes the familiar

$$G_{DIFF} = 1 + (2 \bullet R_{FB}/R_G)$$
$$G_{CM} = 0$$

For the two gain-set resistor circuit, Figure 1B:

$$G_{DIFF} = \frac{V_N \bullet (1 + (R_{FB1}/R_{G1})) - V_P \bullet (1 + (R_{FB2}/R_{G2}))}{V_N - V_P}$$

$$G_{CM} = (R_{FB1}/R_{G1}) - (R_{FB2}/R_{G2})$$

(The CMRR of the Figure 1B circuit *does* depend on buffer amplifier resistor matching.)

Where:

G_{DIFF} = Differential gain of the IA (V/V)
G_{CM} = Common-mode gain of the IA (V/V)

See Figures 1A and 1B for V_S and R_S.

Common-mode rejection ratio is the ratio of differential gain to common-mode gain. Adding gain ahead of the difference amplifier increases the CMR of the IA so long as the op amps in the gain stage have better CMR than the difference amplifier. That is why IA data sheets usually specify one CMR (e.g. 80dB) at gain = 1 and a much higher CMR at higher gains (e.g. 100dB at gain = 1000).

Most high-performance op amps have better CMR than is available from difference amplifiers. Be careful when selecting an input op amp though; the venerable "741" op amp has a minimum high-grade CMR of 80dB, and the world's most popular op amp[1], the LM324, has a min high-grade CMR of only 70dB. High performance bipolar input op amps have the best CMR. The OPA177 has a min CMR of 130dB. FET input op amps usually don't offer quite as much performance. The Burr-Brown OPA627 comes the closest with a min CMR of 106dB.

LIMITING FACTORS IN IA PERFORMANCE

The DC CMR of a standard IA can be improved by driving the power supply connections of the input op amps from sub-regulated power supplies referenced to the IA common-mode input voltage. Op amp CMR is limited by device mismatch and thermal feedback that occurs as the op amp inputs change relative to its power supplies. If the power supply rails are varied to track the common mode input signal, there is no variation of the inputs relative to the power-supply rails, errors which degrade CMR are largely eliminated, and CMR can be substantially improved.

The AC CMR of the IA is limited by the AC response of the input amplifiers. The outputs of the input amplifiers in the IA follow the common mode input signal. As the frequency of the common-mode signal increases, the loop gain of the input op amps diminishes, and CMR falls off.

For large common-mode signals, the slew rate of the input op amps can limit the ability of the IA to function altogether. This will happen when the maximum rate of change of the common-mode signal exceeds the slew rate limit of the op amp. For a sine wave, the maximum rate of change occurs at the zero crossing and can be derived as follows:

$$V = V_P \bullet \sin(2 \bullet \pi \bullet f \bullet t)$$
$$dV/dt = 2 \bullet \pi \bullet f \bullet V_P \bullet \cos(2 \bullet \pi \bullet f \bullet t)$$

At t = 0,

$$dV/dt = 2 \bullet \pi \bullet f \bullet V_P$$
$$\text{Slew rate limit} = 2 \bullet \pi \bullet f_{MAX} \bullet V_P$$

Where:

V = common-mode voltage vs time (t)
V_P = peak common-mode voltage
Slew rate limit = maximum dV/dt
f_{MAX} = maximum common-mode frequency at amplitude V_P beyond which standard IA fails to function due to slew-rate limit of input op amp.

As with DC CMR, AC CMR can be improved by driving the power supply connections of the input op amps from common-mode referenced sub-regulated supplies. Since neither the inputs nor the output of the amplifier change relative to

(1) According to its designer: Frederiksen, Thomas M., *Intuitive IC Op Amps*, National Semiconductor's Technology Series, 1984, back cover.

the power supply rails, nothing within the amplifier moves in response to the common-mode signal. No current flows in the phase compensation capacitors and the phase compensation is therefore defeated for common-mode response.

THE BOOSTED IA

The complete circuit for the enhanced IA is shown in Figure 2. In addition to the three op amp IA, it contains a buffered common-mode voltage generator, and ±5V subregulated power supplies.

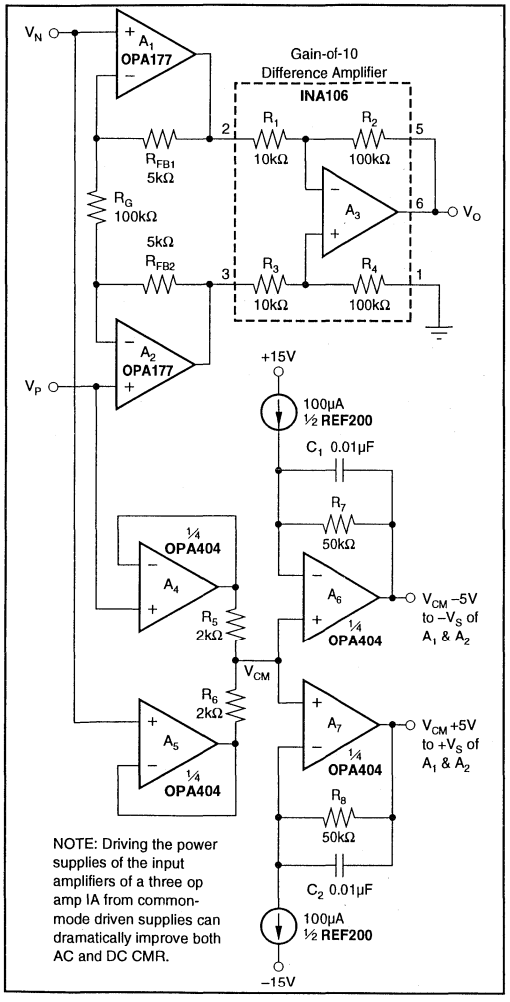


FIGURE 2. Boosted Instrumentation Amplifier.

An INA106 gain-of-10 difference amplifier is used for the difference amplifier. The INA106 contains a precision op amp and ratio matched resistors R_1 through R_4 pretrimmed for 100dB min CMR. No critical resistor matching by the user is required to build a precision IA using this approach.

The common-mode signal driving the subregulated supplies is derived from resistor divider network, R_5, R_6. The network is driven from the IA inputs through unity-gain connected op amps A_4 and A_5. These buffer amplifiers persevere the IA's high input impedance. In some applications the impedance of the R_5, R_6 network connected directly to the IA inputs is acceptable and buffer amplifiers A_4 and A_5 can be deleted as shown in Figure 3. The signal at the R_5, R_6 connection of the resistor divider is the average or common-mode voltage of the two IA inputs.

The negative subregulator consists of A_6, R_7, C_1, and a 100µA current source (1/2 of Burr-Brown REF200). Since no current flows in the op amp input, 100µA flows through the 50kΩ resistor, R_7 forcing a –5V drop from the op amp input to its output. The op amp forces the negative input to be at the same potential as its positive input. The result is a a –5V floating voltage reference relative to the op amp noninverting input terminal.

The positive subregulator is the same as the negative subregulation except for the polarity of the current source connection.

The outputs of the positive and negative subregulators are connected to the power supplies of the input op amps A_1 and A_2 only. All other op amps are connected to ±15V power supplies.

COMMON MODE RANGE OF BOOSTED IA

The common-mode input range of the boosted IA is limited by the subregulated supply voltage. The outputs of the subregulator amplifiers, A_6 and A_7 must swing the common-mode voltage plus the subregulator voltage. The smaller the subregulator voltage, the better the common-mode input range. A subregulator voltage of ±5V was chosen because it is low enough to give good input common-mode range while it is high enough to allow full performance from almost any op amp.

COMMON MODE RANGE OF BOOSTED IA IS AS GOOD AS STANDARD IA

The common-mode input range of the boosted instrumentation amplifier is as good as that of most integrated circuit IAs. It might seem that the subregulated supplies would reduce the IA's common-mode range. But because the boosted IA uses a gain-of-10 difference amplifier rather than a unity gain difference amplifier its common mode range is not limited by the input amplifiers. The common-mode input range of both the boosted IA and the standard IA is about ±7V.

That's right. With a 10V output, the common mode input range of a standard IA is only about ±7V, not ±10V as many have been incorrectly led to believe.

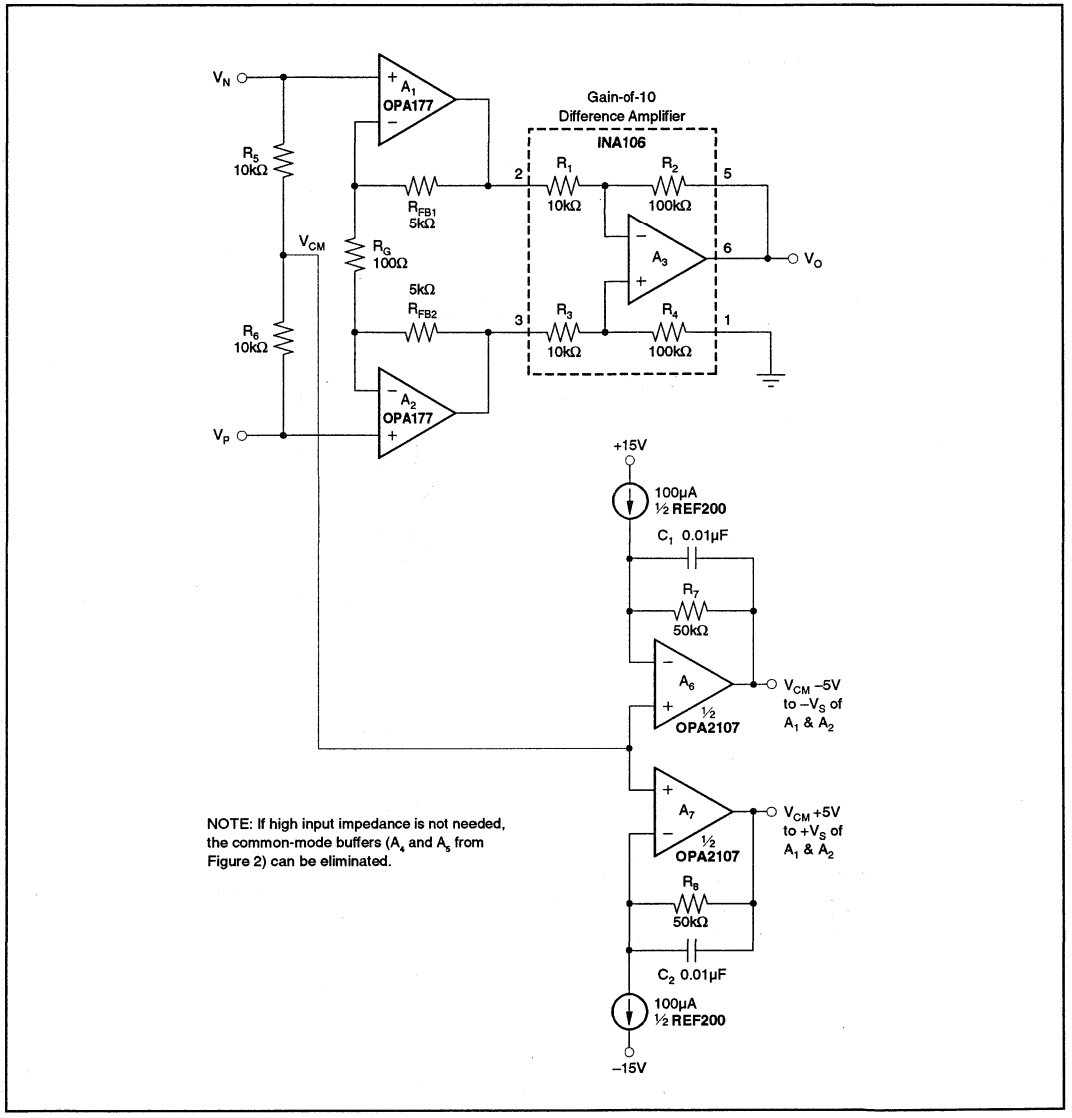


FIGURE 3. Simplified Boosted Instrumentation Amplifier.

The common-mode swing of a standard IA is limited by the output swing of the input amplifiers. The common mode range of the boosted IA is limited by the output swing of the subregulator amplifiers.

Standard IAs use unity gain difference amplifiers for practical reasons. Since standard IAs are designed for general applications, they must be adjustable to unity gain. Because it would be difficult for the user to maintain the resistor ratio matching necessary for good difference amplifier CMR, a fixed unity gain difference amplifier is provided. Gain adjustment is made with the input amplifiers, where matching is not critical for good CMR. Also, The more gain placed ahead of the difference amplifier, the better the IA CMR.

To compare the limits on input common-mode range, assume the op amps used can all swing to within 3V of their power supply rails (i.e. they can swing to ±12V when operating on ±15V power supplies).

In a standard IA, using a unity gain difference amplifier, the input amplifiers must provide a differential 10V output for a 10V IA output. With the input amplifiers in equal gains, each must deliver one half of the 10V differential signal.

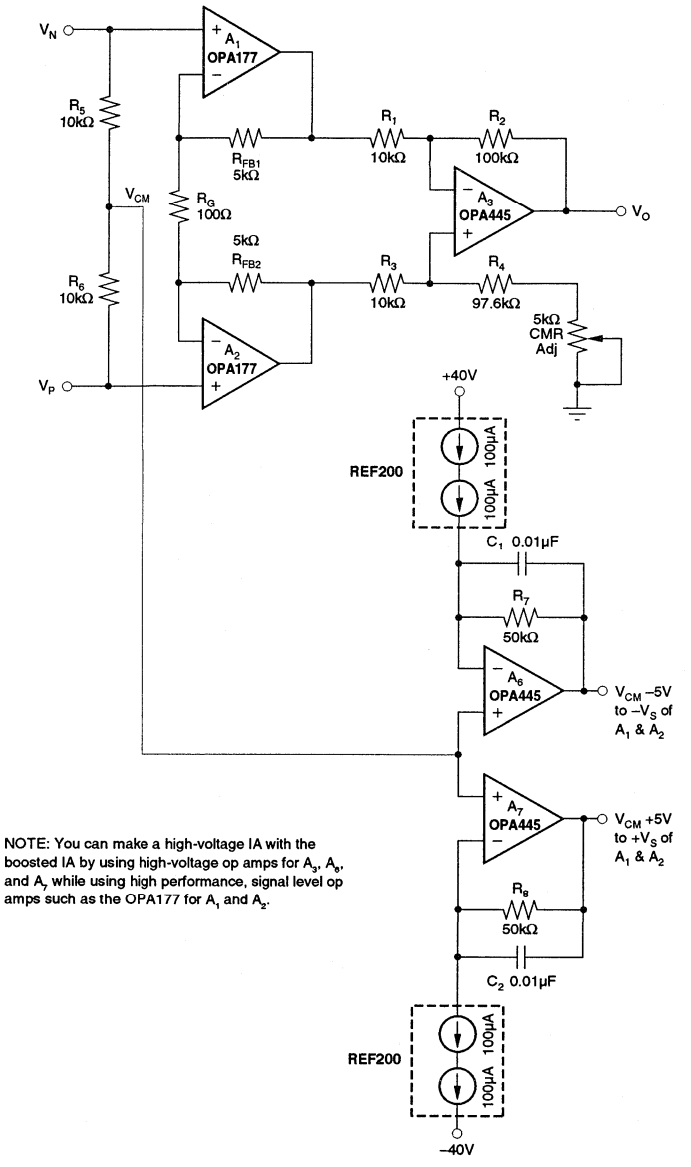
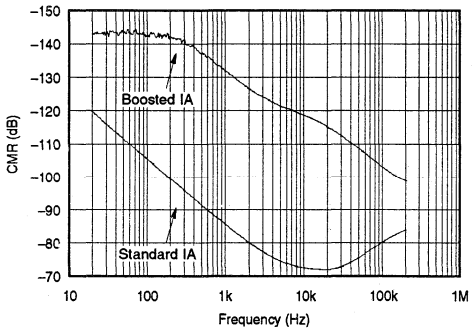


FIGURE 4. High Voltage Instrumentation Amplifier.

With a common-mode input of 7V one input amplifier must deliver 7V common-mode plus 5V differential—its 12V swing limit.

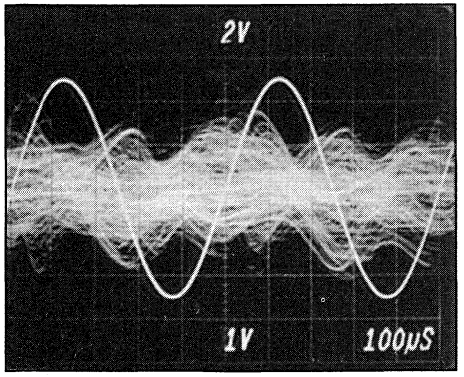
The boosted IA also has a ±7V common-mode input limit. The subregulators are set at ±5V from the input common-mode signal. With a 7V common mode input, one of the subregulator outputs is at its 12V swing limit.

In the boosted IA, using a gain-fo-10 difference amplifier, the buffer amplifiers must provide a differential output of only 1V for a 10V IA output. With the input amplifiers in equal gains, each must deliver one half of the 1V differential signal. With a common-mode input of 7V, one input amplifier must deliver 7V common-mode plus 0.5V differential for a total of 7.5V at its output which is no problem since the V_S is 12V (5V subregulated + 7V common-mode).



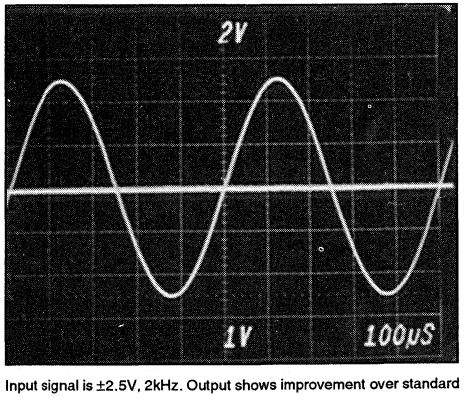
NOTE: Both the standard and boosted IA use OPA177s for input amplifiers. The overall gain of the IA is 1000V/V (input section gain = 100, difference gain = 10). The boosted IA gives more than 100/1 CMR improvement. Noise limits the DC CMR to slightly greater than 140dB referred to a +9dBm common-mode input signal.

FIGURE 5. CMR vs Frequency Comparison between Standard Three Op Amp IA and Boosted IA.



Input signal is ±2.5V, 2kHz. Output shows approximately 56dB CMR.

FIGURE 5B. Common-Mode Input and Output of Standard Gain = 1000V/V IA Using LTC1050 Chopper Stabilized Op Amp.



Input signal is ±2.5V, 2kHz. Output shows improvement over standard IA to approximately 82dB CMR.

FIGURE 5C. Common-Mode Input and Output of Boosted Gain = 1000V/V IA Using LTC1050 Chopper Stabilized Op Amp.

SUBREGULATION IMPROVES PRECISION

Lower power dissipation in the input op amps due to reduced power supplies can improve performance by reducing thermally induced low-frequency noise. In all semiconductor packages thermocouples are formed at various conductor interfaces. Matched-seal metal, side-braze ceramic, cerdip, and many plastic packages use Kovar leads. Significant thermocouples are formed between the lead plating and the Kovar. Thermocouples are also formed between the leads and the solder connections to the printed circuit.

If thermal gradients are properly matched (at the amplifier inputs) the thermocouple errors will cancel. In practice, mismatches occur. Even under laboratory conditions, the error produced can be several tenths of microvolts—well above the levels achievable with low-noise amplifiers. At the output of a high-gain amplifier, the error will appear as low frequency noise or short-term input offset error.

In signal op amp packages, much of the heat is conducted away through the leads. The resultant thermal gradient between the package and the printed circuit can be a major source of error. Air currents cool one lead more than another, resulting in mismatched thermal gradients. Operating the op amp on ±5V supplies (reduced from ±15V supplies) decreases quiescent power dissipation and associated temperature rise by three-to-one, providing a commensurate reduction in thermally induced errors.

PERFORMANCE OF BOOSTED IA vs STANDARD IA

A performance comparison between the standard IA and the boosted IA in Figure 2 is shown in Figure 5. Amplifiers used for A_1 and A_2 are OPA177; A_3 is an INA106 gain-of-10 difference amplifier; and A_4 to A_7 are an OPA404 quad op amp in the boosted circuit. Overall gain of the IA is set at 1000V/V. The OPA177 is an improved version of the industry standard OP 07. It offers 10µV max V_{OS} and 0.1µV/°C max V_{OS}/dT. The OPA404 is used for speed and bias current. The FET inputs of the OPA404 do not add loading at the input of the IA. The speed is high as compared to the OPA177 giving a good improvement of CMR vs Frequency. The CMR plots were made using an HP4194A gain-phase analyzer with an input signal to the IA of +9dBm. As you can see, CMR vs Frequency is boosted dramatically. At 2kHz, for example, the CMR of the standard IA is ≈ 80dB while the CMR of the boosted IA is more than 120dB—more than a 100-to-1 improvement!

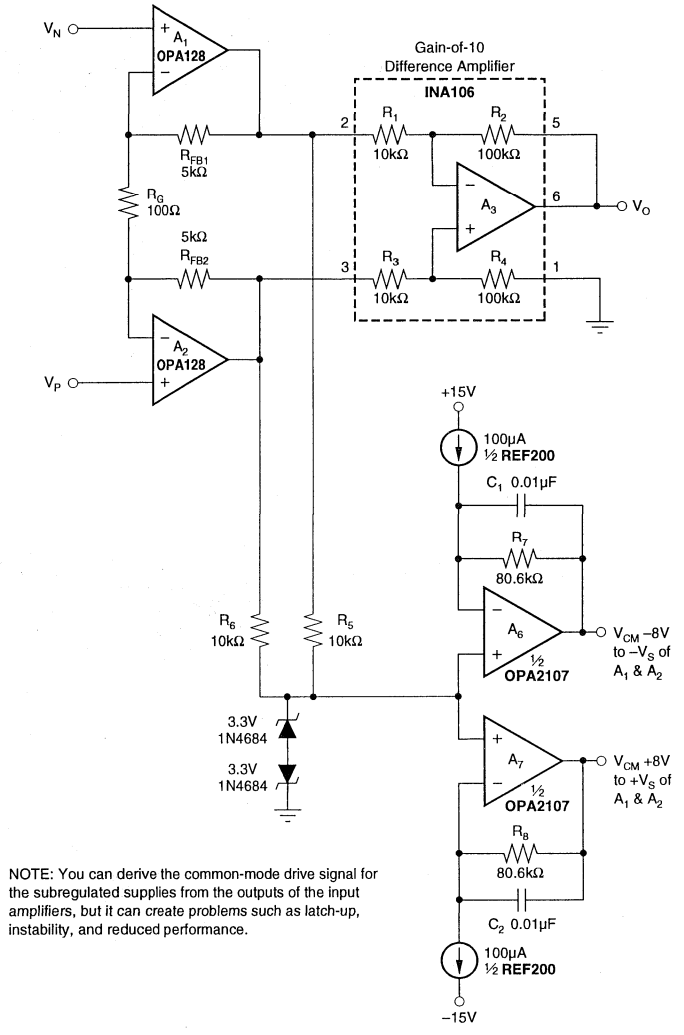


FIGURE 6. Boosted Electrometer Instrumentation Amplifier.

Another dramatic comparison is shown in the scope photos of the same IAs using LTC1050 chopper stabilized op amps for A_1 and A_2. When V_{OS}/dT is critical, chopper stabilized op amps may be the best choice—they offer 5µV max V_{OS} over temperature. As you can see, with a ±2.5V, 2kHz input signal, CMR is limited to ≈56dB by chopper noise. With the boosted circuit, CMR is a respectable ≈82dB.

The limit for CMR performance in the boosted IA is the difference amplifier. The more gain added ahead of the difference amplifier, the better the potential for improvement. For example, with a gain of 100V/V ahead of the difference amplifier an improvement in CMR of 40dB is possible. The actual performance boost will depend on matching and parasitics in the devices selected.

Of course, CMR vs Frequency depends on the dynamic performance of all amplifiers. Improvement in dynamic CMR will be most dramatic when the speed of the amplifiers used for A_4 to A_7 is much higher than the speed of A_1 and A_2.

HIGH-VOLTAGE IA

High voltage IAs can also be easily implemented using the boosted IA configuration. Standard precision signal level op amps can be used for the input amplifiers while the HV chores are taken care of by the other (less critical) op amps.

The simple modifications to the Figure 3 circuit are shown in Figure 4. OPA445 op amps are used for A_6 and A_7 and for the difference amplifier, A_3. To boost the voltage rating of the current sources used in the subregulated supplies, two REF200 current source sections are placed in series. If 1% resistors are used for difference resistors R_1-R_4, a pot may be required to adjust CMR as shown. The resulting IA will provide outstanding performance on power supplies up to ±45V.

BOOSTED ELECTROMETER IA

Electrometer amps depend on the lowest possible input bias current. Connecting the input drive circuitry to the IA inputs as shown in Figure 2 may result in too much bias current. In this case you may want to take the common-mode drive signal from the outputs of the input stage as shown in Figure 6.

Taking the common-mode drive from the outputs of the input stage may seem like a good idea, but it creates problems—latch-up, instability, and reduced performance.

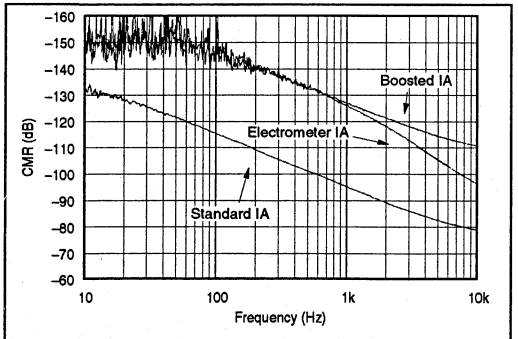
Driving the supplies of the input amplifiers from their outputs can cause latch-up. Many amplifiers exhibit input phase anomalies when their inputs are overloaded or overdriven relative to their power supplies. Unless precautions are taken when deriving the power supplies from the amplifier outputs, these anomalies will result in latch-up conditions. The back-to-back 3.3V zener diodes connected to the common-mode node (where R_5 and R_6 connect) prevents latch-up by keeping the common-mode drive point within 4V of ground. Also, the common-mode driven supplies are increased from 5V to 8V. In combination, this keeps 4V minimum on the power supplies of the input amps eliminating the latch-up condition when using the op amps shown.

The disadvantage of the clamp circuitry is reduced common-mode input range. The input common-mode range is limited to the clamp voltage of approximately 4V.

Driving the supplies of the input amplifiers from their outputs can also cause insatiably. Driving an op amp's power supply pins from the op amp output can cancel the op amp phase compensation and cause the op amp to oscillate. Driving the input op amps power supplies through the two-to-one R_5, R_6 divider does not completely cancel the compensation, but it does reduce amplifier phase margin significantly. Phase shift through A_6 and A_7 further reduces phase margin.

You might think that significantly reduced phase margin would be acceptable if the input amplifiers are used in high gain. But high gain in the differential input/output amplifier depends on virtual grounds at both ends of R_G. At the unity gain frequency of the op amp, where instability occurs, loop gain disappears and the op amps no longer approximate the ideal. At best, the op amps operate in a noise gain of two—the op amps must be stable in a gain of two. That's why you can get in trouble trying to use decompensated op amps in the front-end of an IA.

Using the faster OPA2107 for A_6 and A_7 along with the OPA128 electrometer op amp for A_1 and A_2 results in good stability. The improvement of CMR is shown in the CMR vs Frequency plot, Figure 7. The plot compares a standard IA (using the OPA128 and an INA106) to the Figure 2 and Figure 6 boosted IA circuits. The boosted circuits give a 30dB (better than 30/1) improvement in CMR up to about 1kHz. Beyond 1kHz, the CMR vs Frequency of the Figure 6 circuit begins to fall-off. At 10kHz, the Figure 6 circuit only offers about a six-to-one improvement.

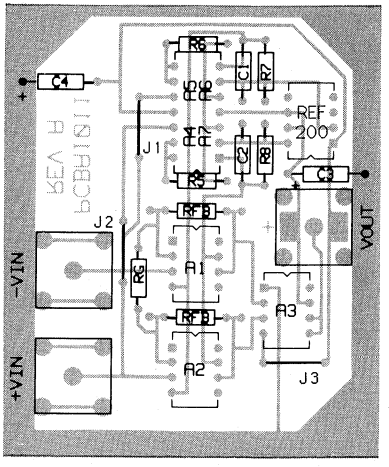


NOTE: The boosted electrometer IA circuit adds CMR boost, but the boost starts to fall off beyond about 1kHz.

FIGURE 7. CMR vs Frequency Comparison between Standard Three Op Amp IA, Boosted IA, and Boosted Electrometer IA.

LAYOUT

To get the best performance from the boosted IA, use a good printed circuit layout. For best CMR, keep the signal-path circuitry symmetrical. A printed circuit layout of the complete boosted IA circuit, Figure 2, is shown in Figure 8. It produced the excellent results shown in this bulletin. Notice that good signal-path symmetry is achieved even though a single-sided layout is used.



Best performance depends on signal-path symmetry. Notice that excellent symmetry can be maintained even with single-sided board layout. Extra pads at RFB allow *stacking* of feedback capacitors.

FIGURE 8. Printed Circuit Layout of Figure 2 Boosted IA.

BURR-BROWN® APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

INPUT FILTERING THE INA117 ±200V DIFFERENCE AMPLIFIER

By R. Mark Stitt (602) 746-7445

Many customers have asked how to add input filtering to the INA117. Since the INA117 is rated for ±200V input voltage (±500V without damage), it is commonly used in environments with very high input noise or with high-voltage input transients. This bulletin shows how to connect input filters, discusses the errors they can add, and shows how to eliminate the errors.

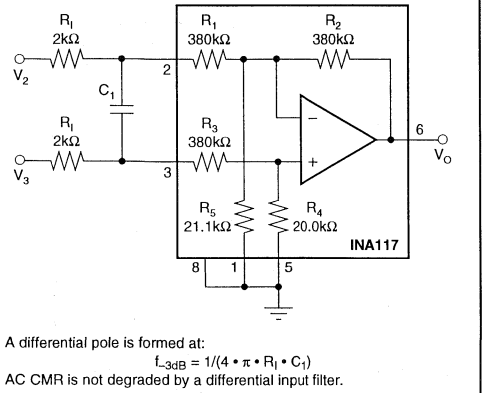
Figure 1 shows the connection of a differential input filter. A pole is formed by C_1 and the two external input resistors. $f_{-3dB} = 1/(4 \bullet \pi \bullet R_I \bullet C_1)$. Differential input filtering is preferred because mismatches in filter components do not degrade CMR.

DON'T USE COMMON-MODE INPUT FILTERS ALONE

Don't be tempted to use common-mode input filtering alone (Figure 2) unless you are prepared to carefully match components. Mismatches between the $R_I \bullet C_2$ time constants reduce AC CMR. The mismatches result in a differential input signal in response to AC common-mode inputs. Even if you successfully match the components for good AC CMR at room temperature, maintaining the match over temperature can be a problem.

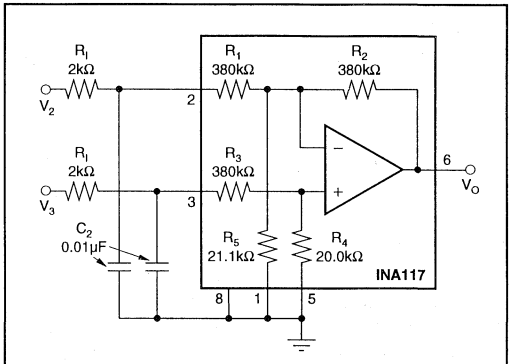
A COMBINATION COMMON-MODE AND DIFFERENTIAL INPUT FILTER IS OK

If you want common-mode input filtering, use it in conjunction with differential input filtering as shown in Figure 3. If



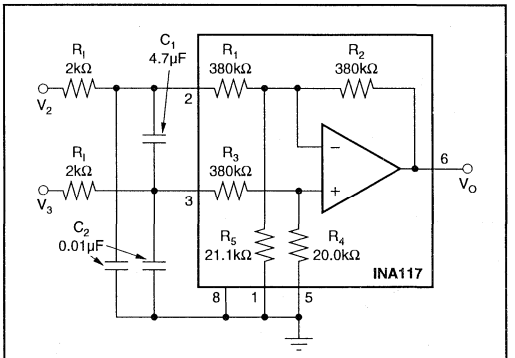
A differential pole is formed at:
$f_{-3dB} = 1/(4 \bullet \pi \bullet R_I \bullet C_1)$
AC CMR is not degraded by a differential input filter.

FIGURE 1. INA117 with Differential Input Filter.



Don't use this common-mode input filter alone. AC CMR will be degraded by mismatches in the filter time constants.

FIGURE 2. INA117 with Common-Mode Input Filter.



If $C_1 >> C_2$, AC common-mode errors due to $R_I \bullet C_2$ mismatches will be shunted by C_1, improving AC CMR.

FIGURE 3. INA117 with a Combination Differential and Common-Mode Input Filter.

$C_1 >> C_2$, AC common-mode errors will be shunted by C_1 so AC CMR can be successfully boosted. A value of $C_1 = 500 \bullet C_2$ is suggested.

Figure 4 shows actual CMR vs Frequency performance plots for the Figure 2 and Figure 3 circuits. Standard INA117 performance is shown for comparison. The standard INA117 has about 60dB CMR at 30kHz. Mismatches of 5% in R • C time constants (5% C_2 mismatch) cause the Figure 2 circuit CMR to drop below 60dB at less than 200Hz. Adding a

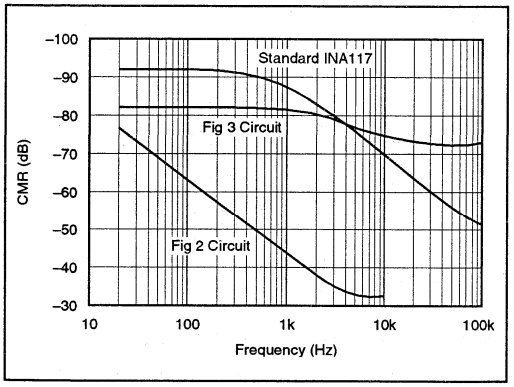


FIGURE 4. CMR vs Frequency Plots for Figure 2 and 3 Circuits with Standard INA117 for Comparison.

4.7µF differential input filter capacitor shunts out common-mode filter errors producing greater than 70dB CMR to 100kHz as shown in the plot of Figure 3's performance.

INPUT RESISTORS CAN REDUCE DC CMR

Notice that the DC CMR of the Figure 3 circuit is reduced from ≈92dB to ≈82dB. The CMR reduction is due to mismatches from input filter resistors, R_I.

CMR in the INA117 depends on close resistor ratio matching. For errors in R_1 and R_3:

$$CMR = -20\ Log(\%/105)$$

Where:
CMR = CMR for errors in R_1 or R_3 [dB]
% = the error in R_1 or R_3 [%]

The number, 105, in the denominator comes from R_1, R_3 sensitivity equations.

$$S^{CMR}_{R_1,R_3} = \pm R_I/(R_1 + R_4)$$

For example, % = 0.002% is required for the typical 94dB INA117 CMR.

Even though the 2kΩ input resistors are relatively small compared to the 380kΩ input resistors in the INA117, mismatches will reduce CMR. Even if perfectly matched external input resistors are used there can still be problems with CMR.

Although some resistor ratios in the INA117 are carefully matched to achieve good CMR, the R_I/R_3 ratio is not. A typical mismatch of 1% can be expected. The effect is to add an effective 1% mismatch to external resistors. The following worst-case CMR can be expected:

$$CMR = -20\ Log((ERROR_1 + ERROR_2)/105)$$

Where:
$ERROR_1$ = Error due R_I, R_1, and R_3 mismatches [%]
$ERROR_1 = R_I \bullet (T_{OL} + 1)/(R_I + 3.8 \bullet 10^5)$
R_I = DC resistance of external filter resistor, R_I, [Ω]
T_{OL} = Tolerance of R_I [%], i.e. 1.0 for 1%
$ERROR_2$ = Initial INA117 error [%]—See Table I

INA117 GRADE	CMR_{117} (dB)	$ERROR_2$ (%)
INA117BM typ	94	0.002
INA117BM min	86	0.005
INA117KP min	70	0.033

TABLE I. Initial INA117 CMR Values.

R_I (Ω)	$ERROR_1$ (%)	$ERROR_2$ (%)	CMR (dB)
1k	0.005	0.005	80
2k	0.010	0.005	76
5k	0.026	0.005	71
10k	0.051	0.005	65

TABLE II. Examples of Worst-Case CMR to be Expected (INA117BM and selected 1% R_Is).

Also,

$$ERROR_2 = \frac{105}{10(CMR_{117}/20)}$$

CMR_{117} = Initial INA117 CMR [dB]

See Tables I and II for examples.

CMR TRIM

If you want to use 10kΩ input resistors and must be assured of good DC CMR, you can use the trim circuit shown in Figure 5. Resistor TCR mismatches can limit difference amplifier performance over temperature. Use high quality film resistors and keep $R_I \leq 10k\Omega$ for good performance over temperature.

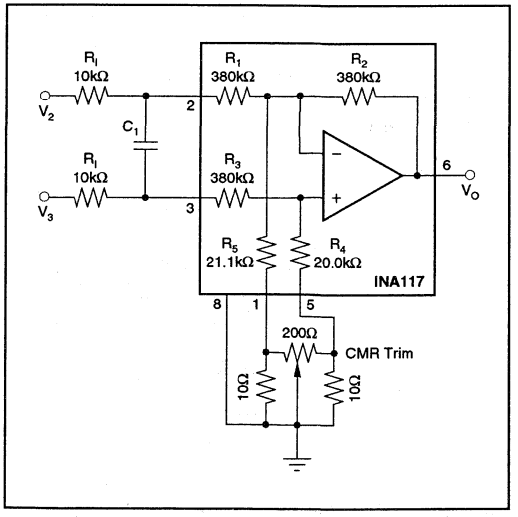


FIGURE 5. INA117 with Differential Input Filter and CMR Trim.

ADDED INPUT RESISTORS CAUSE GAIN ERROR

Adding input resistors to the INA117 causes gain error. When all resistor ratios are properly adjusted for good CMR, INA117 gain is R_2/R_1. When input filter resistors are added, gain is reduced to $R_2/(R_I + R_1)$. With $R_I = 10k\Omega$, gain is ≈ 0.974 V/V (approximately –2.6% gain error). Since gain does not depend on R_3, R_4, or R_5, the gain error can not be corrected by adding resistance in series with any pin.

CORRECTING GAIN ERROR

To correct for the gain error introduced by the input filter resistors, you can add a small amount of positive feedback as shown in Figure 6. Resistors R_{4A}, R_{4B}, and R_{5A} must be selected to maintain CMR and to give the proper positive feedback to correct for gain error.

The following procedure is suggested:

Set $\boxed{R_{4A} = 10\Omega}$

This is an arbitrary but adequate value for R_{4A}. It is the smallest standard 1% value. With this small value, even a 5% ratio matching error between R_{4A} and R_{5A} would only degrade INA117 CMR to 82.5dB. In practice, ratio errors will be lower than this when closest standard 1% resistors are used.

Calculate R_{4B} and R_{5A} and use closest standard 1% resistor value.

$$R_{4B} \approx 18 \bullet R_{4A} + \frac{19 \bullet R_2 \bullet R_{4A}}{R_I}$$

With $R_I < 10k\Omega$ and $R_{4A} = 10\Omega$ this is an adequate approximation for all practical purposes.

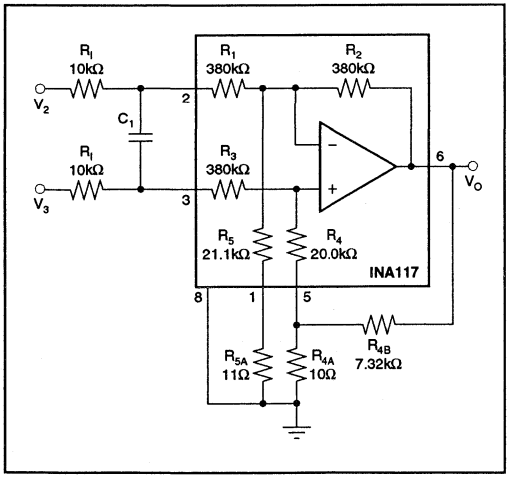


FIGURE 6. INA117 with Differential Input Filter and Positive Feedback Circuit to Compensate for Gain Error Due to R_I.

If $R_2 = 380k\Omega$, $R_I = 10k\Omega$, and $R_{4A} = 10\Omega$:

$$R_{4B} \approx 180 + \frac{72M\Omega}{R_I} \quad \boxed{\approx 7.4k\Omega}, \text{ use } 7.32k\Omega$$

$$R_{5A} \approx \frac{361 \bullet R_2 \bullet R_{4A} \bullet R_{4B}}{324(R_2 \bullet R_{4A}) + 324(R_2 \bullet R_{4B}) - 342(R_{4A} \bullet R_{4B})}$$

With $R_2 = 380k\Omega$ and $R_{4A} = 10\Omega$:

$$R_{5A} \approx \frac{3.61 \bullet R_{4B}}{3.24 + 0.323991 \bullet R_{4B}}$$

With $R_{4B} = 7.4k\Omega$, $\boxed{R_{5A} = 11.13\Omega}$, use 11Ω.

FINE-TRIM FOR ZERO GAIN ERROR

You must trim to get zero gain error. The resistors in the INA117 are accurately ratio trimmed to give excellent CMR and gain accuracy, but their absolute values are only accurate to within about ±20%. With the values calculated above, gain error will be reduced from approximately –2.6% to about ±0.5%.

For lower gain error use the gain-trim circuit shown in Figure 7. The circuit is the same as in Figure 6 except, R_{4B} is replaced with a 5kΩ fixed resistor and a 5kΩ pot.

To trim for zero gain error, ground the INA117 inputs (0V input) and measure the offset voltage, V_{OFF}, at the output. Apply a known input voltage, V_{REF}, (e.g. 10.0V) to the INA117 noninverting input. Measure V_{REF} so you know its precise value. Adjust the 5kΩ pot for the correct INA117 output voltage: $V_{OUT} = V_{REF} + V_{OFF}$.

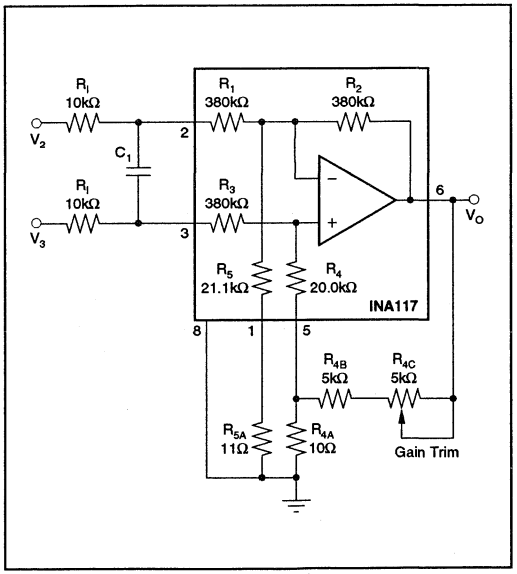


FIGURE 7. INA117 with Differential Input Filter and Gain Trim Circuit.

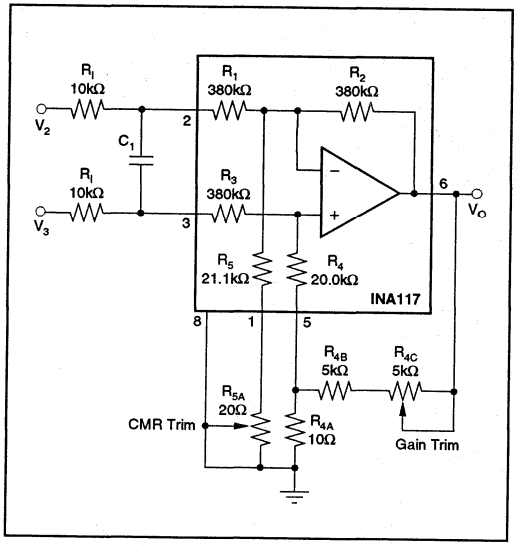


FIGURE 8. INA117 with Differential Input Filter and Both Gain Trim and CMR Trim Circuits.

You can automate the trim process by using an amplifier with a known gain of 1V/V. The Burr-Brown INA105BM difference amplifier with gain error = ±0.01% max is a good choice. Instead of using a voltage reference, drive the input of the INA117 with a ±5V, 10Hz sine or triangle wave (see AN-165, Fig. 46 for a suitable triangle generator circuit). Connect one input of the INA105 to the driven INA117 input. Connect the other input of the INA105 to the INA117 output. Adjust the 5kΩ gain trim pot for zero AC at the INA105 output. Using the AC technique allows you to distinguish between offset and gain error.

If you want to adjust both gain and CMR, use the circuit shown in Figure 8.

BURR-BROWN® APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

IC BUILDING BLOCKS FORM COMPLETE ISOLATED 4-20mA CURRENT-LOOP SYSTEMS

By R. Mark Stitt and David Kunst (602) 746-7445

Current loops have become the standard for signal transmission in the process control industry. Current loops are insensitive to noise and are immune to errors from line impedance. Adding isolation to the 4-20mA current loop protects system electronics from electrical noise and transients. It also allows transducers to be electrically separated by hundreds of volts. Burr-Brown now offers all of the integrated circuit building blocks needed to assemble complete isolated 4-20mA current-loop systems. The product line includes two-wire transmitters, two-wire receivers, low cost isolation amplifiers, and low cost isolation power supplies. Three two-wire transmitters are available: one is general purpose, one designed for use with RTD temperature sensors, and one designed for use with bridge circuits.

THE BASIC ISOLATED 4-20mA TWO-WIRE SYSTEM

Figure 1 shows a typical isolated 4-20mA system. An XTR101 converts a position sensor output into a two-wire 4-20mA current-loop signal. An ISO122 low-cost isolation amplifier isolates the 0-5V signal. Power (±15V for the RCV420, 30V for the current loop) is supplied by the HPR117 low-cost DC/DC converter.

In this example, a Penny & Giles Model HLP 190 50mm linear potentiometer is used as the position transducer. One of the 1mA current sources in the XTR101 is used to bias the transducer. A 2kΩ fixed resistor in parallel with the 2kΩ potentiometer sets its output range to 0-1V. The 2.5kΩ resistor sets a 5V common-mode input level to bias the XTR101 instrumentation amplifier input into its linear region.

With the span-setting resistor connections open, the XTR101 current-loop output is:

$$I_O = 4mA + V_{IN}/62.5\Omega$$

Where:
I_O = current loop output (A)
V_{IN} = Differential IA input voltage between pins 3 and 4 (V)

The XTR101 directly converts the 0-1V position sensor output into a 4-20mA current loop output. The isolated voltage output from the ISO122 is 0-5V for 0-50mm displacement.

Other, more specialized two-wire transmitters are also available. See the brief summary at right of available building blocks.

HPR117 LOW-COST ISOLATED DC/DC CONVERTER

Provides ±15V, 30mA isolated output power with 15V input. Key specifications are:
$\pm V_{OUT} = V_{IN}$, ±5%
(V_{IN} = 13.5V to 16.5V, I_{OUT} = 25mA)
I_{OUT} = 30mA continuous at 70°C.
8mA quiescent current, no load; 80% efficiency, full load
750VDC isolation rating

ISO122 LOW-COST PRECISION ISOLATION AMPLIFIER

Precision analog isolation amplifier in a standard 16-pin plastic DIP. Key specifications are:
Unity gain (±10V in to ±10V out), ±0.05%
0.02% max nonlinearity
5mA quiescent current
140dB isolation mode rejection at 60Hz
1500Vrms continuous isolation rating (100% tested)

RCV420

Self-contained 4-20mA receiver. Conditions and offsets 4-20mA input signals to give a precision 0-5V output. Contains precision voltage reference, 75Ω precision sense resistor and ±40V common-mode input range difference amplifier. The RCV420 has a total combined span and zero error of less than 0.1%—adjustable to zero.

XTR101

General purpose two-wire 4-20mA current-loop transmitter. This transmitter has an instrumentation amplifier input and two 1mA current sources for transducer excitation and offsetting.

XTR103

Two-wire RTD 4-20mA current-loop transmitter with 9V compliance. Similar to XTR101, but with internal linearization circuitry for direct interface to RTDs (Resistance Temperature Detectors). The XTR103, along with an RTD, forms a precision temperature to 4-20mA current-loop transmitter. Along with an RTD, the XTR103 can achieve better than 0.1% span linearity over a –200°C to +850°C temperature span.

XTR104

Two-wire bridge 4-20mA current-loop transmitter with 9V compliance. Similar to XTR101, but with shunt regulator and linearization circuitry for direct interface to resistor transducer bridges. The XTR104 can provide better than 0.1% span linearity from bridges with uncorrected linearity in excess of 2%.

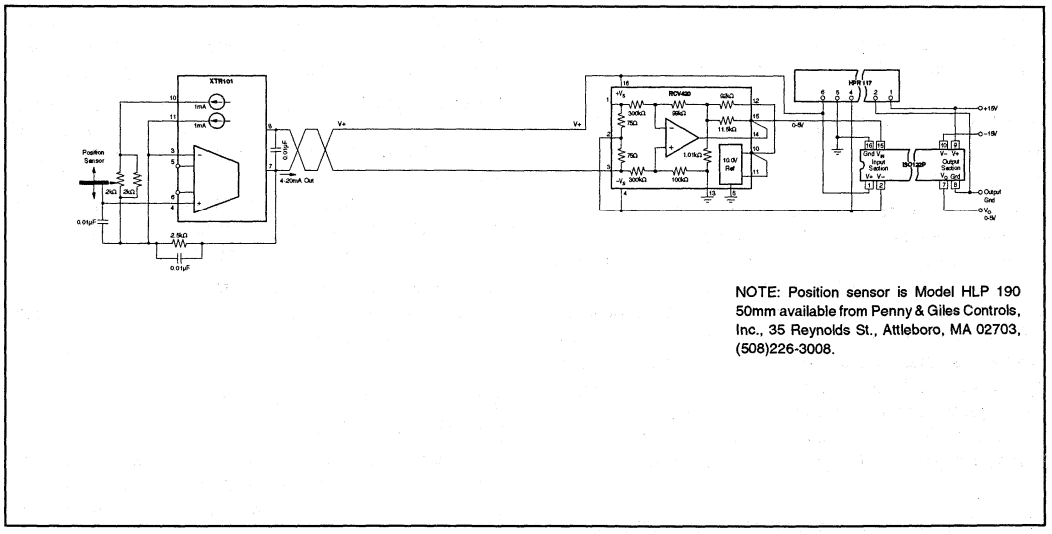


FIGURE 1. Four IC Packages and Transducer Form Complete Isolated 4-20mA Current-Loop System.

THERMISTOR-BASED TEMPERATURE MEASUREMENT

The most often measured physical parameter is temperature. Of the many commonly used temperature measurement transducers, the thermistor is the least expensive. Both positive and negative temperature coefficient types are available in all sorts of packages. Due to their high temperature coefficients, negative temperature coefficient types are the most common and widely used types. Thermistors are useful for temperature measurement from –55°C up to 300°C.

Figure 2 shows the circuit for a thermistor-based two-wire 4-20mA current-loop temperature measurement system. A bridge is formed with a thermistor, R_{T1}, and a 5kΩ variable resistor. The bridge is excited by the two 1mA current sources in the XTR101. The 5kΩ variable resistor is used to set the temperature-range zero for 4mA current loop output. The XTR101 span setting resistor, R_S, sets the span to get 20mA current-loop output at full-scale. XTR101 current-loop output is:

$$I_O = 4mA + V_{IN}(1 + 2500\Omega/R_S)/62.5\Omega$$

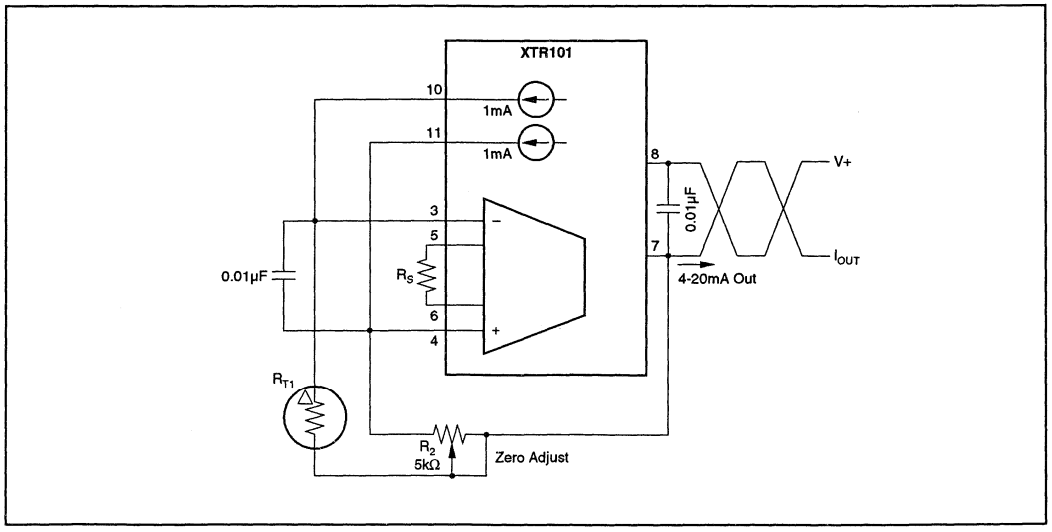


FIGURE 2. Basic Thermistor-Based Two-wire Temperature Measurement Using XTR101.

Where:
I_O = Current loop output (A)
V_{IN} = Differential IA input voltage between pins 3 and 4 (V)
R_S = Span-setting resistor (Ω)

Keep in mind that the maximum differential input range for the XTR101 is 1V.

Since the thermistor is a powered sensor, self heating can be a problem. For example, with a thermistor voltage of 5V, power dissipation is 5V • 1mA = 5mW. If a bead-in-glass type thermistor with a thermal resistance of 600°C/W is used, self-heating can increase the thermistor temperature by 3°C. To minimize this error, use a thermistor in a low thermal resistance package or lower the thermal resistance by heat sinking the thermistor to a thermal mass residing at the temperature to be measured. For example, if air temperature in an enclosure is to be measured, attach the thermistor to the package instead of mounting it in free air.

THERMISTOR-BASED LIQUID LEVEL INDICATOR

Due to high nonlinearities, thermistors can only be used for accurate temperature measurement over relatively small temperature spans. The high output of thermistors, however makes them attractive for other applications. In some applications thermistor self-heating can be used to advantage. Consider, for example, the liquid level indicator shown in Figures 3A and 3B. A bridge is formed by a pair of matched thermistors. The bridge is excited by the 1mA current sources in the XTR101. When both thermistors are submerged in liquid as shown in Figure 3A, the thermistors are at the same temperature—heat-sinked by the liquid. The potentiometer, R_3, is used to correct for component tolerances and zero the bridge for 4mA current-loop output.

When the liquid level falls below thermistor R_{T1} as shown in Figure 3B, the temperature of R_{T1} increases due to self-heating. The resulting bridge imbalance is measured by the XTR. Span-setting resistor, R_S, is selected to give 10mA output under low liquid level conditions. There is no simple rule for selecting R_S. Its value depends on thermistor selection and liquid properties and conditions.

When compared to level detectors using floats and moving parts, a thermistor-based liquid level indicator can have much better reliability.

GAS FLOW MEASUREMENT USING THERMISTORS

The liquid level indicator uses thermistor self-heating for a two-state high/low measurement. The gas flow measurement system shown in Figure 3C gives a quantitative flow rate measurement.

As in the previous example, a matched thermistor bridge is biased by the two 1mA current sources in the XTR101. One thermistor is positioned in the air flow stream. The other thermistor resides in still air—baffled from the air stream. The thermal resistance of the thermistor is proportional to the air flow rate. Potentiometer, R_3, is used to balance the bridge for 4mA out at zero flow rate. Span setting resistor, R_S, is selected to give a full-scale 20mA output at maximum flow rate. The value of R_S depends on thermistor characteristics and gas flow dynamics.

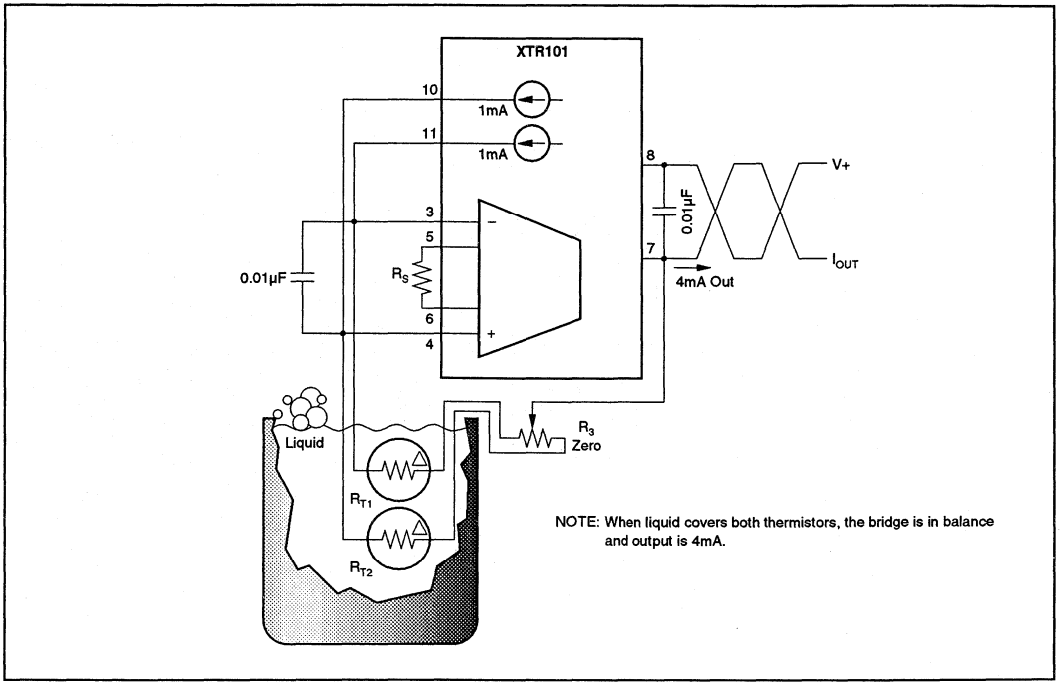


FIGURE 3A. Thermistor-Based Two-wire Liquid Level Detector Using XTR101.

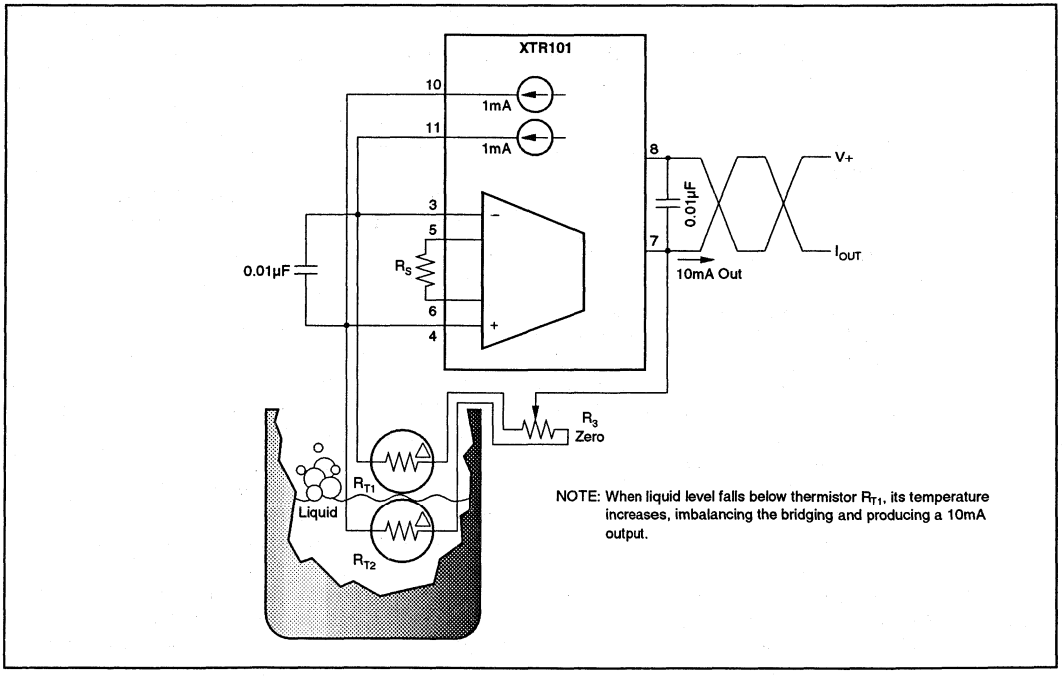


FIGURE 3B. Thermistor-Based Two-wire Liquid Level Detector Using XTR101.

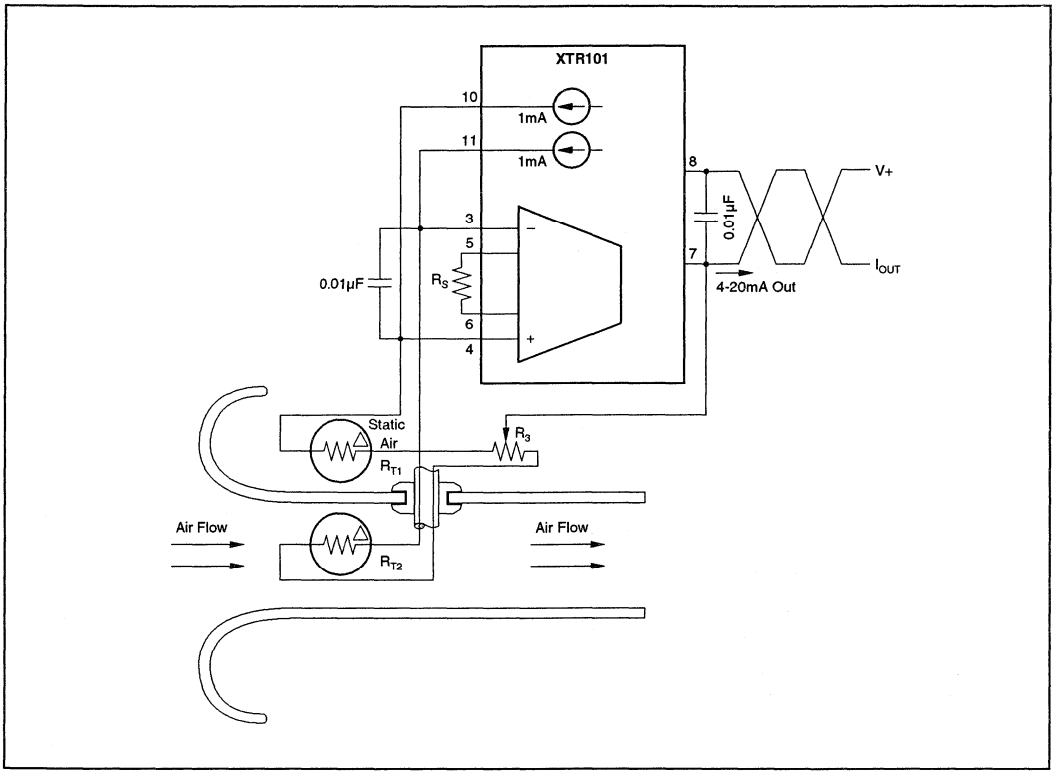


FIGURE 3C. Thermistor-Based Air Flow Rate Measurement Using XTR101.

Many systems today use resistance wire instead of thermistors for gas flow rate measurement. These are sometimes called hot-wire anemometers, and can have faster response due to lower (thermal mass)/(heat transfer) ratio.

DIODE-BASED TEMPERATURE MEASUREMENT

Cousin to the thermistor is the semiconductor diode temperature transducer. Regular silicon diodes, biased with constant current, have a forward voltage of about 0.6V with a temperature coefficient of about -2mV/°C. The usable upper temperature range for silicon semiconductors is about 125°C. Some high-temperature types are useful up to 200°C. In the future, novel semiconductor types such as silicon carbide and diamond promise to raise the upper usable temperature range of semiconductors into the 300°C to 600°C range. For now, thermocouples and RTDs can be used for higher temperature measurements.

Consider semiconductors for measurement of very low temperatures. Specialized silicon diodes can be used at very low temperatures. For example, the LakeShore Cryotronics, Inc., DT-470 series silicon diode cryogenic temperature sensor can be used to measure temperatures near absolute zero—from 1.4K to 475K.

Figure 4 shows a cryogenic temperature measurement circuit using a silicon diode temperature sensor. The sensor requires an accurate 10µA current source for excitation. One of the current sources from the XTR101 is scaled by a precision mirror to supply the 10µA excitation current.

To convert a 1mA current-source output into a precise 10µA for sensor excitation, a precision current mirror is formed with R_2, R_3, and A_1. The 1mA current source is connected to R_2 and the inverting input of the op amp. The op amp drives its inputs to the same voltage through R_3. The result is a precision 0.1V across both R_2 and R_3. The output current at the noninverting input is 1mA • R_2/R_3 = 10µA. With the amplifier specified, op amp bias currents add negligible error.

The other 1mA current source in the XTR101 supplies both a precision zero-set voltage and power for the op amp. The current source is connected to a 5.1V zener through R_1. The current through R_1 is precisely 1mA – 10µA. Zero-set voltage is R_1 • 990µA. The 5.1V zener sets the supply voltage of the op amp. The 249kΩ resistor in series with the temperature sensor diode forces the op amp to operate in its linear common-mode and output ranges.

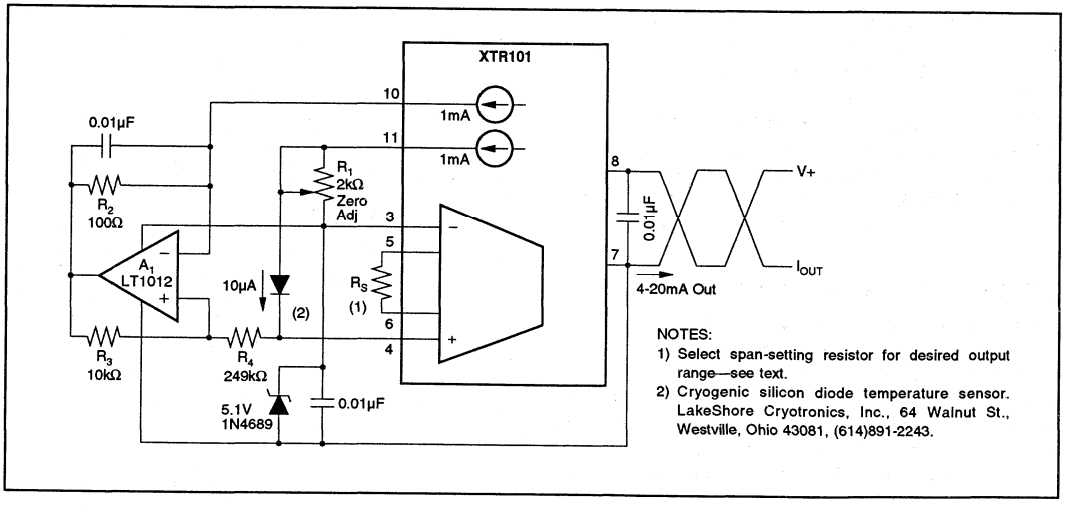


FIGURE 4. Silicon-Diode-Based Cryogenic Temperature Measurement System Using XTR101.

OTHER SILICON TEMPERATURE SENSORS

Although diodes are common in temperature measurement applications, their accuracy is limited. The temperature coefficient of a silicon diode has a nonlinearity of about 1% over a 0-100°C temperature span. Also, the stability of the forward voltage with time is limited.

Better accuracy can be obtained from silicon diodes by measuring the difference in forward voltage drops between diodes operating at different current densities. This voltage has a positive temperature coefficient proportional to absolute temperature. If the diodes have low bulk resistance and are well-matched, temperature coefficient linearity of better than 0.01% is possible.

THERMOCOUPLE-BASED TEMPERATURE MEASUREMENT

In the United States, the most commonly used precision temperature sensor is the thermocouple. Depending on the type, wire size, and construction, thermocouples can be used to measure temperatures from about –250°C up to 1700°C.

When designing thermocouple-based measurement systems, it is helpful to understand how thermocouples work. A common misconception is that temperature somehow creates an EMF in the thermocouple junction.

Thermocouples are based on the Thomson effect, which states that, in a single conductor, a voltage difference will exist between two points that are at different temperatures. The voltage difference is proportional to the temperature differential, and its magnitude and direction depends on the conductor material.

A thermocouple is formed when a pair of dissimilar conductors are connected at one end. If a temperature difference exists along the length, between the two ends of the thermocouple, a voltage output proportional to the temperature difference is generated. This phenomenon is known as the Seebeck effect. The measure of the Seebeck effect is known as the Seebeck coefficient. Seebeck coefficients for common thermocouple types range from about 6µV/°C to 60µV/°C.

A thermocouple responds to the temperature difference between its output and the temperature measuring point where the thermocouple wires are joined. To determine the temperature at the measuring point you must know the temperature at the thermocouple output. One way to do this is to keep the output in an ice bath at 0°C. Thermocouple calibration tables were derived this way, and, following tradition, the thermocouple output junctions have come to be known as *the cold junction.* In reality, the measurement junction may be colder.

In most modern thermocouple-based temperature measurement systems, the thermocouple output end simply resides at the ambient temperature. To compensate for variations in ambient temperature, a temperature-dependent voltage is summed with the thermocouple output. This method is known as cold-junction compensation.

A thermocouple-based 4-20mA temperature measurement system with cold-junction compensation is shown in Figure 5. In this application, a *type J* thermocouple is combined with an XTR101 to give a 4-20mA output for a 0-1000°C temperature change. One of the 1mA current sources in the XTR101 biases a silicon diode used as a temperature transducer for cold-junction compensation. For good accuracy, the thermocouple output junctions and the diode must be maintained at the same temperature. The diode has a forward-voltage temperature dependance of about –2mV/°C. The R_1, R_2 resistor divider attenuates the temperature depen-

dence to match the thermocouple Seebeck coefficient. The other 1mA current source is connected to R_3 for zero adjustment. The 2.5kΩ resistor establishes a 5V bias to keep the XTR101 IA in its linear range. Adjust R_3 for 4mA out with the thermocouple measurement end at 0°C. The span-setting resistor is chosen to give a 4-20mA output for the 58mV/1000°C thermocouple output. Nominal component values and Seebeck coefficients for recommended thermocouples are shown in the table in Figure 5 below.

RTD-BASED TEMPERATURE MEASUREMENT

The highest performance temperature measurement transducer in common use is the platinum resistance temperature detector (RTD). RTDs can be used to accurately measure temperatures from –200°C to 850°C. As with other temperature transducers, best performance requires correction for nonlinearities. The XTR103 is a special purpose 4-20mA current-loop transmitter with built-in circuitry for RTD linearization.

To understand how the linearization circuitry works, consider how an RTD works. In the range from 0°C to 850°C, the temperature/resistance relationship of a Pt-type RTD is:

$$RTD = R_0 \bullet (1 + A \bullet T + B \bullet T^2)$$

Where:
RTD = DC resistance value of RTD (Ω) at temperature T (°C)
R_0 = Value of RTD at 0°C (Ω)

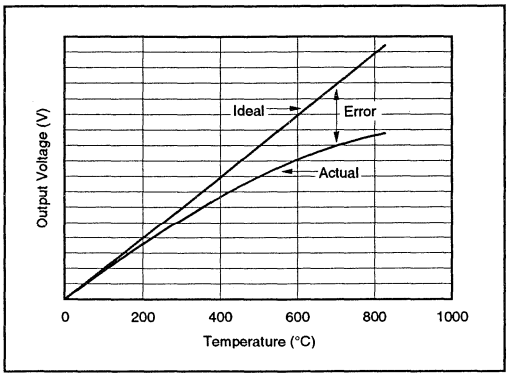
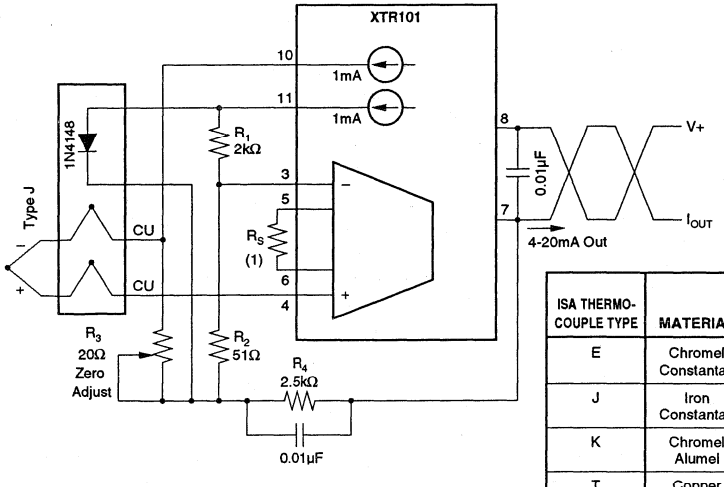


FIGURE 6. RTD Output Voltage vs Temperature.

R_0 = 100Ω for Pt100 = 200Ω for Pt200
A = Detector constant = 3.908 10^{-3} ($°C^{-1}$) (for Pt100)
B = Detector constant = –5.802 10^{-7} ($°C^{-2}$) (for Pt100)

The second-order term, $B \bullet T^2$, in the temperature/resistance relationship causes a nonlinearity in the response of ≈3.6% for a 0°C to 850°C temperature change. Figure 6 shows a plot of the voltage across an RTD with constant current excitation. The nonlinearity is exaggerated to show its characteristic shape. Increasing the current through the RTD by an appropriate amount as temperature increases will "straighten out" the curve and reduce the nonlinearity.



ISA THERMOCOUPLE TYPE	MATERIAL	SEEBECK COEFFICIENT AT 0°C (µV/°C)	R_1 (Ω)	R_2 (Ω)	R_3 (Ω)
E	Chromel Constantan	58.5	2k	60.3	19.0
J	Iron Constantan	50.2	2k	51.5	16.3
K	Chromel Alumel	39.4	2k	40.2	12.8
T	Copper Constantan	38.0	2k	38.7	12.3

NOTE: (1) For 4-20mA with 0-1000°C, R_S = 153.9Ω, nominal R_3 = 16.3Ω.

FIGURE 5. Thermocouple-Based Two-wire Temperature Measurement Using XTR101.

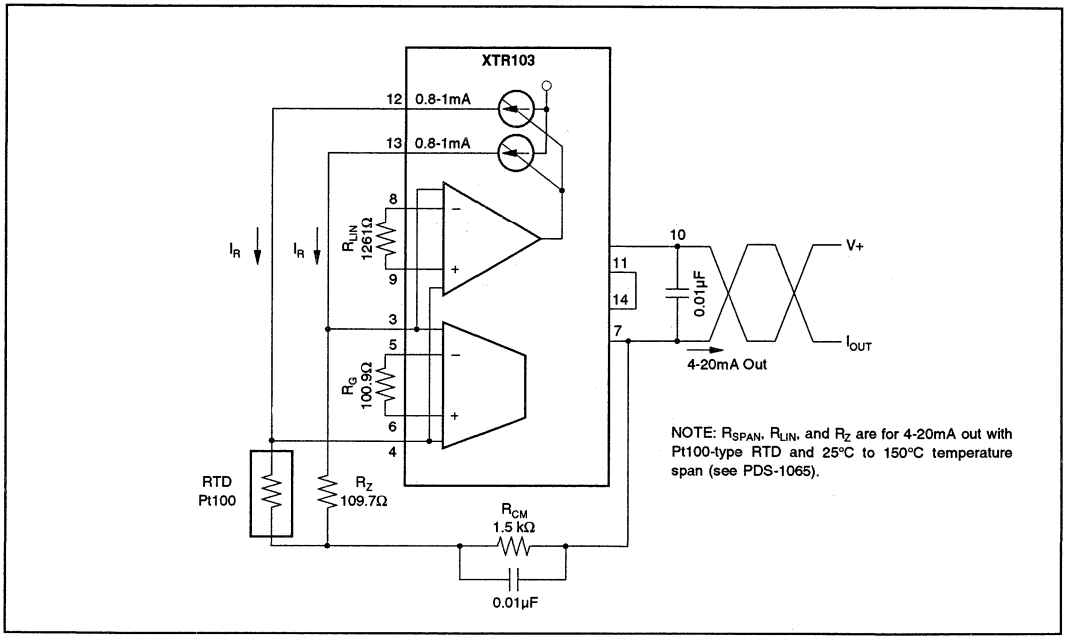


FIGURE 7. RTD-Based Two-wire Temperature Measurement Using XTR103.

An RTD measurement circuit using the XTR103 is shown in Figure 7. The XTR103 is similar to the XTR101, but contains two instrumentation amplifiers—one in the main current control loop, one for linearization.

As with the thermistor-based system, a bridge is formed with an RTD and a fixed resistor, R_Z. The bridge is excited by the two current sources in the XTR103. R_Z is selected to set the temperature-range zero for 4mA current loop output. The span-setting resistor, R_G, sets the IA gain for a 20mA current-loop output at full-scale. The 1.27kΩ resistor biases the IA into its linear range.

The two instrumentation amplifiers are internally connected in parallel. The second IA controls the current sources used to excite the RTD bridge. Gain of the second IA is set by R_{LIN}. With R_{LIN} open the current sources are fixed at 0.8mA. Under control of the second IA, current source output can be increased to 1.0mA—adequate for –200°C to 850°C linearization of both Pt100 and Pt200 type RTDs. Current source output is controlled by the IA input signal according to the following equation.

$$I_R = 0.0008 + V_{IN}/(2 \bullet R_{LIN})$$

Where:

I_R = Current source output (A)

V_{IN} = Voltage difference at the input of the IAs (V)

With the proper R_{LIN}, current source output is increased at the correct rate to correct RTD nonlinearity. Simple selection procedures for R_{LIN} are outlined in the XTR103 product data sheet.

Figure 8 shows the residual nonlinearity for a 0 to 850°C span of both a linearized and an uncorrected RTD. The nonlinearity is improved from 3.6% to better than 0.1%, an improvement of better than 30 to 1. Correction of nonlinearity for smaller spans is even better. The nonlinearity of a 0°C to 100°C span can theoretically be improved from 0.38% to 0.001%. In practice, nonlinearity of better than 0.01% can be expected.

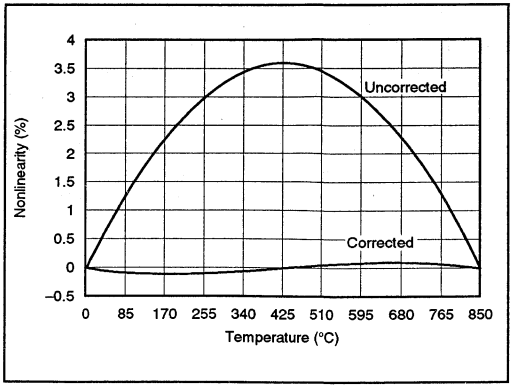


FIGURE 8. Nonlinearity vs Temperature Plot Comparing Residual Nonlinearity of Corrected and Uncorrected RTDs.

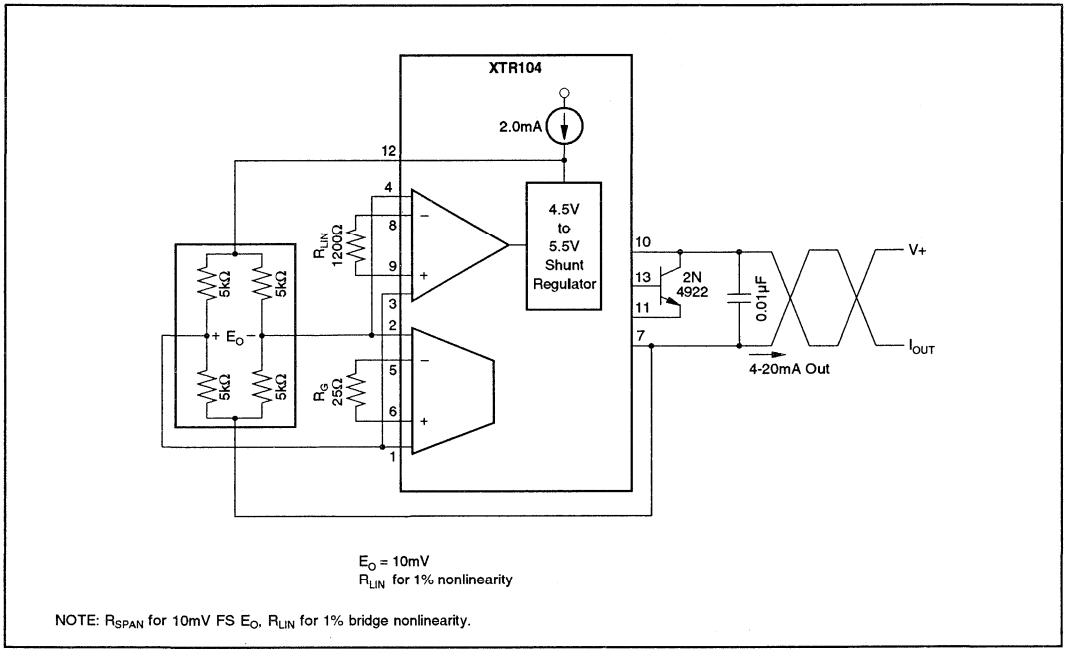


FIGURE 9. Bridge-Based Two-wire Measurement System Using XTR104.

BRIDGE MEASUREMENT 4-20mA CURRENT-LOOP SYSTEMS

Another common transducer is based on the four-resistor (Wheatstone) bridge. Wheatstone bridges are commonly used for pressure measurement. Bridges are usually intended to be biased with a voltage rather than a current source. By changing the voltage bias in response to the bridge output, bridge nonlinearities can be eliminated.

The XTR104 is a two-wire 4-20mA current loop transmitter designed specifically for use with bridges. It is similar to the XTR103 in that it contains two instrumentation amplifiers—one for signal, one for linearization. The difference is the addition of a 5V shunt regulator. The shunt regulator can be adjusted from 4.5V to 5.5V range under control of the second IA. The inputs to the second IA are brought out separately because, unlike RTD linearization, the correction signal may need to be either polarity for bridge linearizaton. Simple selection procedures for R_{LIN} are outlined in the XTR104 product data sheet.

The complete bridge-based 4-20mA current loop transmitter circuit is shown in Figure 9. The XTR104 requires an external pass transistor as shown. Using an external pass device keeps power dissipation out of the XTR104 and improves accuracy. As an option, the XTR103 can use an external pass transistor. In either case, a garden variety bipolar transistor such as the 2N4922 shown is adequate.

Notice that, as with the other two-wire transmitters, only 2mA is available for bridge excitation. This means that, for accurate 5V regulation, bridge elements can be no less than 2.75kΩ unless additional resistance is added in series with the bridge.

BURR-BROWN® APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

SINGLE SUPPLY 4-20mA CURRENT LOOP RECEIVER

By R. Mark Stitt and David Kunst (602) 746-7445

Many industrial current-loop data acquisition systems operate on a 24V or 28V single supply. You can make a single-supply current loop receiver with the RCV420 by using its 10V reference as a pseudo ground. The RCV420 will convert a 4-20mA loop current into a 0 to 5V output voltage with no external components required. The current loop can be sourcing or sinking and can be referenced to either the power-supply V+ or ground.

The complete circuit for a single-supply current loop receiver is shown in Figure 1. In this application, a 4-20mA current source referenced to power-supply ground drives the receiver. The *V–* terminal and the *Ref Com* terminal of the RCV420 are both tied to power supply ground. The 10V reference output (*Ref Out*) becomes a pseudo ground where the current loop receiver common pin (*Rcv Com*) is tied. The current loop receiver output is now referenced to the 10V pseudo ground.

In normal operation, the 4-20mA current loop signal would produce a 0-5V output with the RCV420 offset pin (*Ref In*) connected to the +10V reference. The 10V reference provides a –1.25V offset so 4mA input current will produce 0V out. In this application, the *Ref In* pin is connected to power supply ground which acts as a –10V reference—producing a +1.25V offset. Now with the inputs connected for an inverted output signal, the RCV420 output will be 0 to –5V referenced to the pseudo ground. Since the pseudo ground is at 10V, the actual output will be 10V to 5V—a signal which can drive most floating ground meters.

For a current loop receiver with a 4-20mA current sink referenced to the power-supply V+, use the connection shown in Figure 2.

The circuit can operate on a single supply ranging from +15V to +36V (+44V absolute max). The pseudo ground (*Ref Out*) can source or sink up to 5mA.

For an isolated single-supply 4-20mA current loop receiver, you can connect the circuit to an isolation amplifier as shown in Figure 3. In this circuit the ISO122 is operated single-supply using the 10.0V pseudo ground. Note that the output side of the isolation amplifier still requires dual supplies.

Output from the ISO122 will be 0 to –5V. You could interchange the input connections to the ISO122 to get a 0 to 5V output, but power-supply rejection would degrade performance.

The ISO122 is a low-cost iso amp in a standard plastic DIP. For a hermetic isolation amplifier, use the ISO120. Hook-up details are shown in Application Bulletin AB-009.

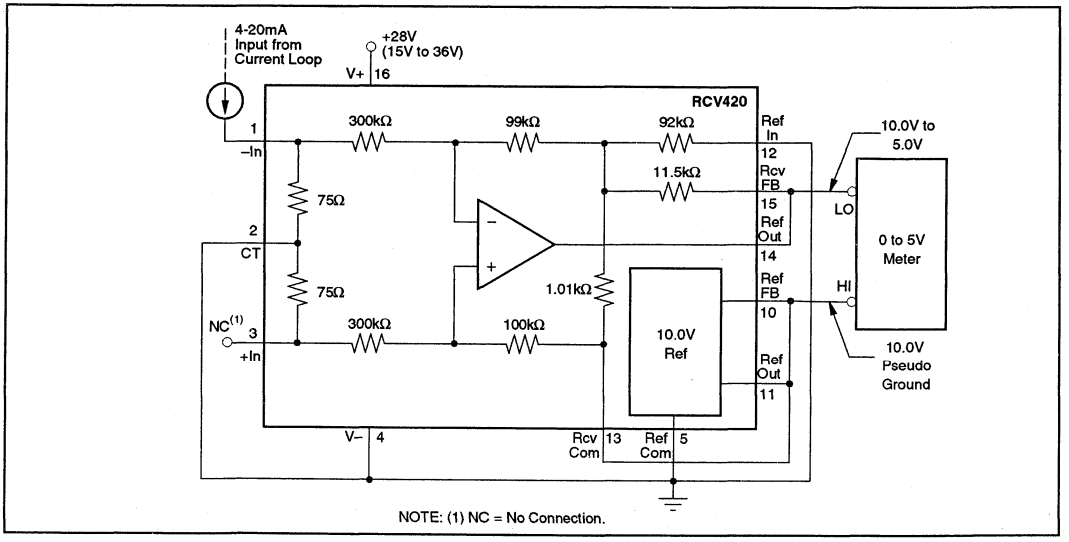


FIGURE 1.

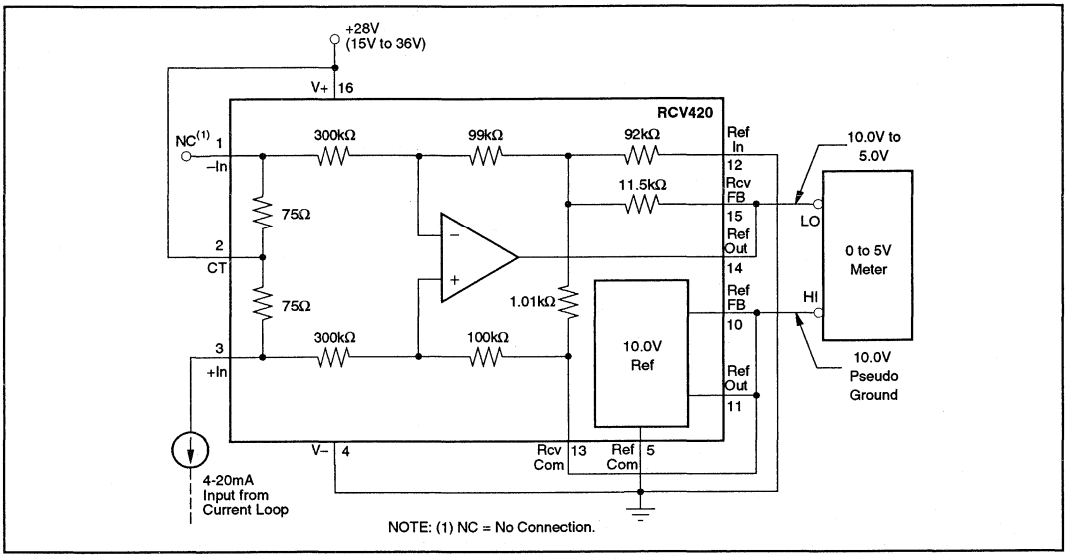


FIGURE 2.

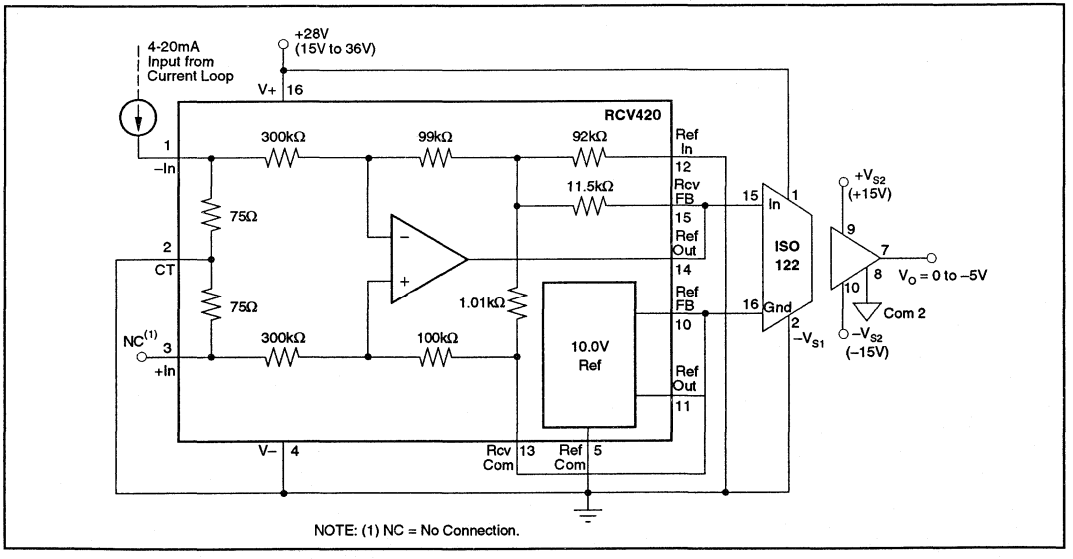


FIGURE 3.

BURR-BROWN®
APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

SINGLE-SUPPLY, LOW-POWER MEASUREMENTS OF BRIDGE NETWORKS

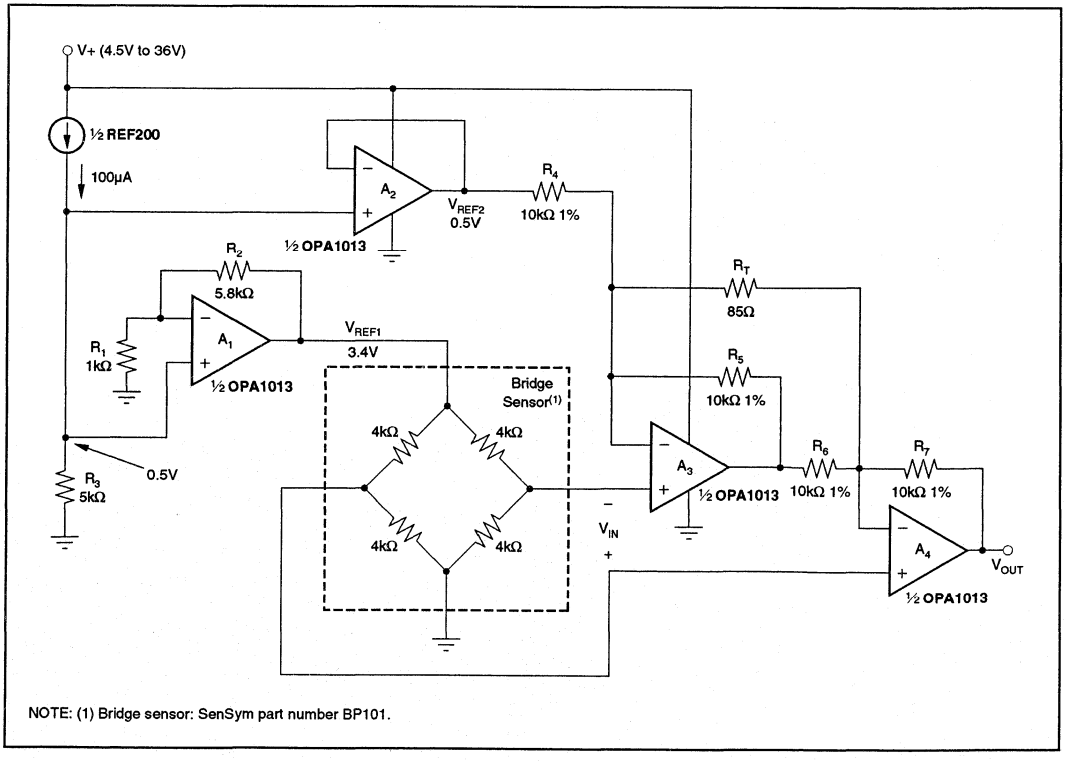
By Bonnie Baker (602) 746-7984

Bridge sensor measurements often need to be made in systems operating on a single 5V power supply. An OPA1013 dual op amp along with a REF200 current source, makes an excellent bridge measurement system which features low power single-supply 5V operation and immunity to power supply variations. One OPA1013 dual op amp is used as a two-op-amp instrumentation amplifier. A second OPA1013 is used with a REF200 to make two voltage references. One voltage reference is used to power the bridge, the other is used to offset the instrumentation amplifier.

In Figure 1, A_1 and A_2 (an OPA1013 dual operational amplifier) along with one of the current sources from the REF200 establishes a 3.4V voltage reference for excitation of a pressure transducer bridge. Although the REF200 contains two current sources, the second current source is not used, which keeps power consumption low.

A second OPA1013 (A_3, A_4), connected as a two op amp instrumentation amplifier, amplifies the differential voltage output from the bridge. Gain is easily adjusted with R_T. If 1% resistors are used for R_4-R_7, common-mode rejection will be better than 80dB for gains greater than 200V/V. A CMR of 80dB is quite acceptable in this application.

The instrumentation amplifier's reference connection is made to a 0.5V reference at the output of A_2. This voltage sets an instrumentation amplifier offset so that a zero bridge output will result in a 0.5V instrumentation amplifier output. The value of the offset can be changed by adjusting R_3.



NOTE: (1) Bridge sensor: SenSym part number BP101.

FIGURE 1. Single-Supply Bridge Measurement Circuit.

For $V_{REF2} = 0.5V$, $R_3 = 5k\Omega$.

For $V_{REF1} = 3.4V$, $R_1 = 1k\Omega$, $R_2 = 5.8k\Omega$.

The required instrumentation amplifier gain can be calculated from its input voltage and the output span. The output voltage equation is:

$$V_{OUT} = V_{IN} [2(1 + R/R_T)] + V_{OUT1}$$

This equation can be rewritten as:

$$V_{OUT} = V_{IN} \bullet GAIN + V_{OUT1}$$

Where: $V_{OUT1} = V_{OUT}$ for zero instrumentation amplifier input or for zero pressure applied to the pressure transducer,

$$GAIN = -V_{OUT}/-V_{IN} = 2(1 + R/R_T)$$
$$R = R_4 = R_5 = R_6 = R_7$$

For example, a pressure sensor specified for 12.6mV full-scale output with 3.4V excitation voltage:

$$GAIN = 238V/V$$
$$\text{if } R = 10k\Omega, R_T = 85\Omega$$

If adjustment is required:

Adjustment Procedure

1. With zero-pressure applied, adjust R_3 for $V_{OUT} = 0.5V$.
2. Apply full-scale pressure to the sensor and adjust R_T for $V_{OUT} = 3.5V$.
3. Repeat procedure if necessary.

There is no true single-supply instrumentation amplifier on the market today. Although some come close, their applications are limited because they are fixed gain. The OPA1013 provides the best solution for this application because of its single supply operation and output swing range within 15mV from ground. The REF200 requires one power supply and is ideal for use in single supply systems. The REF200 provides a simple, economical way to make adjustable voltage references.

The supply voltage of the bridge conditioning circuit can range from 4.5V to 36V without affecting the operation of the circuit. Because of the low quiescent current of the OPA1013 (350μA) and the low current requirements of the REF200 (100μA), this is an excellent circuit for battery operated applications.

BURR-BROWN® APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

DIODE-BASED TEMPERATURE MEASUREMENT

By R. Mark Stitt and David Kunst (602) 746-7445

Diodes are frequently used as temperature sensors in a wide variety of moderate-precision temperature measurement applications. The relatively high temperature coefficient of about –2mV/°C is fairly linear. To make a temperature measurement system with a diode requires excitation, offsetting, and amplification. The circuitry can be quite simple. This Bulletin contains a collection of circuits to address a variety of applications.

THE DIODE

Just about any silicon diode can be used as a temperature measurement transducer. But the Motorola MTS102 Silicon Temperature Sensor is a diode specifically designed and optimized for this function. It is intended for temperature sensing applications in automotive, consumer and industrial products where low cost and high accuracy are important. Packaged in a TO-92 package it features precise temperature accuracy of ±2°C from –40°C to +150°C.

EXCITATION

A current source is the best means for diode excitation. In some instances, resistor biasing can provide an adequate approximation, but power supply variations and ripple can cause significant errors with this approach. These problems are exacerbated in applications with low power supply voltages such as 5V single supply systems. Since the MTS102 is specified for 100µA operation, the Burr-Brown REF200 Dual 100µA Current Source/Sink makes the perfect match. One current source can be used for excitation and the other current source can be used for offsetting.

AMPLIFICATION

In most instances, any precision op amp can be used for diode signal conditioning. Speed is usually not a concern. When ±15V supplies are available, the low cost precision OPA177 is recommended. For 5V single-supply applications, the OPA1013 Dual Single-Supply op amp is recommended. Its inputs can common-mode to its negative power supply rail (ground in single-supply applications), and its output can swing to within about 15mV of the negative rail.

Figure 1 shows the simplest diode-based temperature measurement system. One of the 100µA current sources in the REF200 is used for diode excitation. The other current source is used for offsetting. One disadvantage of this circuit is that the span (GAIN) and zero (OFFSET) adjustments are interactive. You must either accept the initial errors or use an interactive adjustment technique. Another *possible* disadvantage is that the temperature to voltage conversion is inverting. In other words, a positive change in temperature results in a negative change in output voltage. If the output is to be processed in a digital system, neither of these limitations may be a disadvantage.

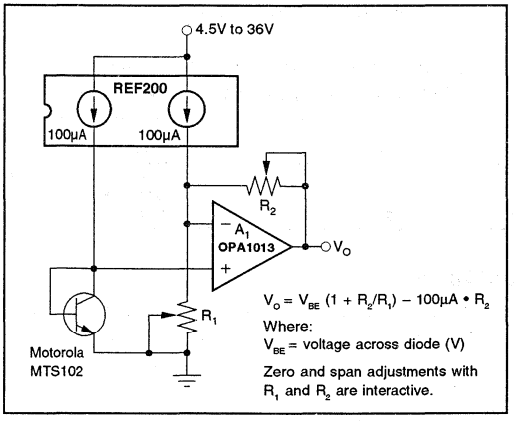


Figure 1. Simple Diode-based Temperature Measurement Circuit.

The following relationships can be used to calculate nominal resistor values for the Figure 1 circuit.

BASIC TRANSFER FUNCTION

$$V_O = V_{BE}\,(1 + R_2/R_1) - 100\mu A \bullet R_2$$

CALCULATING RESISTOR VALUES

$$R_1 = \frac{(\delta V_O/\delta T) \bullet (V_{BE25} + T_C \bullet (T_{MIN} - 25°C)) - (T_C \bullet V1)}{100\mu A \bullet ((\delta V_O/\delta T) - T_C)}$$

$$R_2 = R_1 \bullet \left(\frac{(\delta V_O/\delta T)}{T_C} - 1\right)$$

Where:

R_1, R_2 = Resistor values (Ω)

V_{BE} = Voltage across diode (V)

V_{BE25} = Diode voltage at 25°C (V)

Three choices are available for the MTS102—See table on page 2.

V_1 = Output voltage of circuit at T_{MIN} (V)

V_O = Output voltage of circuit (V)

T_C = Diode temperature coefficient (V/°C)

T_C value depends on V_{BE25}—See table below.

T_{MIN} = Minimum process temperature (°C)

$\delta V_O/\delta T$ = Desired output voltage change for given temperature change (V/°C)
(Note: Must be negative for Figure 1 circuit.)

AVAILABLE VBE_{25} AND T_C VALUES FOR MOTOROLA MTS102 TEMPERATURE SENSOR

V_{BE25} (V)	T_C (V/°C)
0.580	–0.002315
0.595	–0.002265
0.620	–0.002183

EXAMPLE

Design a temperature measurement system with a 0 to –1.0V output for a 0 to 100°C temperature.

T_{MIN} = 0°C

$\delta V_O/\delta T$ = (–1V – 0V)/(100°C – 0°C) = –0.01V/°C

If V_{BE25} = 0.595V, T_C = –0.002265V/°C, and
R_1 = 8.424kΩ
R_2 = 28.77kΩ

For a 0 to –10V output with a 0 to 100°C temperature:
R_1 = 6.667kΩ
R_2 = 287.7kΩ

If independent adjustment of offset and span is required consider the circuit shown in Figure 2. In this circuit, a third resistor, R_{ZERO} is added in series with the temperature-sensing diode. System zero (offset) can be adjusted with R_{ZERO} without affecting span (gain). To trim the circuit adjust span first. Either R_1 or R_2 (or both) can be used to adjust span. As with the Figure 1 circuit this circuit has the possible disadvantage that the temperature to voltage conversion is inverting.

The following relationships can be used to calculate nominal resistor values for the Figure 2 circuit.

BASIC TRANSFER FUNCTION

$$V_O = (V_{BE} + 100\mu A \bullet R_{ZERO}) \bullet (1 + R_2/R_1) - 100\mu A \bullet R_2$$

CALCULATING RESISTOR VALUES

Set R_{ZERO} = 1kΩ (or use a 2kΩ pot)

$$R_1 = \frac{(\delta V_O/\delta T) \bullet (V_{BE25} + (R_{ZERO} \bullet 100\mu A) + T_C \bullet (T_{MIN} - 25°C)) - (T_C \bullet V_1)}{100\mu A \bullet ((\delta V_O/\delta T) - T_C)}$$

$$R_2 = R_1 \bullet \left(\frac{(\delta V_O/\delta T)}{T_C} - 1\right)$$

Where:

R_{ZERO} = Zero (offset) adjust resistor (Ω)

Others = as before

EXAMPLE

Design a temperature measurement system with a 0 to –1.0V output for a 0 to 100°C temperature.

T_{MIN} = 0°C

$\delta V_O/\delta T$ = (–1V – 0V)/(100°C – 0°C) = –0.01V/°C

If V_{BE25} = 0.595V, T_C = –0.002265V/°C, and
R_{ZERO} = 1kΩ (use 2kΩ pot)
R_1 = 9.717kΩ
R_2 = 33.18kΩ

For a 0 to –10V output with a 0 to 100°C temperature:
R_{ZERO} = 1kΩ (use 2kΩ pot)
R_1 = 7.69kΩ
R_2 = 331.8kΩ

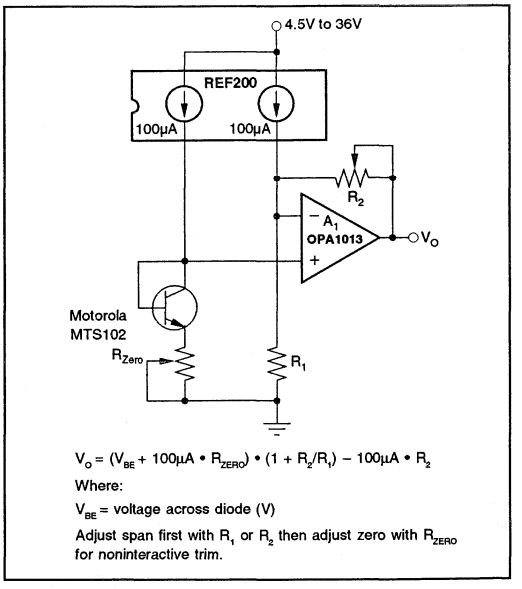


Figure 2. Diode-based Temperature Measurement Circuit with Independent Span (gain) and Zero (offset) Adjustment.

For a noninverting temperature to voltage conversion, consider the circuit shown in Figure 3. This circuit is basically the same as the Figure 2 circuit except that the amplifier is connected to the low side of the diode. With this connection, the temperature to voltage conversion is noninverting. As before, if adjustment is required, adjust span with R_1 or R_2 first, then adjust zero with R_{ZERO}.

A disadvantage of the Figure 3 circuit is that it requires a negative power supply.

The following relationships can be used to calculate nominal resistor values for the Figure 3 circuit.

BASIC TRANSFER FUNCTION

$$V_O = (-V_{BE} - 100\mu A \bullet R_{ZERO}) \bullet (1 + R_2/R_1) + 100\mu A \bullet R_2$$

CALCULATING RESISTOR VALUES

R_1 = same as Figure 2
R_2 = same as Figure 2

Where:
Components = as before

EXAMPLE

Design a temperature measurement system with a 0 to 1.0V output for a 0 to 100°C temperature.

$T_{MIN} = 0°C$

$$\delta V_O/\delta T = (1V - 0V)/(100°C - 0°C) = 0.01V/°C$$

If $V_{BE25} = 0.595V$, $T_C = -0.002265V/°C$, and
$R_{ZERO} = 1k\Omega$
$R_1 = 9.717k\Omega$
$R_2 = 33.18k\Omega$

For a 0 to 10V output with a 0 to 100°C temperature:
$R_{ZERO} = 1k\Omega$
$R_1 = 7.69k\Omega$
$R_2 = 331.8k\Omega$

For a single-supply noninverting temperature to voltage conversion, consider the Figure 4 circuit. This circuit is similar to the Figure 2 circuit, except that the temperature-sensing diode is connected to the inverting input of the amplifier and the offsetting network is connected to the noninverting input. To prevent sensor loading, a second amplifier is connected as a buffer between the temp sensor and the amplifier. If adjustment is required, adjust span with R_1 or R_2 first, then adjust zero with R_{ZERO}.

The following relationships can be used to calculate nominal resistor values for the Figure 4 circuit.

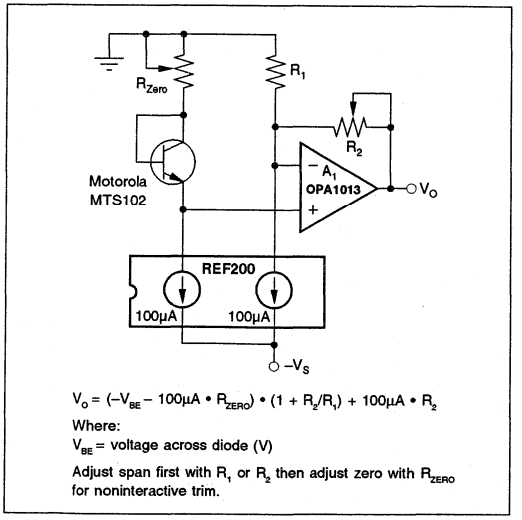


Figure 3. Positive Transfer Function Temperature Measurement Circuit with Independent Span (gain) and Zero (offset) Adjustment.

BASIC TRANSFER FUNCTION

$$V_O = 100\mu A \bullet R_{ZERO} \bullet (1 + R_2/R_1) - V_{BE} \bullet R_2/R_1$$

CALCULATING RESISTOR VALUES

$$R_{ZERO} = \frac{(T_C \bullet V_I) - (\delta V_O/\delta T) \bullet (V_{BE25} + T_C \bullet (T_{MIN} - 25°C))}{100\mu A \bullet (T_C - (\delta V_O/\delta T))}$$

$R_1 = 10k\Omega$ (arbitrary)

$$R_2 = -R_1 \bullet \left(\frac{(\delta V_O/\delta T)}{T_C}\right)$$

Where:
Components = as before

EXAMPLE

Design a temperature measurement system with a 0 to 1.0V output for a 0 to 100°C temperature.

$T_{MIN} = 0°C$

$$\delta V_O/\delta T = (1V - 0V)/(100°C - 0°C) = 0.01V/°C$$

If $V_{BE25} = 0.595V$, $T_C = -0.002265V/°C$, and
$R_{ZERO} = 5.313k\Omega$
$R_1 = 10.0k\Omega$
$R_2 = 44.15k\Omega$

For a 0 to 10V output with a 0 to 100°C temperature:

R_{ZERO} = 6.372kΩ

R_1 = 10.0kΩ

R_2 = 441.5kΩ

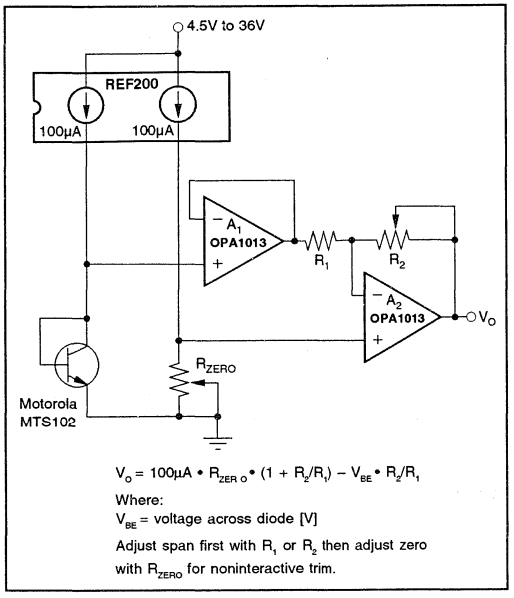


Figure 4. Single-supply Positive Transfer Function Temperature Measurement Circuit with Independent Span (gain) and Zero (offset) Adjustment.

For differential temperature measurement, use the circuit shown in Figure 5. In this circuit, the differential output between two temperature sensing diodes is amplified by a two-op-amp instrumentation amplifier (IA). The IA is formed from the two op amps in a dual OPA1013 and resistors R_1, R_2, R_3, R_4, and R_{SPAN}. R_{SPAN} sets the gain of the IA. For good common-mode rejection, R_1, R_2, R_3, and R_4 must be matched. If 1% resistors are used, CMR will be greater than 70dB for gains over 50V/V. Span and zero can be adjusted in any order in this circuit.

The following relationships can be used to calculate nominal resistor values for the Figure 5 circuit.

BASIC TRANSFER FUNCTION

$$V_O = ((V_{BE2} + 100\mu A \bullet R_{ZERO2}) - (V_{BE1} + 100\mu A \bullet R_{ZERO1})) \bullet GAIN$$

Where:

$GAIN = 2 + 2 \bullet R_1/R_{SPAN}$

CALCULATING RESISTOR VALUES

$$R_{SPAN} = \frac{-2 \bullet R_1 \bullet T_C}{(\delta V_O/\delta T) + 2 \bullet T_C}$$

$R_{ZERO1} = R_{ZERO2}$ = 500Ω (use 1kΩ pot for R_{ZERO})

Where:

R_{SPAN} = Span (gain) adjust resistor [Ω]

Others = as before

EXAMPLE

Design a temperature measurement system with a 0 to 1.0V output for a 0 to 1°C temperature differential.

T_{MIN} = 0°C

$\delta V_O/\delta T$ = (1V – 0V)/(1°C – 0°C) = 1.0V/°C

If V_{BE25} = 0.595V, T_C = –0.002265V/°C, and

R_{ZERO} = 1kΩ pot

R_1, R_2, R_3, R_4 = 100kΩ, 1%

R_{SPAN} = 455Ω

For a 0 to 10V output with a 0 to 1°C temperature differential:

R_{ZERO} = 1kΩ pot

R_1, R_2, R_3, R_4 = 100kΩ, 1%

R_{SPAN} = 45.3Ω

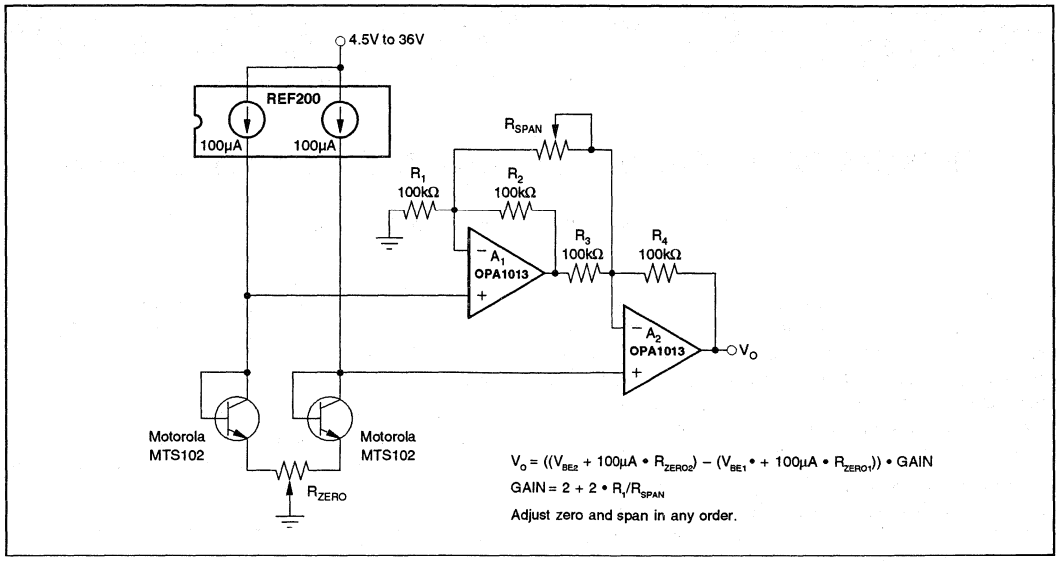


Figure 5. Differential Temperature Measurement Circuit.

BURR-BROWN®
APPLICATION BULLETIN

Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

PROGRAMMABLE-GAIN INSTRUMENTATION AMPLIFIERS

By David Jones (602) 746-7696 and R. Mark Stitt

The INA115 is a precision instrumentation amplifier (IA). Its gain-sense and amplifier output connections are available so that gains can be accurately set using external resistors. By adding switches or a multiplexer, you can make a precision programmable-gain IA (PGIA). Using the circuit topology shown in this bulletin, the switches are in series with op amp inputs so their resistance does not add error.

If you need an IA with more gain steps, you can cascade two or more PGIAs. For example, if you cascade two PGA205s you will get gains of 1, 2, 4, 8, 16, 32, and 64V/V.

For other gains or gain-steps, you may want to make your own PGIA using an INA115. The circuits and equations

binary gains of 1, 2, 4, and 8V/V, use the PGA204 or PGA205.

INA131	100
PGA204	1, 10, 100, 1000
PGA205	1, 2, 4, 8

TABLE I. Fixed and Programmable-Gain IAs.

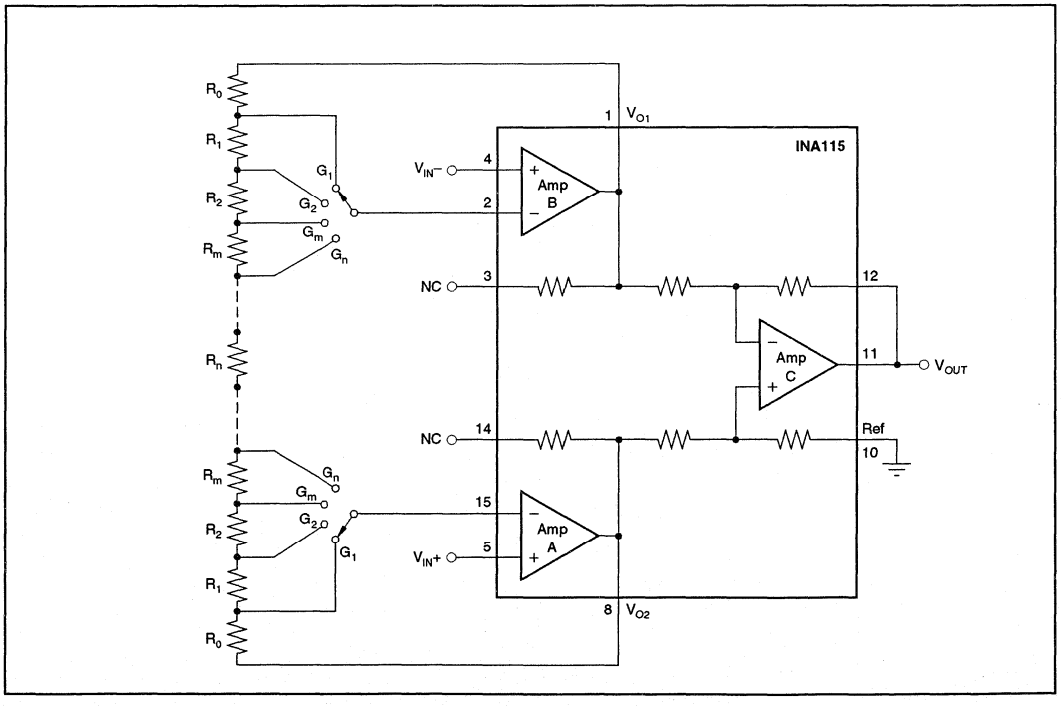


FIGURE 1. Programmable-Gain Instrumentation Amplifier with n Gain Steps and Lowest Gain > 1V/V.

If you want a PGIA with n gains and the first gain is not unity (1V/V), use the following relationships and the circuit shown in Figure 1.

RESISTOR VALUES FOR PGIA WITH n GAINS AND LOWEST GAIN > 1V/V

R_0 = Your choice (e.g. 25kΩ)

R_0 = 25kΩ when using the internal feedback resistors in the INA115 (see Figure 2)

$$R_1 = \frac{R_0 (G_1 - G_2)}{G_2 (1 - G_1)}$$

$$R_2 = \frac{G_1 R_0 (G_2 - G_3)}{G_2 G_3 (1 - G_1)}$$

$$\vdots$$

$$R_m = \frac{G_1 R_0 (G_m - G_{m+1})}{G_m G_{m+1} (1 - G_1)}$$

$$R_n = \frac{2 G_1 R_0}{G_n (G_1 - 1)}$$

Where:

G_m = Intermediate gain (V/V)
G_n = Highest gain (V/V)
R_0, R_1, ... R_n = Resistor value per circuit diagram (Ω)

If you want to use the 25kΩ feedback resistors in the INA115 for the R_0s, you can use the circuit shown in Figure 2. Keep in mind that the gain accuracy and gain drift will be limited by the internal feedback resistors. The 25kΩ feedback resistors have a tolerance of ±0.5% with a temperature coefficient of resistance drift (TCR) of up to 100ppm/°C. In the INA131, PGA204 and PGA205, resistor matching and TCR tracking of the resistors on the die give typical gain error and drift of 0.01% and 5ppm/°C.

GAINS (V/V)	R_0 (Ω)	R_1 (Ω)	R_2 (Ω)	R_3 (Ω)	R_4 (Ω)
2, 4, 8, 16	25k	12.4k	6.19k	3.09k	6.19k
10, 20, 50, 100	25k	1.4k	825	280	562
3dB, 6dB, 9dB, 12db	25k	17.8k	12.4k	8.87k	43.2k
10, 100, 1k, 10k	100k	10k	1k	100	22.1
10, 100, 200, 500	49.9k	4.99k	280	165	221
100, 200, 400, 800	100k	511	255	127	255

NOTE: Nearest Standard 1% Resistor Values.

TABLE II. Examples of Resistor Values for Selected Gains—Figure 1 and 2 Circuits.

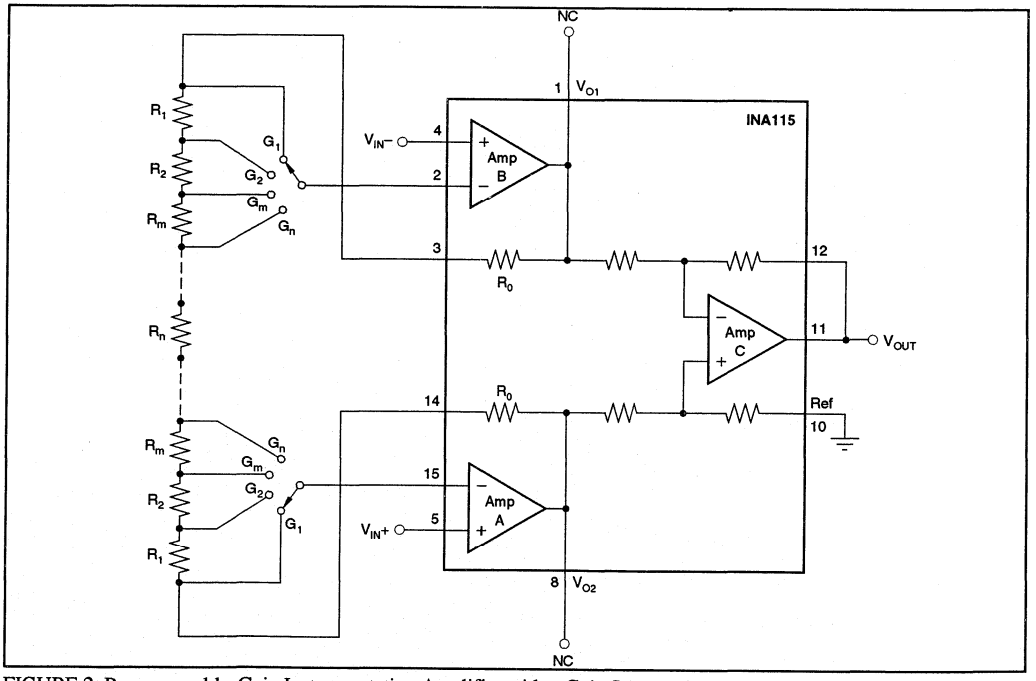


FIGURE 2. Programmable-Gain Instrumentation Amplifier with n Gain Steps and Lowest Gain > 1V/V. This circuit uses the 25kΩ feedback resistor in the INA115 for R_0 of Figure 1.

If you want a PGIA with n gains and the first gain is unity (1V/V), use the following relationships and the circuit shown in Figure 3.

RESISTOR VALUES FOR PGIA WITH n GAINS AND LOWEST GAIN = 1V/V

$R_0 = 0$

R_1 = Your choice (e.g. 25kΩ)

R_1 = 25kΩ when using the internal feedback resistors in the INA115 (see Figure 4)

$$R_2 = \frac{R_1 (G_2 - G_3)}{G_3 (1 - G_2)}$$

$$R_3 = \frac{G_2 R_1 (G_3 - G_4)}{G_3 G_4 (1 - G_2)}$$

$$\vdots$$

$$R_m = \frac{G_2 R_1 (G_m - G_{m+1})}{G_m G_{m+1} (1 - G_2)}$$

$$R_n = \frac{2 G_2 R_1}{G_n (G_2 - 1)}$$

Where:

G_m = Intermediate gain (V/V)
G_n = Highest gain (V/V)
$R_0, R_1, \ldots R_n$ = Resistor value per circuit diagram (Ω)

If you want to use the 25kΩ feedback resistors in the INA115 for the R_1s, you can use the circuit shown in Figure 4. Keep in mind the gain accuracy and gain drift limitations discussed previously.

An actual example of a four-gain digitally programmable IA is shown in Figure 5. It uses a four-channel differential multiplexer (MUX) for gain switching.

GAINS (V/V)	R_0 (Ω)	R_1 (Ω)	R_2 (Ω)	R_3 (Ω)	R_4 (Ω)
1, 2, 4, 8	0	25k	12.4k	6.19k	12.4k
1, 8, 64, 512	0	25k	3.09	392	113
1, 2, 5, 10	0	25k	15k	4.99k	10k
1, 10, 100, 1k	0	49.9k	4.99k	499	110
1, 10, 100, 200	0	20k	2k	110	221
0dB, 3dB, 6dB, 9dB	0	24.9k	17.8k	12.4k	60.4k

NOTE: Nearest Standard 1% Resistor Values.

TABLE III. Examples of Resistor Values for Selected Gains—Figure 3 and 4 Circuits.

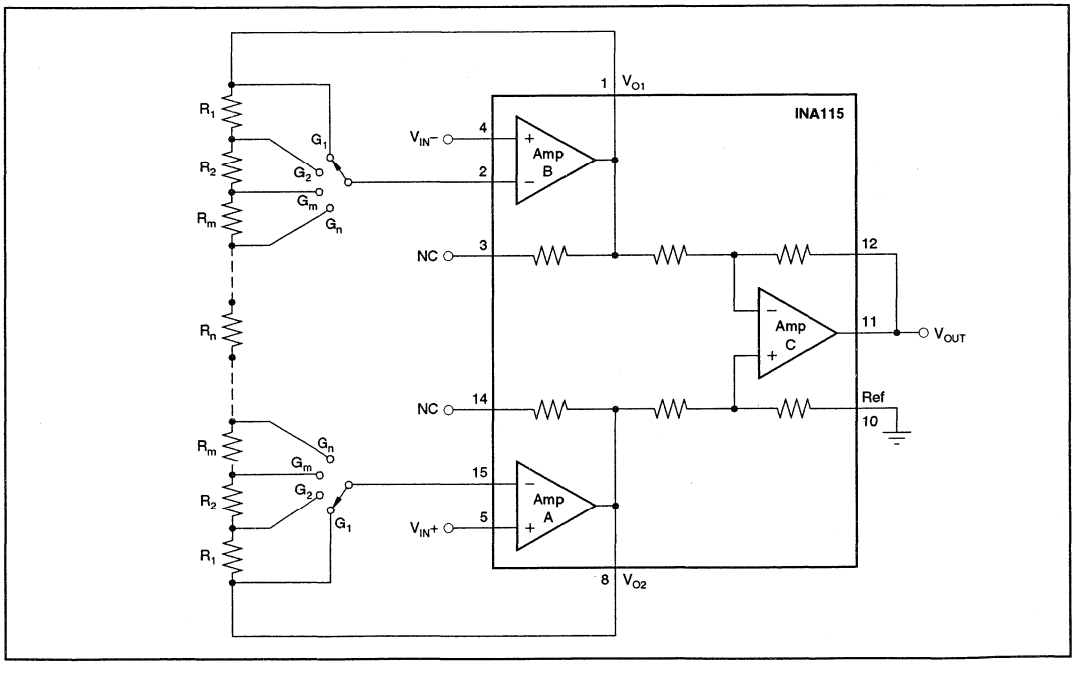


FIGURE 3. Programmable-Gain Instrumentation Amplifier with n Gain Steps and Lowest Gain = 1V/V.

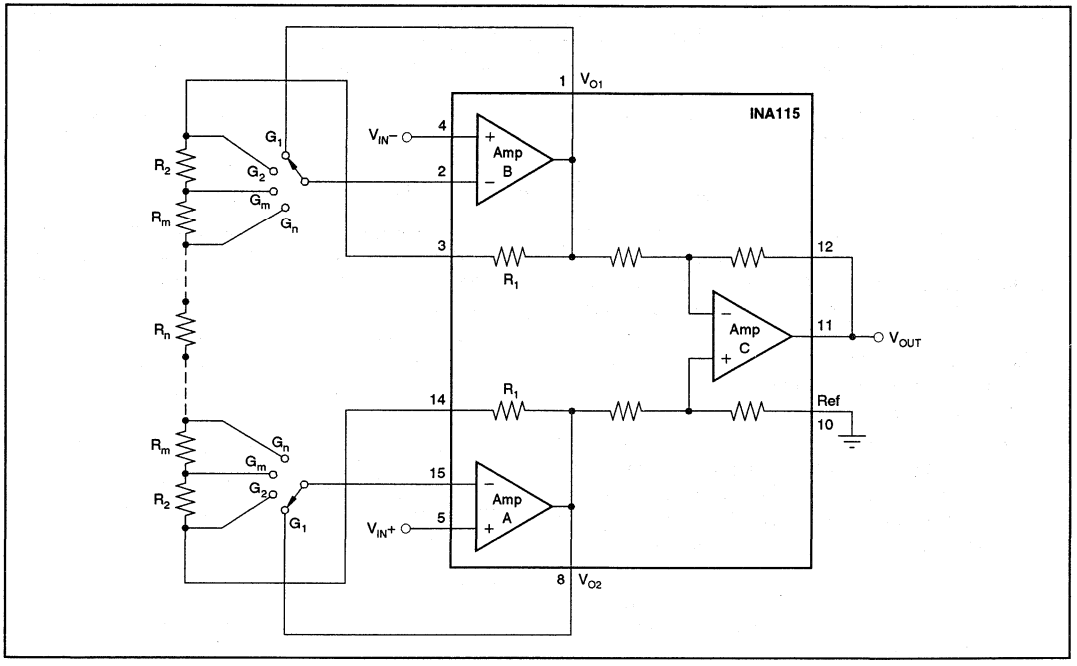
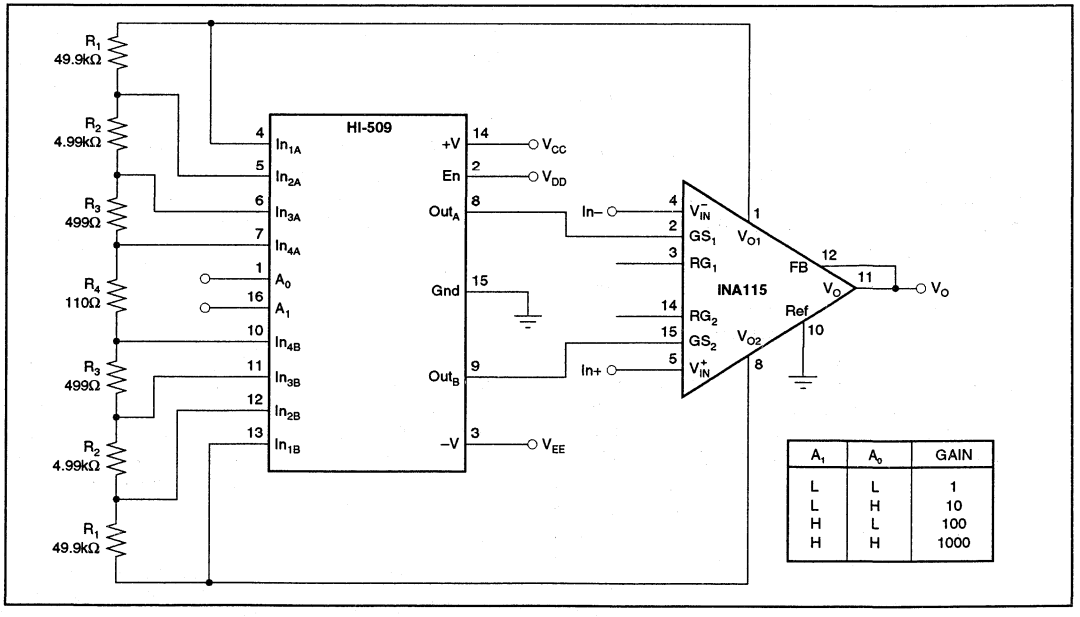


FIGURE 4. Programmable-Gain Instrumentation Amplifier with n Gain Steps and Lowest Gain = 1V/V. This circuit uses the 25kΩ feedback resistor in the INA115 for R_1 of Figure 3.



A_1	A_0	GAIN
L	L	1
L	H	10
H	L	100
H	H	1000

FIGURE 5. Programmable-Gain Instrumentation Amplifier Example with Four Gain Steps and Lowest Gain = 1V/V.

BURR-BROWN® APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

USE LOW-IMPEDANCE BRIDGES ON 4-20mA CURRENT LOOPS

By R. Mark Stitt (602) 746-7445 and David Jones

If you need more transducer excitation current than is available on a standard 4-20mA 2-wire current loop, consider a 3-wire transmitter. A 2-wire 4-20mA transmitter uses the same two wires for signal and power. Part of the 4mA minimum loop current is used to power the transmitter circuitry. The remaining current can be used for transducer excitation. In some applications even the entire 4mA is not enough for transducer excitation.

Exciting a low-impedance bridge (such as a 350Ω bridge) often requires more current than is normally available from a 2-wire 4-20mA current loop. A 350Ω bridge excited with a 10V reference requires more than 28mA. An easy way to solve this problem is to use a 3-wire transmitter such as the XTR110.

The XTR110 3-wire transmitter is similar to a 2-wire transmitter, except that one of the two wires is connected to ground and a third (power supply) wire is added. With external power available at the transmitter, it is easy to interface to low-impedance bridges. The XTR110 contains an on-board precision 10.0V reference for sensor excitation. The reference has a sense connection so that its output can be easily boosted.

THE COMPLETE BRIDGE TO CURRENT-LOOP CIRCUIT IS SHOWN IN FIGURE 1

A series-pass transistor, Q_1, boosts the XTR110's 10.0V reference output-current to drive the bridge. Using an external pass transistor allows high output-drive without overheating the XTR110. To improve reliability you may need to heat-sink Q_1, especially for high ambient temperatures.

An INA114 precision instrumentation amplifier is used to amplify the bridge output to drive the XTR110 low-impedance input. The INA114 is operated single-supply from the 10V reference to eliminate any error due to power-supply changes. The XTR110 is connected so a 1V to 5V input on pin 5 produces a 4-20mA output. A voltage divider buffered by an OPA177 drives the INA114 *reference* pin. With 3V on the *reference* pin, the INA114 output is 3V with the bridge in balance. This produces a 12mA (mid-scale) XTR110 output with the bridge in balance. If you want to use the bridge in a unipolar mode, the resistor divider can be set to put either 1V or 5V on the INA114 *reference* pin to produce either a 1V or 5V INA114 output at bridge balance. In any case, select the INA114 gain-set resistor for 4V INA114 output change with ±full-scale bridge output.

A P-channel enhancement-mode MOSFET, Q_2, is used to drive the 4-20mA output current. Using an external FET to drive the output current improves precision by eliminating thermal feedback. If an internal driver were used, the signal-dependent power change due to the 4-20mA current change would result in relatively large nonlinearity in the transfer function.

Burr-Brown offers a complete line of 2-wire and 3-wire current loop transmitters and receivers.

XTR101

General purpose two-wire 4-20mA current-loop transmitter. This transmitter has an instrumentation amplifier input and two 1mA current sources for transducer excitation and offsetting.

XTR103

Two-wire RTD 4-20mA current-loop transmitter with 9V compliance. Similar to XTR101, but with internal linearization circuitry for direct interface to RTD Resistance Temperature Detectors. The XTR103, along with an RTD, forms a precision temperature to 4-20mA current loop transmitter. Along with an RTD, the XTR103 can achieve better than 0.1% span linearity over a –200°C to +850°C temperature span.

XTR104

Two-wire bridge 4-20mA current-loop transmitter with 9V compliance. Similar to XTR101, but with shunt regulator and linearization circuitry for direct interface to high-impedance strain-gauge and Wheatstone bridges. The XTR104 can provide better than 0.1% span linearity from bridges with uncorrected linearity in excess of 2%.

XTR110

Three-wire 4-20mA current-loop transmitter. Essentially a precision, single-supply voltage-to-current converter with an internal 10.0V reference and input resistor network for span offsetting. Various input-output ranges are available by pin strapping so that 0 to 5V or 0 to 10V inputs can be used to get 0 to 20mA or 4 to 20mA outputs for example.

RCV420

Self-contained 4-20mA receiver. Conditions and offsets 4-20mA input signals to give a precision 0-5V output. Contains precision voltage reference, 75Ω precision sense resistor and ±40V common-mode input range difference amplifier. The RCV420 has a total combined span and zero error of less than 0.1%—adjustable to zero.

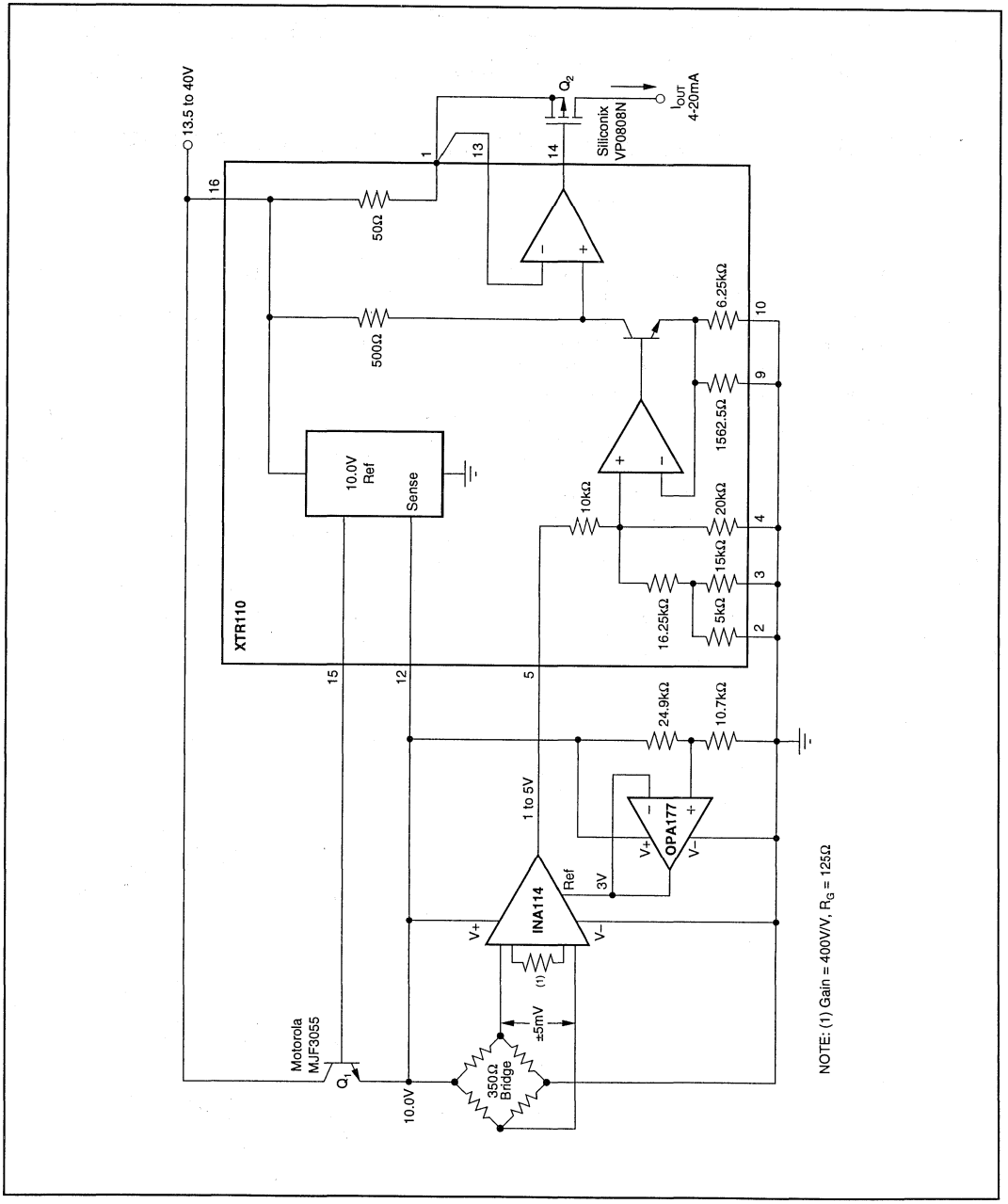


FIGURE 1. Complete 350Ω Bridge to 4-20mA Current-Loop Transmitter Uses XTR110 3-Wire Current Loop Transmitter and INA114 Precision Instrumentation Amplifier Operating in a Single-Supply Mode.

BURR-BROWN® APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

PRECISION IA SWINGS RAIL-TO-RAIL ON SINGLE 5V SUPPLY

By R. Mark Stitt (602) 746-7445

You can combine a precision instrumentation amplifier (IA) and an inexpensive CMOS op amp to get the best of two worlds—the precision of a bipolar IA and 5V single-supply operation. Using the INA131 gives 50µV max voltage offset, 0.25µV/°C max offset drift, and 110dB min common-mode rejection. How close the output swings to the power supply rail depends on which "rail-to-rail" CMOS op amp you use. With a TI TL2272 you can expect the output to swing within 100mV of the rails.

The circuit is shown in Figure 1. INA131 is fixed Gain = 100 IA specified to operate on power supplies as low as ±2.25V. Its output can swing ±1.25V on ±2.5V supplies. Adding a gain-of-2 "rail-to-rail" CMOS op amp, A_4, inside the feedback loop boosts output swing to ±2.5V (0 to 5V on a single 5V supply). Because the CMOS op amp is inside the feedback loop, its errors are divided-down by the loop gain of A_3 in the INA131 so they contribute negligible error to the composite amplifier.

The gain of the CMOS amplifier is set by R_1, R_2, and R_3.

$$\text{Gain} = 1 + \frac{R_1 \bullet R_2 + R_2 \bullet R_3}{R_1 \bullet R_3}$$

With the values shown, Gain ≈ 2V/V. Remember, since A_4 is in the INA131 feedback loop, its exact gain is unimportant. The INA131 will still have a precise gain of 100V/V ±0.024%.

Using the R_1, R_3 divider to set the gain forces the INA131 output swing to be centered midway between the +5V supply and ground for rail-to-rail output swing.

Compensation capacitor, C_1, provides high-frequency feedback around A_4 to assure loop stability. It is important to choose A_4 with at least 2MHz small-signal bandwidth for good loop stability.

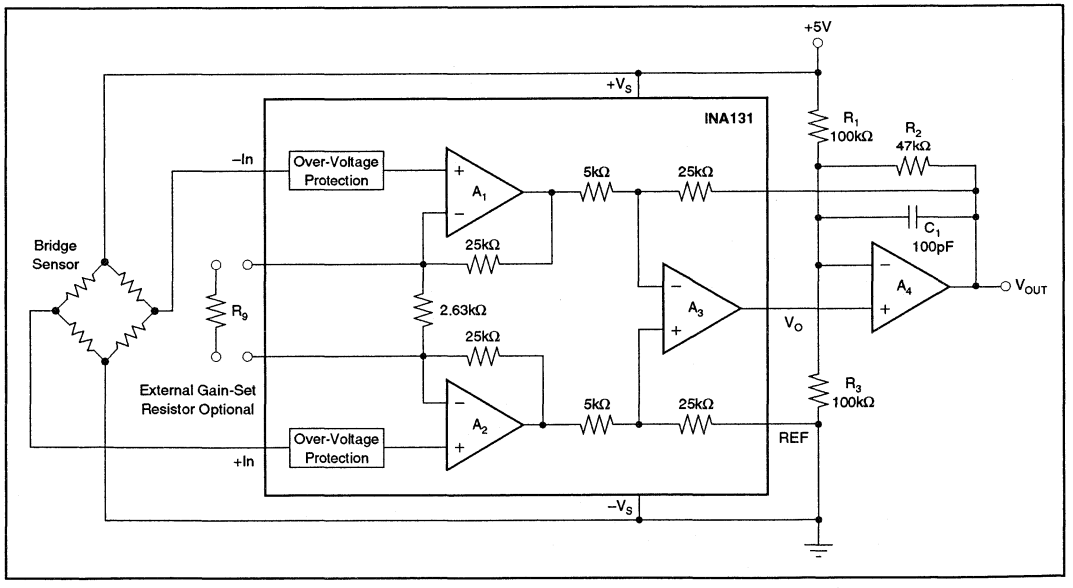


FIGURE 1. Adding a "Rail-to-Rail" CMOS Op Amp in its Feedback Loop Allows the INA131 Output to Swing Rail-to-Rail on a Single 5V Supply.

Figure 2 shows the output swing of the composite IA. In this triple exposure, the output sine-wave signal is superimposed with the ground rail and +5V rail.

Although the output of the composite IA will swing rail-to-rail, its inputs will not function at ground. This is not a problem for the bridge application shown. In this application, the bridge is biased from the +5V power supply to ground. With a balanced bridge, the IA inputs are at 2.5V (midway between the +5V power supply and ground). Because the INA131 uses a gain-of-five difference amplifier, the inputs to A_3 are at 2V when the INA131 inputs are at 2.5V. This allows the INA131 to operate properly with common-mode input voltages from 2V to 3V.

As with most rail-to-rail op amps, the TLC2272 is a dual op amp. If the second op amp is not used elsewhere, it can be used for filtering or added gain.

Gain can also be increased by connecting an optional gain-set resistor, R_G, as shown in Figure 1. Gain-set resistors in the INA131 are trimmed for precise ratios, not to absolute values. Absolute accuracy of the internal gain-set resistors is ±40%. To compensate for this tolerance, the value of the external gain-set resistor may need to be adjusted from device to device. Nominal gain with an external R_G can be calculated as follows:

$$\text{Gain} = 100 + \frac{250\text{k}\Omega}{R_G}$$

Where:

R_G is the external gain-set resistor (Ω)
Accuracy of the 250kΩ term is ±40%.

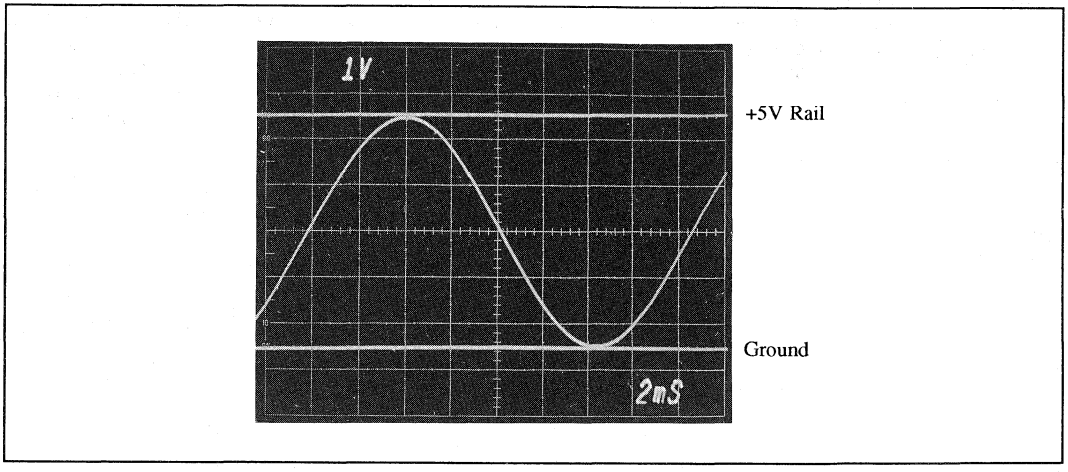


FIGURE 2. Triple Exposure Showing Rail-to-Rail Output Swing of Composite Precision IA.

BURR-BROWN® APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

LEVEL SHIFTING SIGNALS WITH DIFFERENTIAL AMPLIFIERS

by David Jones, (602) 746-7696

The INA105 is a unity gain differential amplifier consisting of a premium grade operational amplifier and an on-chip precision resistor network. The self-contained INA105 makes it ideal for many applications. One such application is precision level shifting.

Figure 1 shows a general case of a unity gain differential amplifier that performs a signal level shift proportional to the voltage V_{SHIFT} appearing on pin 3 of the OPA27. An operational amplifier is used to drive the INA105's "Ref" pin (pin 1) with a low impedance source to preserve true differential operational of the INA105.

A basic understanding of the circuit operation can be gained by considering the INA105 as a three input summing amplifier. The voltage transfer function is then $E_{OUT} = E_2 - E_1 + V_{REF}$. As this relation shows, the output will respond to a difference signal and algebraically add the voltage at the "Ref" input. Therefore, V_{REF} may take on any arbitrary value that will not saturate the INA105 amplifier's output. In the case of the circuit in Figure 1, $V_{REF} = V_{SHIFT}$, yielding an output of $E_O = E_2 - E_1 + V_{SHIFT}$.

Precision fixed level shifting can be easily accomplished by the use of a voltage reference source such as the REF102. A REF102 used with an additional INA105 can be used to provide an accurate, low drift, +5V reference to drive the "Ref" pin of the differentially connected INA105 as shown in Figure 2. If, for example, the input signal is a bipolar ±5V signal, the output will be level shifted to a unipolar 0-10V signal. The same reference circuit also has –5V available and may thus be used for the opposite conversion from unipolar 0-10V to bipolar ±5V signals. (Request PDS-1018 for INA105 and PDS-900 for REF102.)

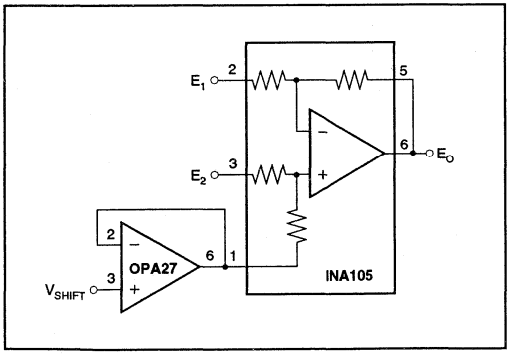


FIGURE 1. Level Shifting Circuit Using the INA105's V_{REF} Pin.

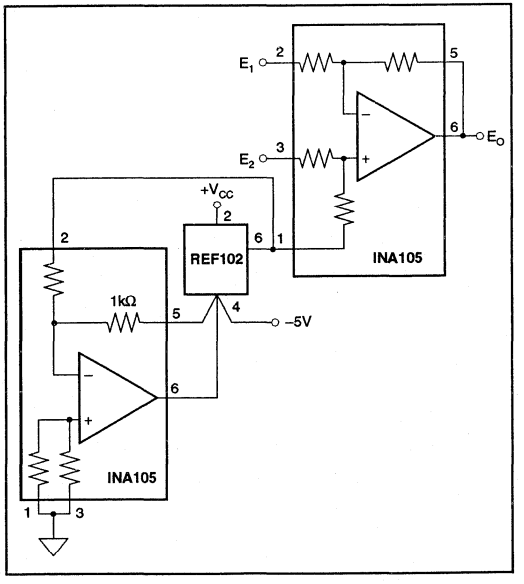


FIGURE 2. Precision Level Shift Circuit from a Fixed Voltage Reference.

BURR-BROWN®
APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

SIMPLE CIRCUIT DELIVERS 38Vp-p AT 5A FROM 28V UNIPOLAR SUPPLY

by Jason Albanus (602) 746-7985

Since the first analog IC requiring bipolar supplies was developed, people have been trying to operate them from unipolar supplies. Not only do the "headroom" ($V_S - V_{OUTMAX}$) requirements come into play, but with a unipolar supply typically come unipolar outputs. To get bipolar output swings from a unipolar supply, drive the load differentially and create a reference signal which can be used a "pseudo ground" for amplifier and input signal reference. **This circuit topography requires that your signal be elevated to $V_S \div 2$.**

The INA105 is a precision unity gain differential amplifier, and as a low cost monolithic circuit, it offers high reliability and accuracy. With an initial offset voltage of 50µV, gain error of 0.005%, and small signal bandwidth of 1MHz, the INA105 makes an ideal amplifier for creating this pseudo ground. The OPA2541 is a dual power operational amplifier capable of operation from power supplies up to ±40V (or a single, unipolar 80V) at output currents of 5A continuous. With two monolithic power amplifiers in a single package it provides unequaled functional density, and provides the means to deliver differential outputs at high power. By using the INA105 to create the pseudo ground, and the OPA2541 to drive 5A loads differentially, the circuit in Figure 1 can be developed. At 5A output current, the OPA2541 requires a typical headroom of 4.5V, and as configured, output voltage swings of $2V_S - 18V$ (peak-to-peak) can be achieved. The output swing can be calculated by realizing that when one of the amplifiers reaches its positive output limit ($V_S - V_{HEADROOM}$), the other amplifier should reach its negative output limit ($0V + V_{HEADROOM}$). This creates a voltage swing

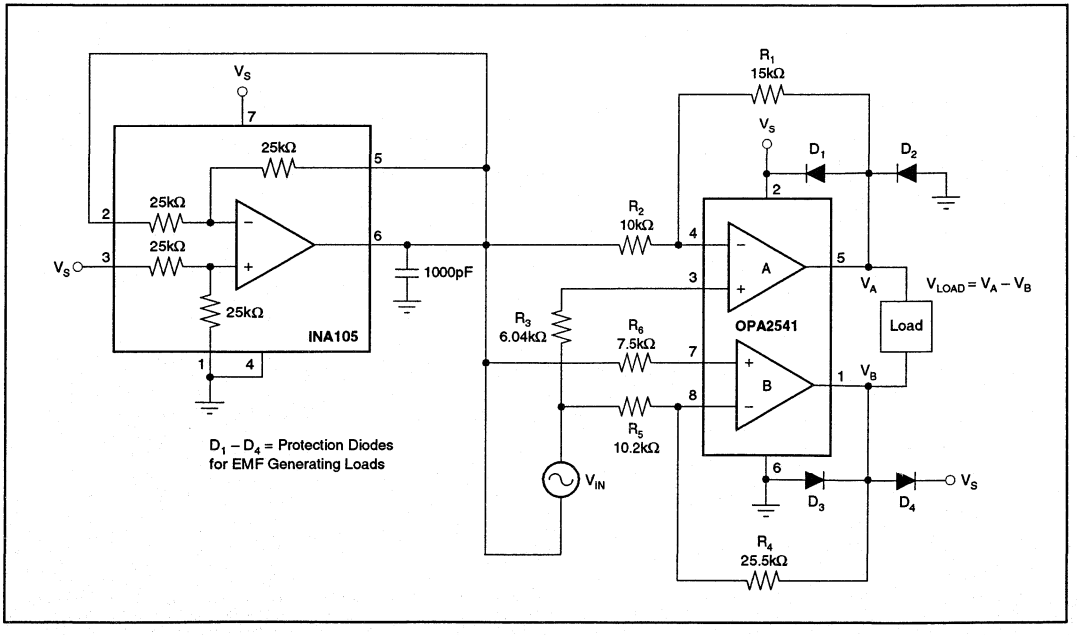


FIGURE 1. Single Supply, Bipolar Output Swing for Floating Signal Source.

of $V_S - 2V_{HEADROOM}$. This is then multiplied by two, when the input signals reverse polarity so do the output signals which are referenced to the pseudo ground. This causes the peak-to-peak output voltage to be $2V_S - 4V_{HEADROOM}$. For standard 28V systems, this means that you can see output swings of 38Vp-p at 5A (see *Equations for detailed explanation*). When only driving 500mA the headroom is typically only 3.2V, and output swings of $2V_S - 12.8V$ are realizable. This means that from the same 28V supply, the peak-to-peak output is 43.2V. By using the maximum rated supply of 80V, a peak-to-peak output of 142V with load currents of 5A can be realized.

Although the OPA2541 is capable of operating with supply voltages up to 80V, the INA105 is limited to an overall power supply voltage of 36V. If higher supply voltages are required, an amplifier such as the OPA445 and a precision resistor network should be utilized for the pseudo ground.

Equations:

$$
\begin{aligned}
V_G &= \text{Pseudo ground voltage} \\
&= V_S/2 \\
V_{IN}' &= V_G + V_{IN} \\
V_{LOAD} &= \text{Differential voltage across the load} \\
&= V_A - V_B \\
A_V &= 1 + (R_1/R_2) \\
&= R_4/R_5 \\
V_A &= V_{IN}' \{1 + (R_1/R_2)\} - V_G (R_1/R_2) \\
&= V_{IN}' (A_V) - V_G (A_V - 1) \\
&= V_{IN} (A_V) + V_G \\
V_B &= -V_{IN}' (R_4/R_5) + V_G \{1 + (R_4/R_5)\} \\
&= -V_{IN}' (A_V) + V_G (A_V + 1) \\
&= -V_{IN} (A_V) + V_G \\
V_{LOAD} &= V_A - V_B \\
&= \{V_{IN} (A_V) + V_G\} - \{-V_{IN}(A_V) + V_G\} \\
&= V_{IN} (2A_V)
\end{aligned}
$$

BURR-BROWN® APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

PARTIAL DISCHARGE TESTING: What It Is and What It Means

With the introduction of the ISO120 and ISO121, Burr-Brown also introduced partial discharge testing of analog isolation components. We have received several requests for an explanation of the test, what it provides for us and our customers, and how it relates to the more traditional test for isolation voltage ratings. What follows is information about the older test method and what it accomplished, partial discharge, how we test for it, and a comparison of similar products tested using the different methods. Some of this material appears in the ISO120/121 PDS, but bears repeating to give you the whole story.

ISOLATION VOLTAGE RATINGS— WHAT DO THEY MEAN?

An isolation voltage rating is a statement about the *level of voltage* a device can *withstand for long periods of time* with a *high confidence* that the *barrier will not break down.* In the initial development of a part, basic physical and materials design determines the desired rating and long-term, high-voltage life testing of the part verifies it. However, it's impractical to long-term life test every isolation amplifier or power supply that we ship. We need a test that will verify that the part can withstand its rated voltage and give assurance that it will survive that much voltage for long periods of time.

STRESS TESTING

One way to do that is to overstress the part briefly (i.e., subject the part to levels significantly above its *rated* voltage) and then test the part at rated continuous voltage for a short period of time. Alternatively, one can test the part at the overstress voltage for a fixed time, such as 60 seconds.

We have used both methods, depending on the division producing the part and its intended market applications. In either case, the philosophy is something like life testing. In much the same way as accelerated life testing is used to identify infant mortality problems with electronic components, the current method of dielectric withstand testing is used to identify problems with dielectric materials used in isolation circuits.

The choice of overstress voltage is an important one. Many isolation applications see not only the continuous voltage, but also experience transient voltages. Historically, we have used an overstress voltage, V_{TEST} = (2 x Continuous Rating) + 1000V. This choice is used in some UL specifications and is appropriate for conditions where systems transients are not well defined.

However, there are other methods of testing for high-voltage breakdown and some have been around a long time. In 1944, Austin and Hacket published *Internal Discharges in Dielectrics: Their Observation and Analysis.* Since that time, the phenomenon they described, and now termed partial discharge, has steadily gained wider acceptance in the evaluating dielectric materials. For a number of years, the manufacturers of power distribution equipment have used a measurement of RF noise to detect the ionization that precedes high-voltage breakdown. This method is OK for large transformers or similar equipment, but it has not been sensitive enough for small components such as those used in Burr-Brown's isolation amplifiers and power supplies.

Partial discharge testing is similar in concept to the RF noise detection, and recent advances in test equipment and testing standards now make it possible to use this much more sensitive method with our products. Just as Burr-Brown's products are at the forefront of technology, our use of partial discharge testing for some products should be seen as being on the leading edge of testing dielectric materials. We are not abandoning the older, more accepted test standards. However, in preparing to meet the demands for what we believe to be a world-class testing standard, we would like to tell you something about partial discharge, how it's tested, and why we believe it will become the recognized superior method of testing dielectric materials.

PARTIAL DISCHARGE

When an isolation barrier has a defect such as an internal void, the defect will display localized ionization when exposed to high voltage. This ionization starts at one voltage and stops at a lower voltage. These are called the inception and extinction voltages. As high voltage is applied to the barrier, voltage will also build up across the void. When the inception voltage is reached, the void ionizes, shorting itself out. When the voltage across the void drops below the extinction voltage, ionization ceases.

This action redistributes charge within the barrier and is known as partial discharge. If the barrier voltage continues to rise, another partial discharge cycle begins. If the barrier voltage is AC and is large enough, partial discharge cycles will repeat many times during the positive and negative peaks. If the ionization begins and continues, it can damage the barrier, leading to failure. If the discharge does not occur, the barrier receives no damage.

The inception voltage of the individual voids tends to be constant. Therefore, the total charge redistributed within the

barrier is a very good indicator of the number of the voids and their likelihood of becoming a failure. Setting a very low limit on the allowable partial discharge in testing gives a very high degree of confidence that HV failure will not occur.

PARTIAL DISCHARGE AND BARRIER EVALUATION

The barrier itself displays an inception and an extinction voltage. The bulk inception voltage varies with the type of insulation, its thickness, and the number of defects. It directly establishes the maximum voltage that can be applied across the test device before destructive partial discharge can begin. Measuring the bulk inception voltage on each part provides an absolute maximum rating for each device.

Measuring the bulk extinction voltage can also provide a lower, more conservative voltage from which to derive a safe continuous rating. In theory, directly from these two measurements one could then specify the maximum transient voltage and continuous voltage ratings. In practice, testing to determine the inception voltage, and de-rating from the inception voltage by a factor related to transients determines the continuous rated voltage.

PARTIAL DISCHARGE TESTING IN PRODUCTION

Once the continuous rating is established, a convenient 100% production test is needed. It should provide firm GO/NOGO information, be very sensitive, be non-destructive and, for economic reasons, be very short. These are the benefits of partial discharge testing! In the last couple of years, manufacturers have produced equipment which can reliably test for very low values of partial discharge, and some standards are being developed to specify test methods. The first such standard that we are aware of was developed by VDE in Germany and applies to testing of optocouplers. We have adopted the method described in VDE 0884 to test for partial discharge in our production tests. The test is conducted in two stages. First, a one second test at rated voltage checks for leakage current. Another one second test checks for partial discharge at 1.6 times rated voltage; the level of partial discharge must be <5pC (5×10^{-12} Coulombs). The 1.6 multiplier takes into account the ratio of transient voltage to continuous rating and is specified in the VDE standard.

Internal Burr-Brown test procedures allow two retries if a part fails the initial test. Sometimes ozone generated by the test voltage is enough to trigger the GO/NOGO circuit, so we clear out the test chamber before retest. If failure occurs a second time, the part is cleaned and retested. Fingerprints on the part can also trigger the GO/NOGO. If it still fails, we scrap it.

OTHER ADVANTAGES OF PARTIAL DISCHARGE TESTING

Not only can this test method provide far more qualitative information about stress withstand levels than did previous stress tests, but it can also provide *quantitative* measurements upon which quality assurance and control measures could be based. Should we ever find it desirable to do so, sampled information on PD, inception and extinction voltages would be ideal information upon which to base SPC for our iso manufacturing process. Please understand that we are ***not*** currently working on SPC for this aspect of the iso product line, but PD testing does offer this advantage should we decide to make use of it.

In addition to the potential for use in SPC, and for the same reasons, PD testing of products in development improves our knowledge of the new product and its manufacturing methods. It has become a powerful development evaluation tool, and, we believe, has helped us develop better, more capable products. Using it in production testing allows good correlation with development test results and proves invaluable in investigating manufacturing problems that can arise with any new product.

COMPARISON OF ISO TESTING—NEW AND OLD

The following chart summarizes the differences in time and test voltages for the two test methods. Some of you have expressed feelings that the new test levels and times will leave customers concerned about their validity and application in areas where agency certification (UL, for example) is a must.

Of most concern, from the feedback we received, was compliance of PD testing with UL544 for medical equipment. Most people are familiar with the UL requirement that an OEM test its finished product at 2500Vrms for 60 seconds. This test is required *only* for patient-connected equipment and *not* for all medical equipment. What most people do not know is that UL allows a choice of *two* conditions for this test. The first is 2500Vrms/60s, known as Condition A, and the second is Condition B, requiring a 3000Vrms/1s test. Paragraph 42.2 of UL544 (Revised 1985) allows either test in 100% production testing. Please note that we test the ISO121 at 5600Vrms for one second; we easily conform to Condition B. Since we demonstrate no PD at that voltage, we will easily pass any 2500V test as well.

PRODUCT	ISO102	ISO120	ISO106	ISO121	UNITS
Rated Voltage	1500 2121	1500 2121	3500 4950	3500 4950	Vrms Vpeak
Test Voltage	4000 5656	2500(1) 3535	5697(2) 8000(2)	5600 7920	Vrms Vpeak
Test Time At Max Voltage	10	1	10	1	s
Time At Rated Voltage	60	1(3)	60	1(3)	s

NOTES: (1) We cheat a little here, this is 1.67 times rated, not 1.6 times rated. (2) Upper limit of our production test equipment for this test method. (3) Proceeds PD test; checks for barrier leakage current.

BURR-BROWN® APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

NOISE SOURCES IN APPLICATIONS USING CAPACITIVE COUPLED ISOLATED AMPLIFIERS

By Bonnie C. Baker (602) 746-7984

Noise is a typical problem confronting many isolation applications. Isolation products such as analog isolation amplifiers, optocouplers, transformers and digital couplers, are used in applications to transmit signals across a high voltage barrier while providing galvanic separation between two grounds. Burr-Brown's isolated analog amplifiers and digital couplers use one of three coupling technologies in their isolation products, each having its own set of advantages and disadvantages in noisy environments. These technologies are inductive coupling, capacitive coupling and optical coupling. Isolation amplifiers and digital couplers are used for a variety of applications including breaking of ground loops, motor control, power monitoring and protecting equipment from possible damage. An understanding of the design techniques used to transmit signals across the isolation barrier, as well as an understanding of the sources of noise, allows the users to quickly identify design and layout problems and make appropriate changes to reduce noise to tolerable levels.

Noise is defined in this application note as a signal that is present in a circuit other than the desired signal. This definition excludes analog nonlinearities which may produce distortion. As shown in Figure 1, there are three primary types of noise endemic to isolation applications, each with their own set of possible solutions. The first noise source is device noise. Device noise is the intrinsic noise of the devices in the circuit. Examples of device noise would be the thermal noise of a resistor or the shot noise of a transistor. A second source of noise that effects the performance of isolation devices is conductive noise. This type of noise already exists in the conductive paths of the circuit, such as the power lines, and mixes with the desired electrical signal through the isolation device. The third source of noise is radiated noise. Radiated noise is emitted from EMI sources such as switches or motors and coupled into the signal. This application bulletin will cover these three noise classifications as they relate to capacitive coupled isolation amplifiers.

THEORY OF OPERATION OF THE CAPACITIVE COUPLED ISOLATION AMPLIFIERS

The capacitive coupled isolation amplifiers are designed with an input and output section galvanically isolated by a pair of matched capacitors. A block diagram of this type of

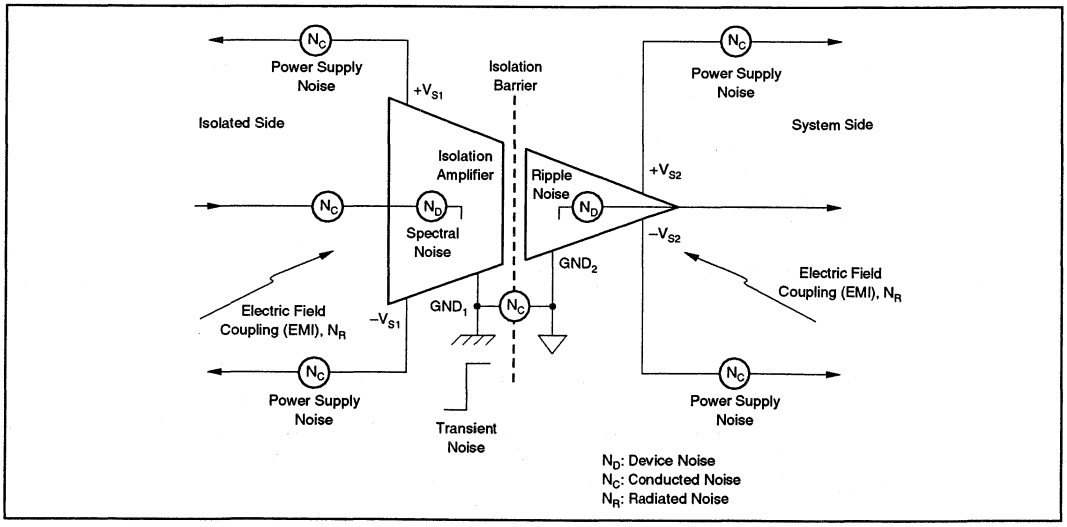
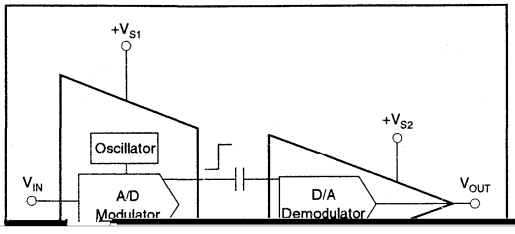


FIGURE 1. The Three Basic Types of Noise in Isolation Applications are Device Noise, Conducted Noise, and Radiated Noise.

isolation amplifier is shown in Figure 2. The capacitive coupled isolation amplifiers employ digital modulation schemes to transmit a differential signal across the isolation barrier. The modulation schemes used in the capacitive coupled isolation amplifiers are duty-cycle modulation or voltage-to-frequency, depending on the product. Both modulation schemes are basically voltage to time. An internal oscillator is used to modulate the analog input signal into a digital signal which is transmitted across the isolation barrier. Most capacitive coupled amplifiers (ISO103, ISO107, ISO113, ISO120, ISO121, ISO122), as shown in the block diagram in Figure 3, modulate the analog signal to a duty-cycle encoded signal; The remainder of the isolation amplifiers (ISO102 and ISO106), as shown in the block diagram in Figure 4, modulate the analog voltage to a frequency.



The modulated signal is transmitted to the other side of the isolation barrier through a pair of matched capacitors built into the plastic or ceramic package. The value of these capacitors varies from lpF to 3pF depending on the device. The resulting capacitor is simple and reliable by design.

After the modulated signal is transmitted across the isolation barrier, it is demodulated back to an analog voltage. The output section of the isolation amplifier detects the modulated signal and converts it back to an analog voltage by using averaging techniques. Most of the undesired ripple voltages inherent in the demodulation process is then removed.

DEVICE NOISE AND CAPACITIVE COUPLED ISOLATION AMPLIFIERS

Device noise is generated by the devices in the circuit. Examples of device noise generators would be a discrete resistor, which generates thermal noise, or an operational amplifier, which would generate 1/f noise, etc. Specifically, with Burr-Brown's capacitive coupled isolation amplifiers, there are two device noise specifications of consequence.

Ripple Noise

A by-product of the demodulation scheme for the duty-cycle

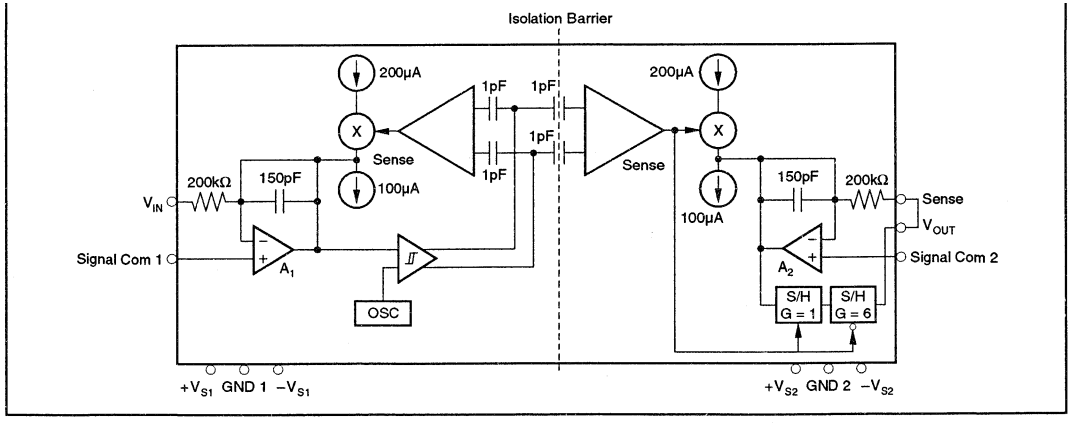


FIGURE 3. The Basic Block Diagram of the ISO103, ISO107, ISO113, ISO120, ISO121, and ISO122 Isolation Amplifiers, which use Duty-Cycle Techniques to Transmit Signal Across the Isolation Barrier.

This ripple voltage noise can easily be eliminated by using a low pass R-C or active filter at the output of the isolation amplifier as shown in Figure 6. This two-pole, unity-gain, Sallen-Key type filter is designed with a Q = 1 and a 3dB bandwidth = 50kHz. The OPA602 is selected to preserve DC accuracy of the ISO122. In Figure 6, the dynamic range of the ISO122 is changed from a typical 9-bit resolution to 11-bit resolution (see AB-023). The ISO102 and ISO106 isolation amplifiers have an active filter built into their outputs. This low pass filter provides a significant reduction in the ripple voltage. The remaining noise at the output of the isolation amplifier is spectral noise. If the ripple noise of the isolation amplifier is sufficiently reduced, the spectral noise will begin to dominate.

Spectral Noise

The spectral noise, or wideband noise, is the second type of isolation amplifier device noise. This noise is generated by the jitter of the modulation process. In the case of the ISO102 and ISO106, the jitter is dominated by the time uncertainty of the one-shot. With the ISO103, ISO113 and ISO107 the jitter noise is dominated by the translation of voltage noise in the comparator. Spectral noise can be reduced by reducing the signal bandwidth, or again using a low pass filter at the output of the isolation amplifier. Another method of reducing the noise contribution from spectral noise as well as the ripple voltage noise is to use a pre-gain stage to the isolation amplifier. This technique is shown in Figure 7. By gaining the signal before it is transmitted across the isolation barrier, the signal-to-noise ratio will be improved.

CONDUCTIVE NOISE AND ITS EFFECT ON ISOLATION AMPLIFIER SIGNALS

The second source of noise, conductive noise, can be coupled into the signal path through the three paths as shown in Figure 8. Noise on the power supply lines is coupled into the signal through the supply pins and eventually to the signal path. Noise coming from the input of the isolation amplifier is transmitted directly across the barrier. And finally, a fast change in the voltage difference between the grounds of the isolated system can corrupt the signal and in some cases give an erroneous output.

Power Supply Noise

Noise on the power supply lines can be coupled into the isolation amplifier through the supply pins. Isolation amplifiers require isolated supplies, typically DC/DC converters. DC/DC converters utilize high-frequency oscillators/drivers to transmit voltage information across a transformer barrier. The output stage of the DC/DC converters rectify, filter and in some instances regulate the output voltage. The output voltage has the desired DC component as well as remnants of the switching frequency in the form of a complex ripple voltage. The DC/DC converter regulation (or lack there of) and switching frequency can have an effect on the performance of the isolation amplifier. In the cases where the isolation amplifier is self-powered (ISO103, ISO113, and ISO107), the DC/DC converter is synchronized with the isolation amplifier oscillator, however, it is unregulated. The system power supply performance should be evaluated and possibly a regulator chip added to the circuit on the system

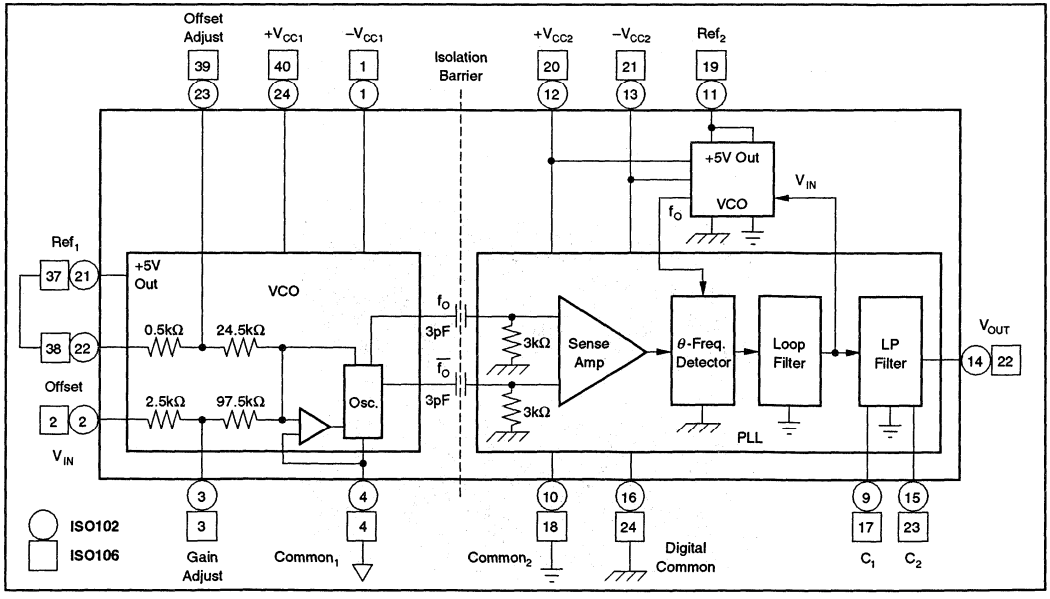


FIGURE 4. The Basic Block Diagram of the ISO102 and ISO106, Isolation Amplifiers, which use Voltage-to-Frequency Modulation Techniques to Transmit Signal Across the Isolation Barrier.

side. The isolation amplifiers that are not self-powered (ISO102, ISO106, ISO120, ISO121, and ISO122) require power be supplied by an external DC/DC converter or a battery.

In the case where the noise on the power supply line is less than the bandwidth of the isolation amplifier, the noise manifests itself as a small signal offset voltage. The magnitude of this error is specified in the data sheets of the isolation amplifiers as power supply rejection (PSR). Usually the contribution of a power supply rejection error is less than the ripple voltage that is generated by the demodulation process mentioned above.

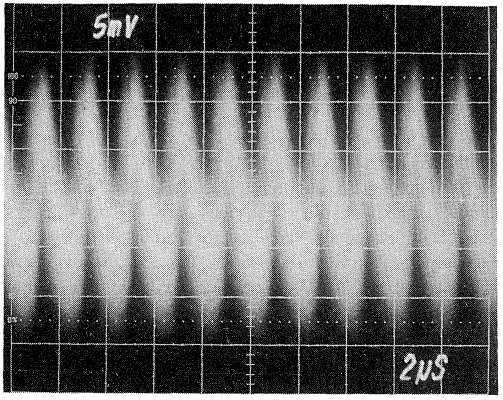
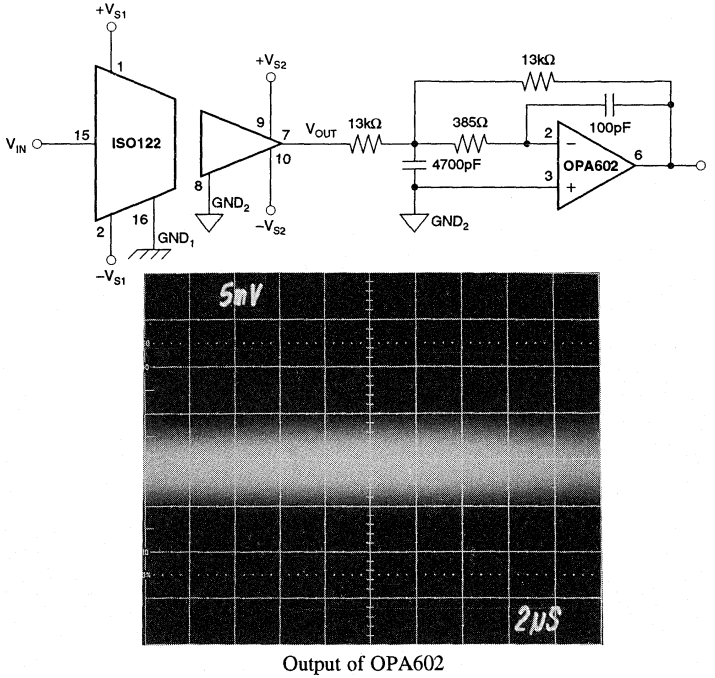


FIGURE 5. The Unfiltered Output of the ISO122 Isolation Amplifier Showing Approximately a 20mVp-p Output Ripple.

Power supply noise greater than the bandwidth of the isolation amplifier can come from several sources. Some of these sources can be the DC/DC converter switching frequency, switching noise from digital logic, switching noise from motors, or from the oscillator used in the isolation amplifier, to name a few. It is easy to assume that the isolation amplifier will filter out noise that is greater than its own bandwidth. That assumption is erroneous, because of aliasing between the power supply noise and the isolation amplifier's own oscillator.

To illustrate this point, refer to the performance curve from the ISO122 data sheet shown in Figure 9. The x-axis represents the power supply noise frequency. The left y-axis represents the ratio between voltage out to supply voltage in. The right y-axis represents the frequency of the output signal generated by the aliasing effect. As illustrated, if a supply line has a switching frequency of 750kHz, there will be a noise ripple contribution at the output of the ISO122 of about –33dBm and the frequency component of that noise will be 250kHz, which can easily be filtered using methods illustrated in Figure 6. If the supply line has a switching frequency noise of 900kHz, there will be a noise ripple



Output of OPA602

FIGURE 6. The ISO122 Isolation Amplifier with a Two-Pole, Low Pass Filter to Reduce Ripple Voltage Noise.

contribution at the output of the ISO122 of about –20dBm with a frequency component of 50kHz. Since the typical bandwidth of the ISO122 is 50kHz, this aliased noise will be difficult to filter without effecting the signal bandwidth.

A danger zone for the power supply switching frequency noise in this example is a frequency band of ±50kHz around 500kHz and multiples of 500kHz. This is because the ISO122's bandwidth is 50kHz and the modulation/demodulation oscillation frequency for the ISO122 is 500kHz. To complicate matters further, a DC/DC converter ripple voltage will never have the frequency content of a simple sine wave, but rather a fairly complex summation of several frequencies, usually multiples of the fundamental frequency. If the DC/DC converter switching frequency is selected to be exactly the same frequency (or a multiple) of the modulation/demodulation oscillator frequency of the isolation amplifier, the aliasing phenomena will not be a problem. This, of course, is unrealistic because of lot to lot variances and variations in temperature performance of both the DC/DC converter and the isolation amplifier. A small difference between the two switching frequencies will generate low frequency noise in the signal path that is impossible to filter.

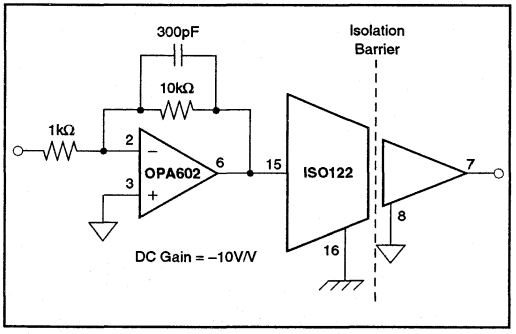


FIGURE 7. By Using a Pre-Gain Stage the Signal-to-Noise Ratio is Improved. In this Example the Signal-to-Noise Ratio is Improved by 20dB.

There are two design issues taken into consideration when selecting the DC/DC converter switching frequency for a specific isolation amplifier. As an example, in the case of the ISO122, an acceptable DC/DC switching frequency would be 400kHz. In this case, the difference between the DC/DC switching frequency and the isolation amplifier's oscillating frequency is 100kHz. The aliased noise will have a fundamental frequency content of 100kHz, which is easily filtered by the isolation amplifier. Additionally, the 5th harmonic of the DC/DC converter and the 4th harmonic of the ISO122 are equal. Generally, the amplitude of the DC/DC converter ripple having the frequency content of a higher harmonic is considerably smaller than that of lower harmonics. Signals aliased back from higher harmonic elements of the DC/DC converter's ripple voltage will be less.

In cases where the isolation amplifier has voltage-to-frequency modulation topology (ISO102 and ISO106), the selection of the DC/DC converter becomes more difficult. The frequency modulation range of the ISO102 and ISO106 is 0.5MHz (V_{OUT} = –10V) to 1.5MHz (V_{OUT} = +10V). In these applications, proper by-pass designs can help reduce noise caused by the switching frequency of the DC/DC converter.

Figure 10 illustrates resistor-capacitor and inductor-capacitor decoupling networks that can be used to isolate devices from power supply noise. These networks are used to eliminate coupling between circuits, keep power-supply noise from entering the circuit and to suppress the reflected ripple current of the DC/DC converter caused by the dynamic current component at its switching frequency. When the

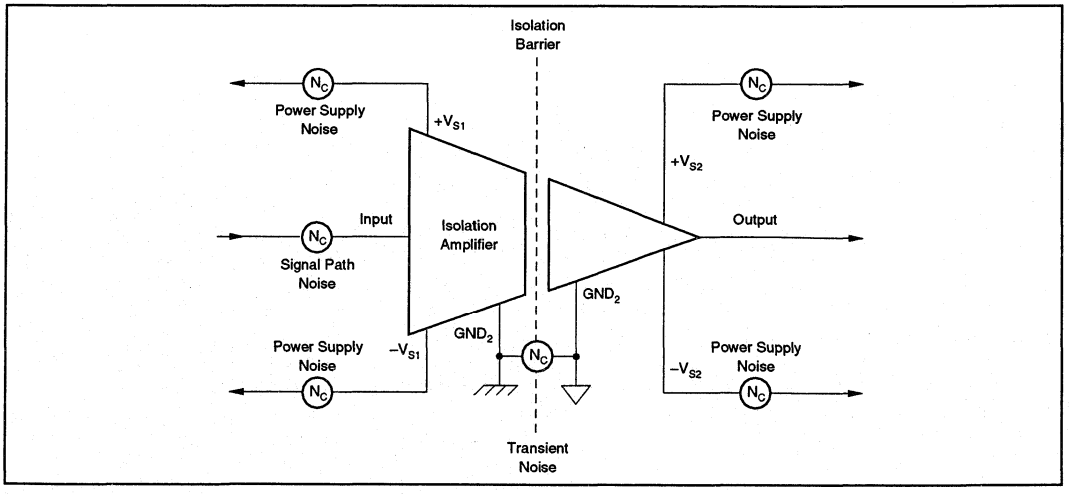


FIGURE 8. The Three Sources of Conductive Noise in an Isolation Application are from the Power Supply Lines, the Signal Path and Between the Isolated Grounds.

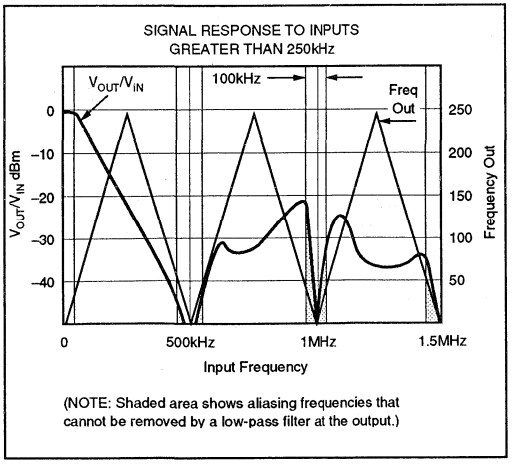


FIGURE 9. Noise Rejection Performance Curve of the ISO122.

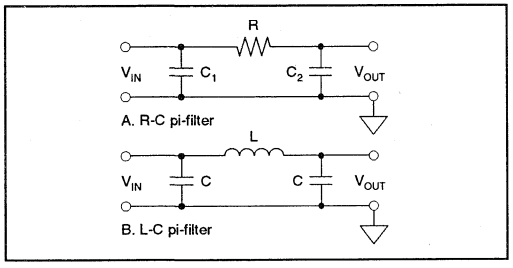


FIGURE 10. Suggested Pi-Filter Designs to Eliminate Power Supply Noise.

R-C filter is used, the voltage drop in the resistor causes a decrease in power-supply voltage (see AB-024 for more details). The L-C circuit provides more filtering, especially at high frequencies, however, the resonant frequency of the network can amplify lower frequencies. If a resistor is placed in series with the inductor, this resonant frequency is attenuated. See Figure 11 for the frequency response and design equations of the L-C network. This by-pass design approach is known as a pi-filter. The filter should be positioned on the PCB as close to the noise source as possible.

Power supply noise can be reduced by one or a combination of four methods. First, the designer should carefully select the DC/DC converter according to its power performance and switching frequency. Second, filter the output of the isolation amplifier to eliminate high frequency noise. Third, use a pi-filter on the supply lines as close to the switching source as possible. And fourth, in some instances, an external synchronization pin on the isolation amplifier makes it possible to synchronize multiple channels of isolation amplifiers to each other and the DC/DC power supplies.

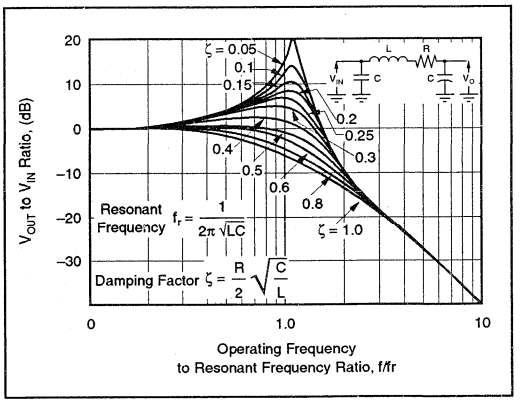


FIGURE 11. The L-C Pi-Filter Response and Design Formulas

Input Signal Noise

Noise in the signal path at the input of the isolation amplifier that is within the bandwidth of the isolation amplifier will be transmitted across the barrier with the desired signal. This type of noise is impossible to eliminate with a filter before or after the isolation amplifier and should be eliminated at its source. Typically, noise is coupled into the signal path where there is a metal trace with a high impedance node next to a metal trace where noise is present.

Signal path noise that is above the bandwidth of the isolation amplifier may or may not be transmitted across the barrier. Using the performance curve of the ISO122 in Figure 9, it is easy to deduce how much noise will be transmitted. In this instance, the x-axis represents the input noise frequency. The left y-axis represents the ratio between voltage out to input voltage. The right y-axis represents the frequency of the output signal generated by the aliasing effect. If there is concern that there will be high frequency noise at the input of the isolation amplifier, usually a low pass filter before the isolation amplifier will reduce the effects of input noise aliasing into the signal bandwidth.

High dV/dt Changes Between The Ground References Of The Isolation Barrier

A third source of conductive noise for isolation applications is caused by the transients between the two ground references across the isolation barrier (as shown in Figure 12). The isolation mode voltage (IMV) is the voltage that appears across the isolation barrier between the input common and output common. A fault condition may directly apply high voltage AC to the isolated common, forcing AC current through the barrier capacitors. Finite isolation mode rejection results in small output AC noise. Another specification that describes the ability of an isolation product to reject high transients between the grounds is called Transient Immunity (TI). These transients most commonly occur in motor control applications. Transient Immunity is specified in volts per seconds. A high Transient Immunity indicates a

MODEL	Isolation Function	Isolation Barrier-Type (Signal/Power)	Signal Modulation Method	Isolation Barrier Test Voltage[6] kV	Isolation Barrier Impedance[1] Ω/pF	Isolation Mode Rejection Ratio at 60Hz dB	Transient Immunity[1] kV/µs	Wide-band Noise Density[1] µV/Hz	Signal Output Ripple[1] mVp-p	Full Scale Bandwidth/ Small Signal Bandwidth kHz/µs	Number of DC/DC Channels	DC/DC Output Ripple/External Filter Capacitor/ Frequency[1] mVp-p/µF/kHz
ISO103	Buf-DC/DC	Cap/Mag	Duty Cycle	4rms	10E12/9	130[1]	1	4	25	20/75	1	5/1/1600
ISO107	Buf-DC/DC	Cap/Mag	Duty Cycle	8 peak	10E12/13	100[1]	0.006	4	20	20/75	1	10/0/1600
ISO113	Buf-DC/DC	Cap/Mag	Duty Cycle	4rms	10E12/9	130[1]	1	4	25	20/75	1	5/1/1600
ISO212	Amp-DC/DC	Mag	Balanced AM	1.2rms[2]	10E10/12	115[1]	0.6[3]	0.02	8	2/400	1	10/10/25
3656	Amp-DC/DC	Mag	Flyback	8DC	10E12/6	112	0.1[3]	0.117	5	1.3/500	1	100/.47/900
ISO100	Amp	Opto	Linear	2.5DC	10E12/2.5	108[1]	1[3]	6	0	5/100	—	—
ISO102	Buffer	Cap	Frequency	4rms	10E14/6	115	0.1	16	3	5/100	—	—
ISO106	Buffer	Cap	Frequency	8 peak	10E14/6	125	0.1	16	3	5/100	—	—
ISO120	Buffer	Cap	Duty Cycle	2.5rms[2]	10E14/2	115[1]	1	4	10	20/50	—	—
ISO121	Buffer	Cap	Duty Cycle	5.6rms[2]	10E14/2	115[1]	1	4	10	20/50	—	—
ISO122	Buffer	Cap	Duty Cycle	2.4rms[2]	10E14/2	140[1]	1	4	10	20/50	—	—

NOTES: (1) Typical. (2) Conforms with VDE884 partial discharge test methods. (3) Value based on limited evaluation; should be used for comparison purposes only.

greater ability to reject isolation mode voltage transients. If transient voltages between the grounds exceed the capabilities of the isolation amplifier, the input of the sensor amplifier may start to false trigger and the output will display spurious errors. Transient immunity is defined as the maximum rate of change of IMV voltage that does not interfere with the normal transmission of information across the barrier. Errors due to high transients that are less than 1% of the full scale range of the isolation amplifier are deemed to be within the normal transmission range.

A high transient phenomena is easy to identify by tracking the difference between the grounds and correlating it to errors at the output of the isolation amplifier. If the transients are predictable, this error can be filtered from the signal by timing data collection at the output of the isolation amplifier to when the data is known to be valid. In addition, selecting an isolation amplifier with a high Transient Immunity specification will reduce the errors caused by IMV transients.

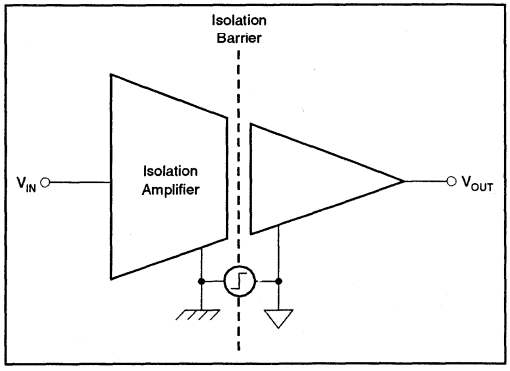


FIGURE 12. Transient Noise is Caused by High dV/dt Transients Between the Grounds of the Isolation Application.

RADIATED NOISE

Radiated noise is transmitted through air into high impedance nodes. Some isolation technologies are more sensitive to radiated noise interference than others. Radiated noise, also called EMI interference, can easily be identified as a problem by experimenting with the proximity of a circuit to a radiating device or by experimenting with shielding techniques. There are numerous sources for radiated noise such as ground planes, power planes, metal traces in close proximity, switching networks, inductors, toroids, etc. The E-field or the B-field portion of the radiated field can have an effect on isolation amplifiers. Specifically, a high E-field in the vicinity of the capacitively coupled isolation amplifiers can effect the performance of the device. In near-field emission areas, transmission of radiated sources is proportional to the inverse cube distance.

Radiated noise can transmit directly into the signal, usually through the capacitive barrier of the isolation amplifier. If the frequency content of the radiated noise is a multiple of the oscillating frequency of the isolation amplifier (plus or minus the bandwidth of the amplifier) the radiated noise will appear in the signal bandwidth. As an example, refer to Figure 9, using the left y-axis equal to the ratio of the output voltage of the isolation amplifier and the field strength of the radiate noise at the point of entry. Although it is difficult to quantify the field strength of a radiated signal at the point of entry, the concepts in Figure 9 still apply. In heavy fields, isolation amplifiers can produce signals outside of its linear region.

Radiated noise can be identified as a problem by experimenting with shielding or using a 10X scope probe to identify hot spots. Various metallic materials can be used for shielding as long as the metal is connected to a ground in the circuit. The most effective shielding material found in experimentation is Mumetal, however, copper and even conductive tape have been used to identify and eliminate problem areas.

CONCLUSION

Noise problems in any application can be difficult to solve, particularly if the causes and effects are not known. When investigating a noise problem in an isolation application, one or a combination of three noise sources can be identified as responsible for a noisy output of the isolated amplifier. By understanding the source of noise, steps can be taken in layout and circuit design to significantly reduce noise errors to acceptable levels.

REFERENCES

(1) Ott, Henry W., *Noise Reduction Techniques in Electronic Systems*, John Wiley & Sons, NY, 1976.

(2) Morrison, Ralph, *Noise and Other Interfering Signals*, John Wiley & Sons, NY, 1991.

(3) Zirngast, Mark F., *Isolation Amplifiers-Design and Implementation: Isolation, Transformer and Optical Techniques, Part 1*, Electronic Engineering, April, 1989, pp. 37-40.

(4) Zirngast, Mark F., *Isolation Amplifiers-Design and Implementation: Capacitive Isolation , Part 2*, Electronic Engineering, May, 1989, pp. 33-45.

(5) Burt, Rod, *Cut Noise in Isolated Circuits with Variable Carrier Amplifier*, Electronic Design, April 14, 1988, pp. 101-104.

(6) Baker, Bonnie, *Improved Device Noise Performance for the 3650 Isolation Amplifier*, Application Bulletin AB-044, Burr-Brown Corporation.

(7) Stitt, Mark, *Very Low Cost Analog Isolation with Power*, Application Bulletin AB-024, Burr-Brown Corporation.

(8) Stitt, Mark, *Simple Filter Eliminates ISO Amp Ripple and Keeps Full Bandwidth*, Application Bulletin AB-023, Burr-Brown Corporation.

BURR-BROWN® APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

BOOST ISO120 BANDWIDTH TO MORE THAN 100kHz

By R. Mark Stitt and Rod Burt (602) 746-7445

There has been considerable demand for high-bandwidth isolation amplifiers. The highest bandwidth Burr-Brown ISO amps are the ISO100 and the ISO120/121/122 family with bandwidths of about 50kHz. The ISO120/121 bandwidth can be boosted to more than 100kHz by adding gain in the feedback.

Adding gain in the feedback of the ISO120/121 increases bandwidth and decreases phase margin—see Figure 4. The ISO120 was designed with approximately 70° phase margin in the output stage for maximally flat magnitude response and a f_{-3dB} bandwidth of approximately 50kHz. With a gain of 2.4V/V in the feedback as shown in Figure 1, phase margin is decreased to an acceptable 45°. Due to gain peaking, the actual f_{-3dB} bandwidth is increased to almost 150kHz. With the addition of an input filter as shown in Figure 2, flat magnitude response with a bandwidth of greater than 100kHz is obtained. Since the added gain is within the ISO120 feedback loop, the overall gain of the isolation amplifier is unchanged (gain = 1).

To verify the phase margin, analyze the step response of the Figure 1 circuit (shown in the Scope Photo 1). The 25% overshoot translates to a damping factor of 0.4 and 45° phase margin.

If the ISO120 is used in the clocked mode, maximum bandwidth is determined by the clock frequency. For 150kHz bandwidth and 45° phase margin with a gain of 2.4V/V in the ISO120 feedback, the clock frequency should be 500kHz. Lower clock frequencies will result in reduced phase margin and possible instability. Higher clock frequencies will result in better phase margin, but clock frequencies above 700kHz are not recommended.

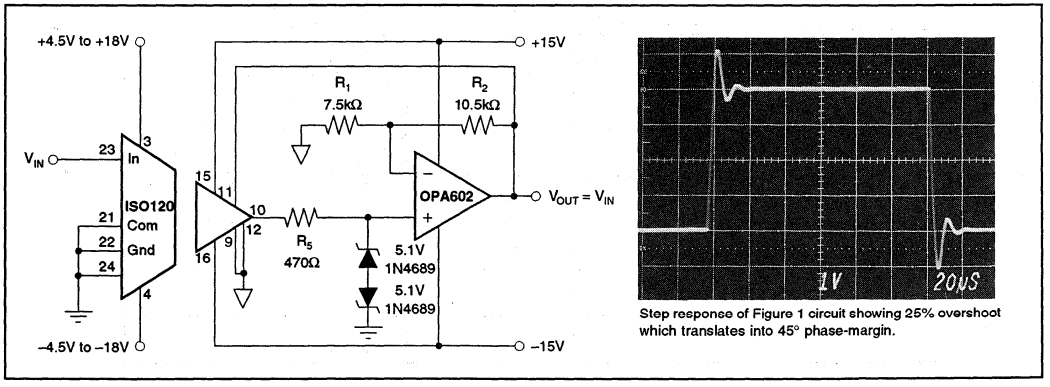


FIGURE 1. ISO120 with f_{-3dB} Bandwidth Boosted to Approximately 150kHz.

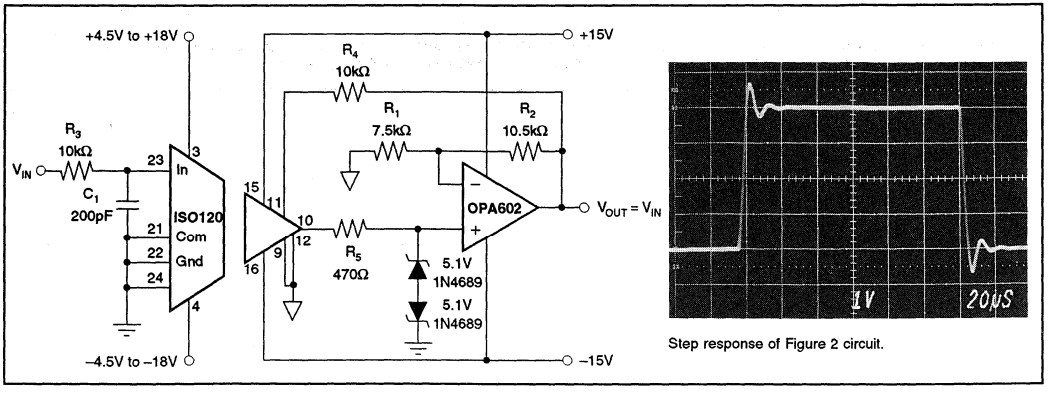
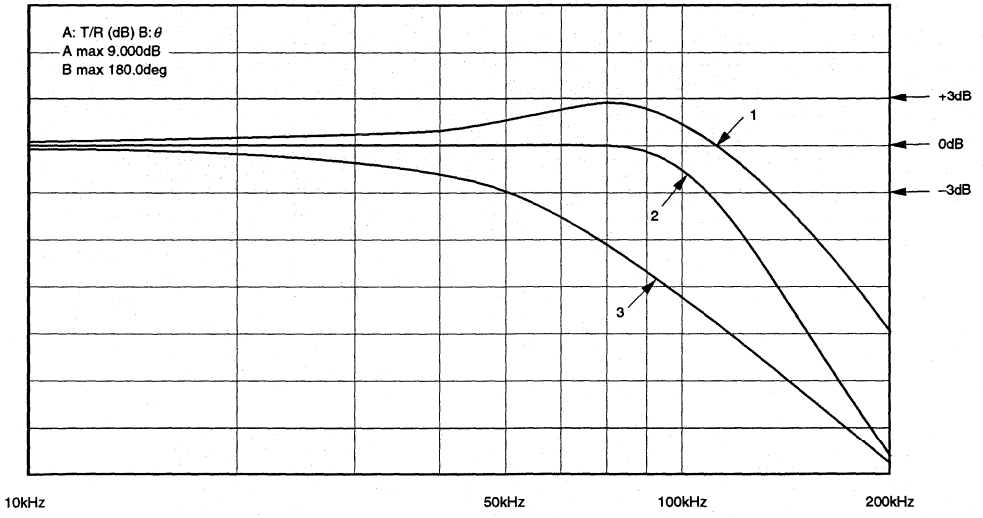


FIGURE 2. ISO120 with Flat Magnitude Response and f_{-3dB} Bandwidth Boosted to More Than 100kHz.

Adding gain in the feedback of the ISO120 can also increase its slew rate and full-power response. So long as the op amp providing gain in the feedback has adequate slew rate, the 2V/µs slew rate of the ISO120 is multiplied by its gain. When using an OPA602 with a gain of 2.4V/V in the feedback, the 30kHz 20Vp-p full-power response of the ISO120 is increased to more than 70kHz. Driving the OPA602 input below about –12V will cause signal inversion and possible circuit lock-up. The 470Ω/back-to-back zener network prevents possible lock-up by keeping the op amp input from being driven beyond its linear common-mode input range.

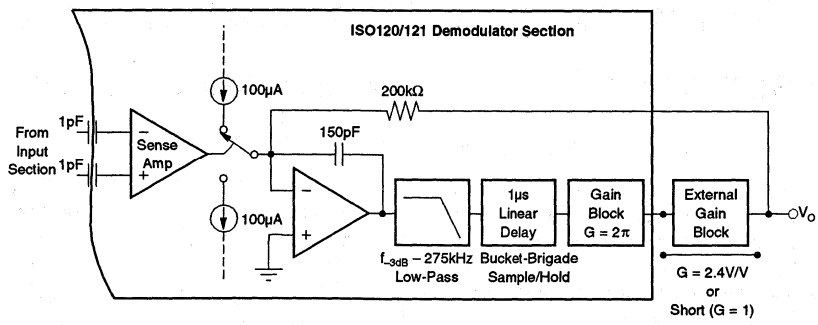
The addition of an input filter to compensate for the gain peaking, as shown in Figure 2, gives a flat magnitude response of more than 100kHz. In addition to the gain of 2.4V/V amplifier in the feedback, a simple 80kHz input filter formed by C_1 and R_3 is inserted at the input. The 10kΩ input resistor, R_3, decreases the ISO120 gain by about 5%. A matching 10kΩ resistor in the feedback, R_4, restores gain accuracy. The step response for the Figure 2 circuit is shown in the scope photo.

The Gain vs Frequency Plot, Figure 3, compares the response of the Figure 1 and Figure 2 circuits, to the standard ISO120. The top plot is the Figure 1 circuit showing about +3dB magnitude peaking and almost 150kHz f_{-3dB} bandwidth. The center plot is the Figure 2 circuit with the 80kHz input filter. The magnitude response is flat with an f_{-3dB} bandwidth greater than 100kHz. The bottom plot shows the standard ISO120 circuit with an f_{-3dB} bandwidth of about 50kHz.



Gain vs Frequency plot comparing: 1) Figure 1 circuit showing almost 150kHz f_{-3dB} bandwidth with +3dB gain peaking, 2) Figure 2 circuit showing flat magnitude response and more than 100kHz f_{-3dB} bandwidth, and 3) standard ISO120 showing 50kHz f_{-3dB} bandwidth.

FIGURE 3. Gain vs Frequency Plot.



The output demodulator section of the ISO120/121/122 consists of the integrator loop shown. This technique can not be applied to the ISO122 because the feedback connection is not available externally. Stability is determined by the phase margin at the open-loop response unity gain point, f_{UG}.

The unity-gain frequency is:

$$f_{UG} = \frac{6.28 \bullet gain_{EXT}}{2 \bullet \pi\ (200k\Omega) \bullet (150pF)} = 33kHz \bullet gain_{EXT}$$

The phase margin is approximated by:

$$180° - \underbrace{90°}_{\substack{200k\Omega,\ 150pF \\ integrator}} - \underbrace{\tan^{-1}(f_{UG}/275kHz)}_{\substack{higher\ order \\ poles}} - \underbrace{1\mu s \bullet f_{UG} \bullet 360°}_{\substack{sample/hold \\ delay^*}}$$

*The sample/hold delay is $1/(2 \bullet freq_{CLK})$. For a 500kHz clock frequency, the delay is 1µs. The free-running clock frequency is approximately 500kHz.

For $gain_{EXT}$ = 1:
f_{UG} = 33kHz, Phase Margin = 70°, and
f_{-3dB} = 50kHz

For $gain_{EXT}$ = 2.4:
f_{UG} = 80kHz, phase margin = 45°, and
f_{-3dB} = 150kHz with +3dB gain peaking at 80kHz.

FIGURE 4. Analysis of ISO120/121 Demodulator Section.

For Immediate Assistance, Contact Your Local Salesperson

BURR-BROWN® **APPLICATION BULLETIN**

Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

SYNCHRONIZATION OF ISO120/121 ISOLATION AMPLIFIERS

By Rod Burt and R. Mark Stitt (602) 746-7445

Internal clock circuitry in the ISO120/121 precision isolation amplifier (ISO amp) can be synchronized to an external clock signal. Synchronization to an external clock can be used to eliminate beat frequencies in multichannel systems or for rejection of specific AC signals and their harmonics—see the ISO120/121 product data sheet, PDS-820.

The external clock signal can be directly connected to the ISO120/121 if it is a sine or triangle wave of the proper amplitude. At clock frequencies above 400kHz, a square wave external clock can also be directly connected to the ISO120/121. Other clock signals can be used with the addition of the signal conditioning circuit shown in Figure 2.

SYNCHRONIZING TO A SINE OR TRIANGLE WAVE EXTERNAL CLOCK

The ideal external clock signal for the ISO120/121 is a ±4V sine wave or ±4V, 50% duty-cycle triangle wave. The *ext osc* pin of the ISO120/121 can be driven directly with a ±3V to ±5V sine or 25% to 75% duty-cycle triangle wave and the ISO amp's internal modulator/demodulator circuitry will synchronize to the signal.

EXTERNAL CLOCK FREQUENCY RANGE	C_1, C_2 ISO120/121 MODULATOR, DEMODULATOR EXTERNAL CAPACITOR
400kHz to 700kHz	none
200kHz to 400kHz	500pF
100kHz to 200kHz	1000pF
50kHz to 100kHz	2200pF
20kHz to 50kHz	4700pF
10kHz to 20kHz	0.01µF
5kHz to 10kHz	0.022µF

TABLE I. Recommended ISO120/121 External Modulator/Demodulator Capacitor Values vs External Clock Frequency.

EXTERNAL CLOCK FREQUENCY RANGE	C_X
400kHz to 700kHz	30pF
200kHz to 400kHz	180pF
100kHz to 200kHz	680pF
50kHz to 100kHz	1800pF
20kHz to 50kHz	3300pF
10kHz to 20kHz	0.01µF
5kHz to 10kHz	0.022µF

TABLE II. Recommended C_X Values vs Frequency for Figure 2 Circuit.

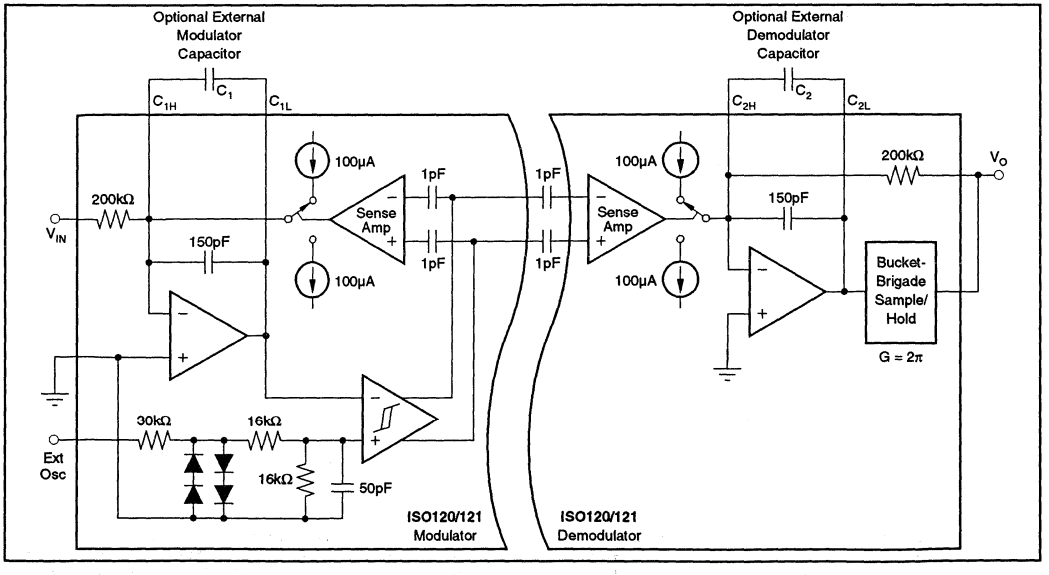


FIGURE 1. ISO120/121 Block Diagram Showing Internal Clamp and Filter Circuitry at the Ext Osc Pin.

Synchronizing to signals below 400kHz requires the addition of two external capacitors to the ISO120/121. Connect one capacitor in parallel with the internal modulator capacitor and connect the other capacitor in parallel with the internal demodulator capacitor as shown in Figure 1.

The value of the external modulator capacitor, C_1, depends on the frequency of the external clock signal. Table I lists recommended values.

The value of the external demodulator capacitor, C_2, depends on the value of the external modulator capacitor. To assure stability, C_2 must be greater than $0.8 \bullet C_1$. A larger value for C_2 will decrease bandwidth and improve stability:

$$f_{-3dB} \approx \frac{1.2}{200k\Omega\,(150pF + C_2)}$$

Where:
$f_{-3dB} \approx$ –3dB bandwidth of ISO amp with external C_2 (Hz)
C_2 = External demodulator capacitor (F)

For example, with $C_2 = 0.01\mu F$, the f_{-3dB} bandwidth of the ISO120/121 is approximately 600Hz.

SYNCHRONIZING TO A 400kHz TO 700kHz SQUARE-WAVE EXTERNAL CLOCK

At frequencies above 400kHz, an internal clamp and filter provides signal conditioning so that a square-wave signal can be used to directly drive the ISO120/121. A square-wave external clock signal can be used to directly drive the ISO120/121 *ext osc* pin if: the signal is in the 400kHz to 700kHz frequency range with a 25% to 75% duty cycle, and ±3V to ±20V level. Details of the internal clamp and filter circuitry are shown in Figure 1.

SYNCHRONIZING TO A 10% TO 90% DUTY-CYCLE EXTERNAL CLOCK

With the addition of the signal conditioning circuit shown in Figure 2, any 10% to 90% duty-cycle square-wave signal can be used to drive the ISO120/121 ext osc pin. With the values shown, the circuit can be driven by a 4Vp-p TTL signal. For a higher or lower voltage input, increase or decrease the 1kΩ resistor, R_X, proportionally. e.g. for a ±4V square wave (8Vp-p) R_X should be increased to 2kΩ.

The value of C_X used in the Figure 2 circuit depends on the frequency of the external clock signal. Table II shows recommended capacitor values.

Note: For external clock frequencies below 400kHz, external modulator/demodulator capacitors are required on the ISO120/121 as before.

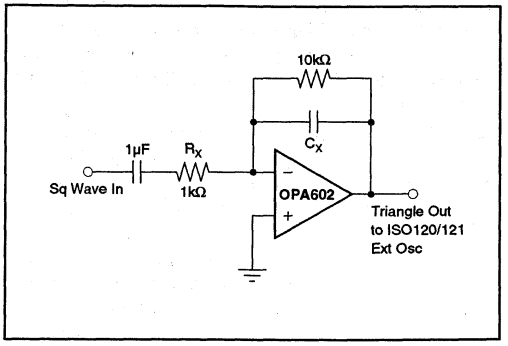


FIGURE 2. Square Wave to Triangle Wave Signal Conditioner for Driving ISO120/121 Ext Osc Pin.

For Immediate Assistance, Contact Your Local Salesperson

BURR-BROWN® **APPLICATION BULLETIN**

Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

SINGLE-SUPPLY OPERATION OF ISOLATION AMPLIFIERS

By Rod Burt and R. Mark Stitt (602) 746-7445

For simplicity, many systems are designed to operate from a single external power supply. In battery powered systems such as aircraft and automotive, it's often a requirement. Isolation amplifiers such as the ISO120 and ISO122 can be easily modified for input side single-supply operation with the addition of an INA105 difference amplifier. With ISO amps, it's the isolated input side power supply which most often needs to be single supply. The output side of the ISO amp uses a split ±15V power supply, allowing a full ±10V output swing.

The difference amplifier has advantages as compared to traditional single-supply amplifiers. The inputs of a difference amplifier can swing to both the positive and negative power-supply rails. In fact, in the application shown in Figures 1 and 2, the input range of the circuit extends approximately 2V below ground (the negative power supply rail). This is because the resistors internal to the INA105 divide the input level in half as seen by the op amp.

The technique is illustrated in Figures 1 and 2 using the ISO120 and ISO122. These ISO amps are specified for operation from dual supplies as low as ±4.5V and can be operated with a total single power supply voltage as low as 9V. The circuit shown is designed for operation from a single +15V power supply. This allows a 0V to +5V input range.

The most common application is for a single ended input referred to ground as shown. For a differential input, pin 2 can be connected to a second input instead of ground. This provides a 0V to 5V differential input with common-mode to either rail.

To understand how the circuit works, consider the operation of the INA105 difference amplifier. The difference amplifier forces its output (pin 6) relative to its reference (pin 1) to be equal to the differential input (pin 3 – pin 2). The difference amplifier reference pin and the ISO amp common are held at approximately 5.1V by the 10kΩ resistor and the zener diode. This pseudo ground establishes an arbitrary acceptable operating point for the ISO amp. The difference amplifier then translates its input, relative to true ground, up to the 5.1V pseudo ground. In other words, a 0V to 5V input between pins 3 and 2 of the INA105 is seen as a 0V to 5V signal at the ISO amp input.

Isolated power is often at a premium and both the ISO120/122 and the INA105 operate on relatively low power. Common zener diodes, on the other hand, may require several mA for proper operation. The 1N4689 zener diode specified is a low level type designed for applications requiring low operating currents. It has a sharp breakdown voltage specified at a low 50µA.

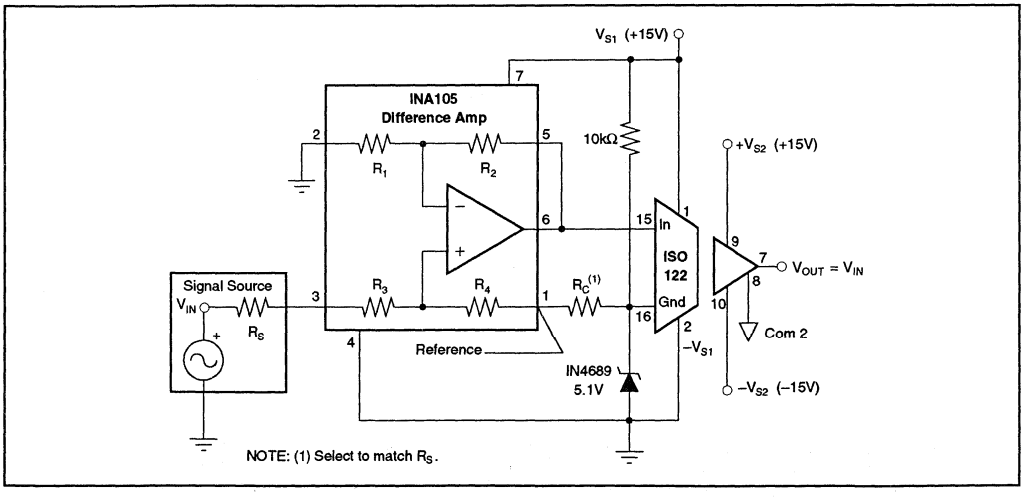


FIGURE 1. Single Supply Operation of the ISO122 Isolation Amplifier.

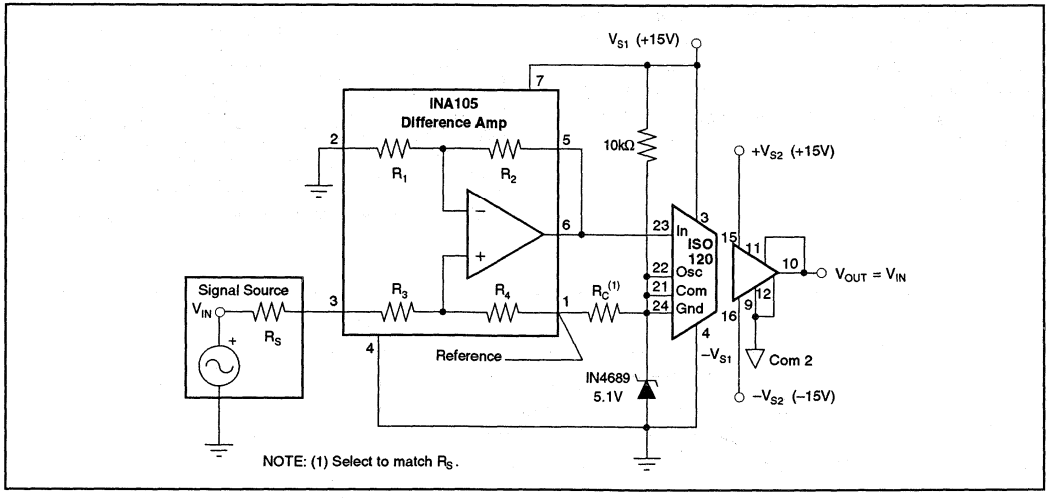


FIGURE 2. Single Supply Operation of the ISO120 Isolation Amplifier.

The accuracy of the INA105 difference amplifier relies on careful resistor ratio matching ($R_3/R_4 = R_1/R_2$). Any source impedance of the signal (R_S) adds to the difference resistor (R_3). For low source impedances, the error is acceptable. For better accuracy at higher source impedances, a compensating resistor (R_C) can be added to restore the ratio matching. The resistors in the INA105 are 25kΩ. For 0.1% gain accuracy, no compensating resistor is required with source impedances up to 25Ω. For source impedances up to 2.5kΩ, use a compensating resistor which matches R_S within 1%. If the source impedance is not known exactly, a trim pot can be used to adjust gain accuracy.

For operation with source impedances greater than 2.5kΩ, a unity-gain-connected single-supply op amp can be added to buffer the input as shown in Figure 3. Although the input range of the OPA1013 single-supply op amp includes the negative rail, its output can not quite swing all the way to the rail. The negative swing limit of this circuit is therefore ≈100mV—still adequate in many applications.

For an instrumentation amplifier (IA) front end, the other half of the OPA1013 can be connected to the inverting input of the INA105 (pin 2) as shown in Figure 4.

For a true single-supply ISO amp with high impedance differential inputs, the circuit shown in Figure 5 can be used. In this circuit, the inputs—and therefore the outputs—of the OPA1013s are level-shifted up a V_{BE} with a matched pair of PNP input transistors. The transistors are biased as emitter followers by a pair of 100μA current sources contained in the REF200 dual current source.

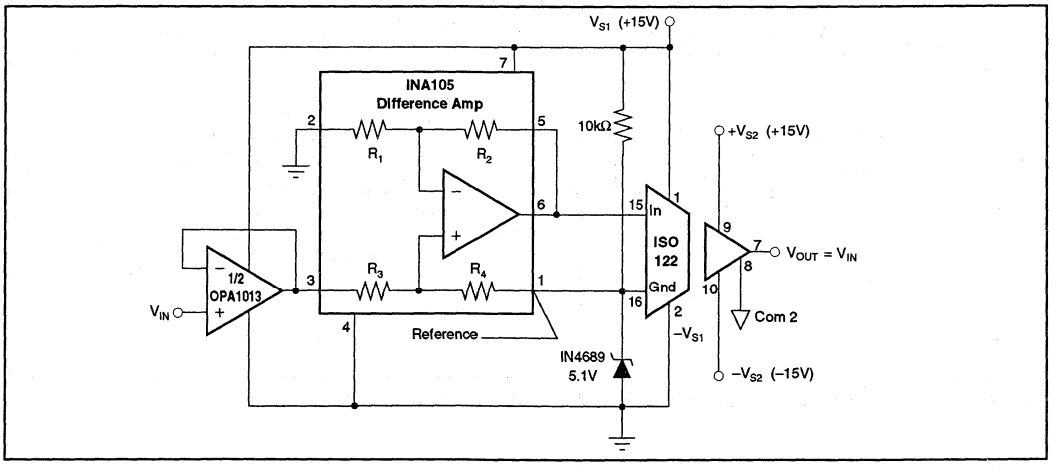


FIGURE 3. Single Supply (almost—see text), High Input Impedance Isolation Amplifier.

The circuits shown in this bulletin were designed for 0V to 5V operation from a single +15V power supply. With reduced range, operation from a lower voltage is feasible. For higher input range the circuit can be operated from a higher supply voltage. Table 1 shows the ranges obtainable for selected power supplies.

V_S (V)	INPUT RANGE FIGURES 1, 2 (V) (1)	INPUT RANGE FIGURES 3, 4 (V) (1)	INPUT RANGE FIGURE 5 (V) (1)
20+	–2 to +10	0.1 to +10	–0.3 to +10
15	–2 to +5	0.1 to +5	–0.3 to +5
12	–2 to +2	0.1 to +2	–0.3 to +2
Note: (1) Since the amplifier is unity gain, the input range is also the output range. The output can go to –2V since the output section of the ISO amp operates from dual supplies.			

TABLE 1. Single-Supply ISO Amp Input Range vs Power Supply.

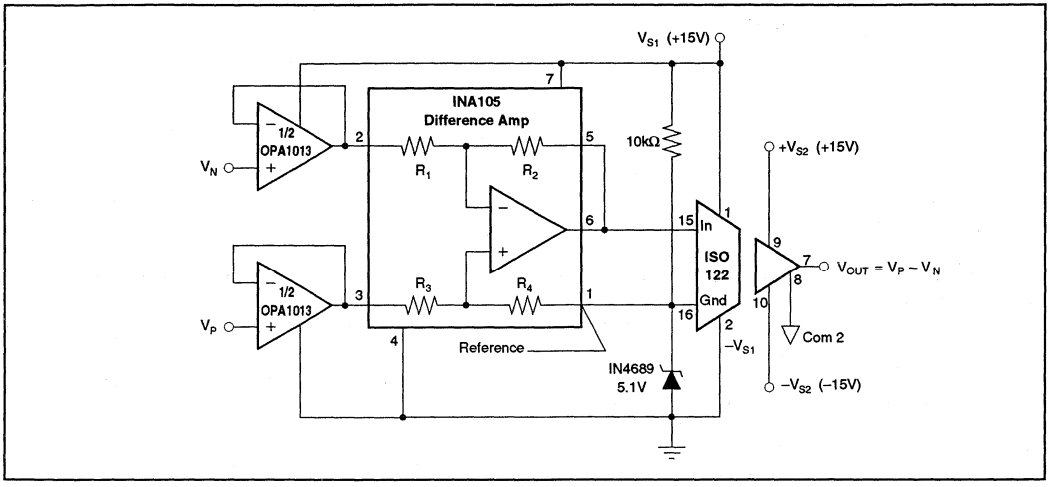


FIGURE 4. Single Supply (almost—see text), Isolation Amplifier with High-Impedance Differential Inputs.

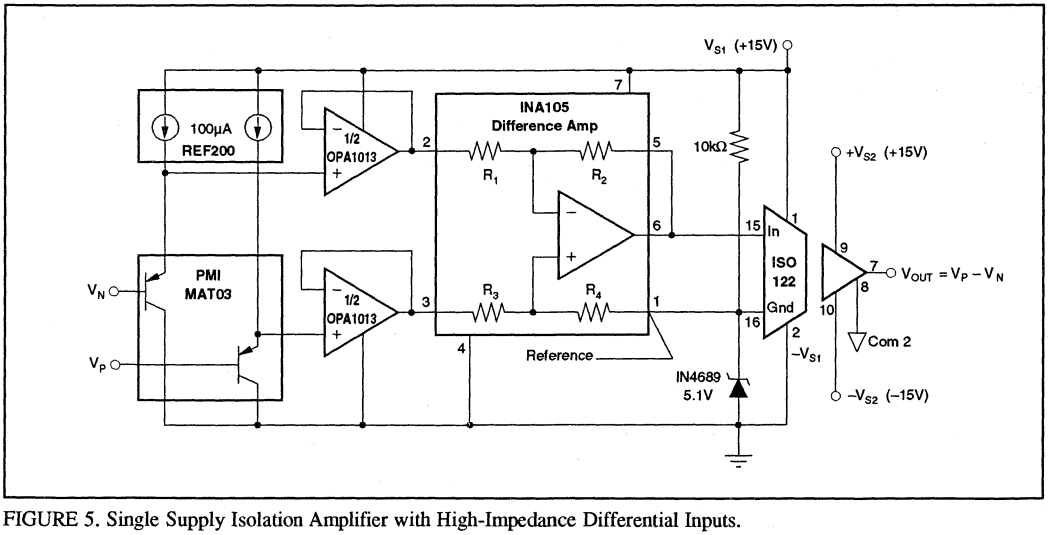


FIGURE 5. Single Supply Isolation Amplifier with High-Impedance Differential Inputs.

For a single-supply ISO amp with higher common-mode-voltage differential inputs, an INA117 high common-mode voltage difference amplifier can be substituted for the INA105 difference amplifier as shown in Figure 6. With a +15V power supply, the input common mode range is approximately +125V, –50V. With a +12V supply, the input common mode range is approximately ±50V. Differential input range remains as shown in Table I for Figures 1 and 2.

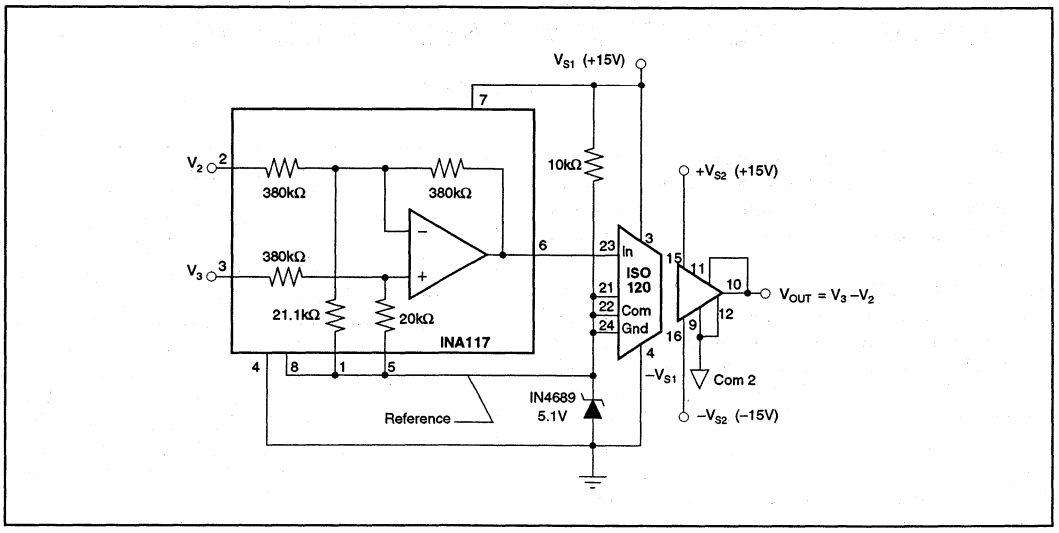


FIGURE 6. Single Supply Isolation Amplifier with High Common-Mode Range Differential Inputs.

BURR-BROWN®
APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

SIMPLE OUTPUT FILTER ELIMINATES ISO AMP OUTPUT RIPPLE AND KEEPS FULL BANDWIDTH

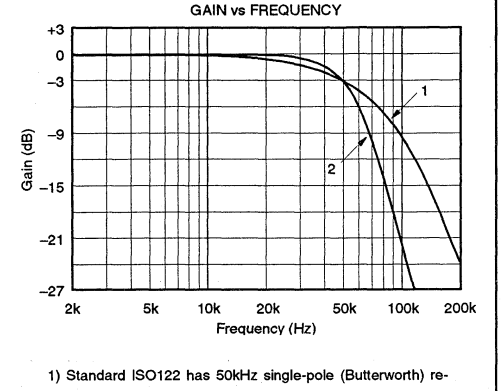
By Mark Stitt (602) 746-7445

The ISO120/121/122 isolation amplifiers (ISO amps) have a small (10-20mVp-p typ) residual demodulator ripple at the output. A simple filter can be added to eliminate the output ripple without decreasing the 50kHz signal bandwidth of the ISO amp.

The ISO120/121/122 is designed to have a 50kHz single-pole (Butterworth) signal response. By cascading the ISO amp with a simple 50kHz, Q = 1, two-pole, low-pass filter, the overall signal response becomes three-pole Butterworth. The result is a maximally flat 50kHz magnitude response and the output ripple reduced below the noise level.

Figure 1 shows the complete circuit. The two-pole filter is a unity-gain Sallen-Key type consisting of A_1, R_1, R_2, C_1, and C_2. The values shown give Q = 1 and f_{-3dB} bandwidth = 50kHz. Since the op amp is connected as a unity-gain follower, gain and gain accuracy of the ISO amp are unaffected. Using a precision op amp such as the OPA602 also preserves the DC accuracy of the ISO amp.

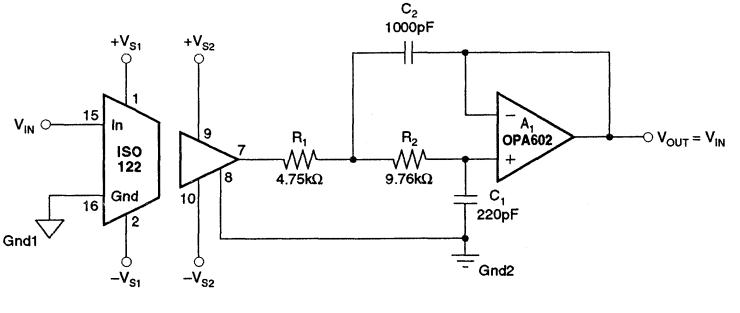
Figure 2 compares the magnitude response of the standard and filtered ISO amp. Figures 3 and 4 show the output ripple improvement. Figures 5 and 6 show the good step response of both the standard and filtered ISO amp.



1) Standard ISO122 has 50kHz single-pole (Butterworth) response.

2) ISO122 with cascaded 50kHz, Q = 1, two-pole, low-pass filter has three-pole Butterworth response.

FIGURE 2. Gain vs Frequency Plot.



NOTE: Cascading the 50kHz single-pole response ISO122 with a 50kHz, Q = 1, two-pole, low-pass filter produces an overall three-pole Butterworth response and eliminates output ripple.

FIGURE 1. ISO122 with Output Filter for Improved Ripple.

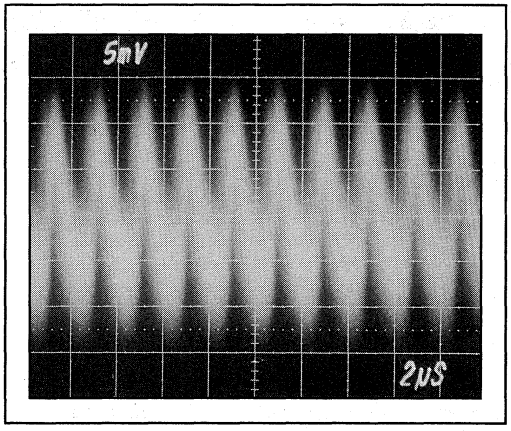


FIGURE 3. Standard ISO122 (approximately 20mVp-p output ripple).

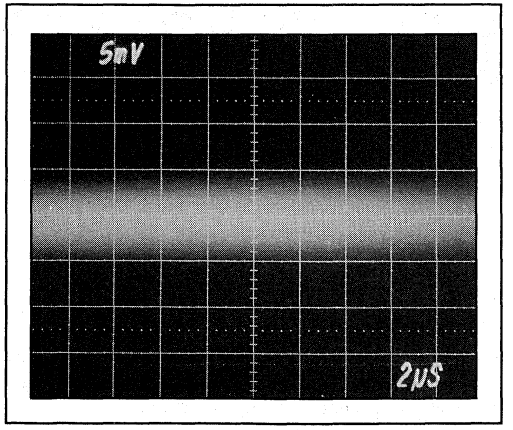


FIGURE 4. Filtered ISO122 (no visible output ripple).

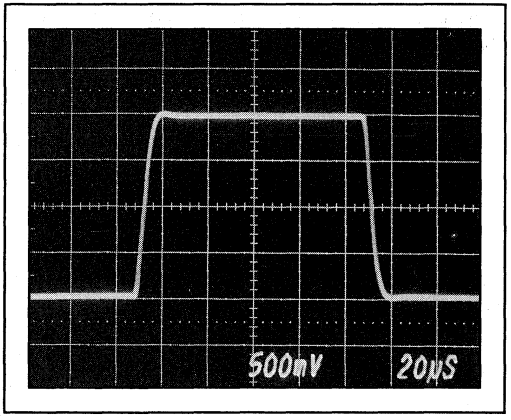


FIGURE 5. Step Response of Standard ISO122.

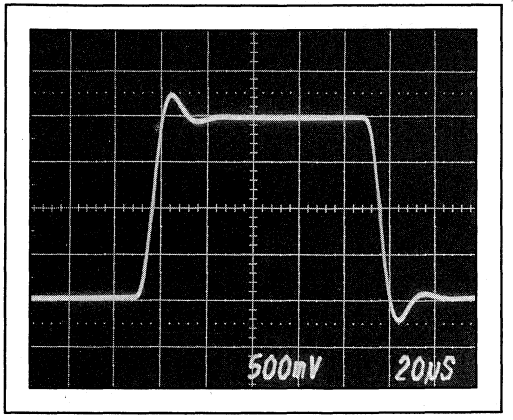


FIGURE 6. Step Response of ISO122 with Added Two-pole Output Filter.

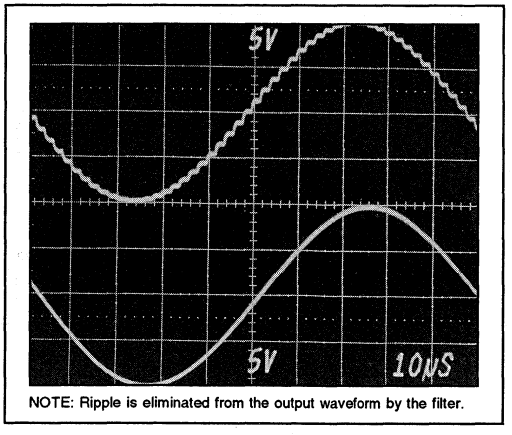


FIGURE 7. Large-signal, 10kHz Sine-wave Response of ISO122 with and without Output Filter.

BURR-BROWN® APPLICATION BULLETIN

Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

VERY LOW COST ANALOG ISOLATION WITH POWER

By Mark Stitt (602) 746-7445

You can make a low-cost, precision analog isolation amplifier (ISO amp) with power by combining the ISO122 low-cost ISO amp with the HPR117 low-cost DC/DC converter. With isolated signal and isolated power in separate packages, complete application flexibility is assured.

The ISO122 features:

- Unity gain (±10V In to ±10V Out): ±0.05%
- 0.02% max nonlinearity
- 5mA quiescent current
- 140dB isolation mode rejection at 60Hz
- 1500Vrms continuous isolation rating (100% tested)

The HPR117 features:

- $V_{OUT} = V_{IN}$, ±5% (V_{IN} = 13.5V to 16.5V, I_{OUT} = 25mA)
- I_{OUT} = 25mA (750mW) continuous at 85°C
- 8mA quiescent current, no load
- 80% efficiency, full load
- Low output ripple
- 750VDC isolation rating

OUTPUT-SIDE POWERED ISO AMP

The most commonly used ISO amp configuration is shown in Figure 1. Both the ISO amp and the DC/DC converter are powered at the output side of the ISO amp. The HPR117 is connected to +15V and ground. The ISO122 is connected to ±15V and ground. The power-supply connections for the input side of the ISO amp are connected directly to the HPR117 output. No bypass capacitors are needed. The HPR117 has built-in 0.33µF bypass capacitors on both the input and outputs.

The isolated ±15V power output from the HPR117 can also be used for ancillary input-side circuitry such as input amplifiers and references. The ISO122 input section consumes about ±5mA. An additional ±20mA is available for other circuitry.

INPUT-SIDE POWERED ISO AMP

Some applications call for output-side isolation as shown in Figure 2. Isolated ±15V, 20mA auxiliary power is available on the output side for ancillary circuitry.

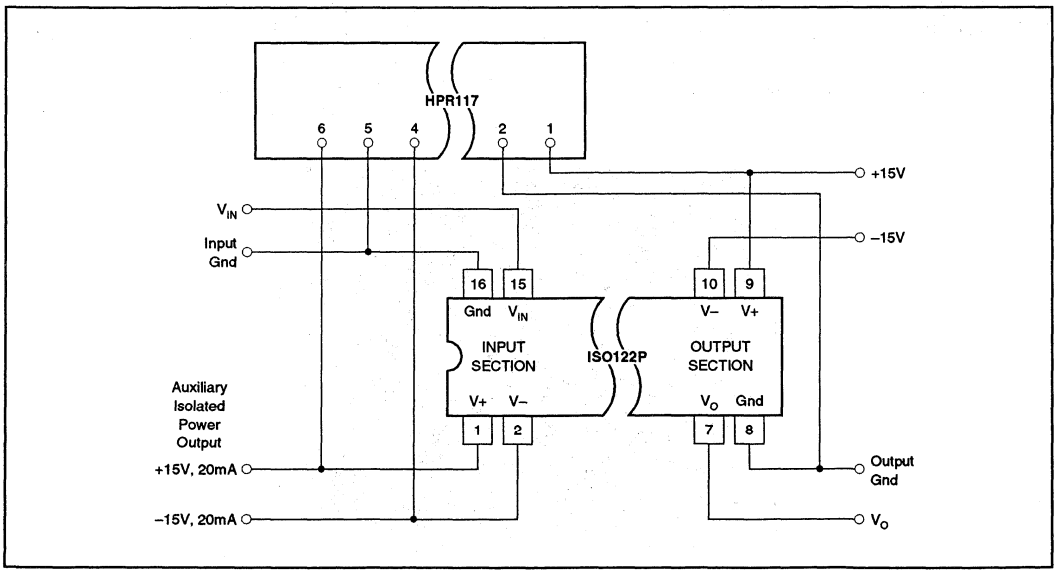


FIGURE 1. Output-Side Powered ISO Amp.

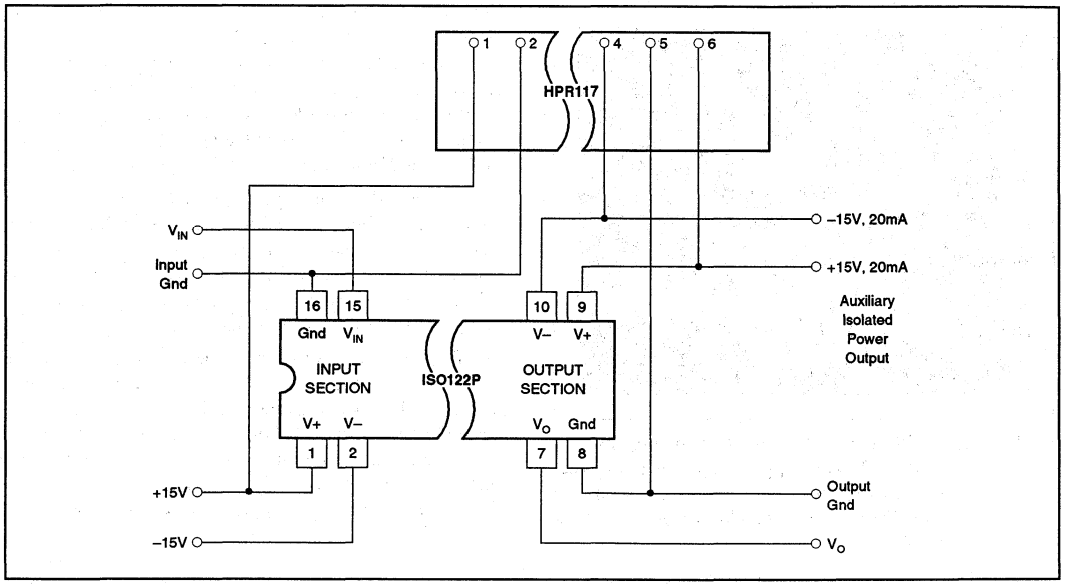


FIGURE 2. Input-Side Powered ISO Amp.

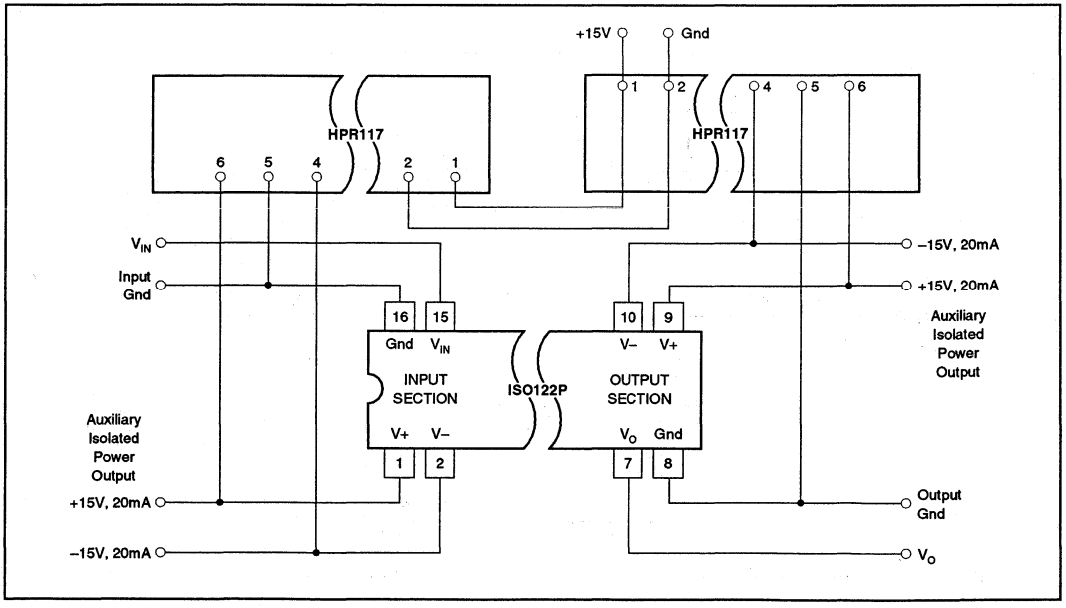


FIGURE 3. Powered ISO Amp with Three-Port Isolation.

THREE PORT ISO AMP

Some applications call for three-port isolation as shown in Figure 3. Both the input and output side of the ISO amp are isolated from the power-supply connection. Isolated ±15V, 20mA auxiliary power is available on both the input and output side of the ISO amp.

ADD RC FILTER TO POWER SUPPLY OUTPUT FOR LOW NOISE

Although performance is good using the ISO122 connected directly to the HPR117, best performance can be achieved with additional filtering. The output ripple of the HPR117 can interact with the ISO122 modulator/demodulator cir-

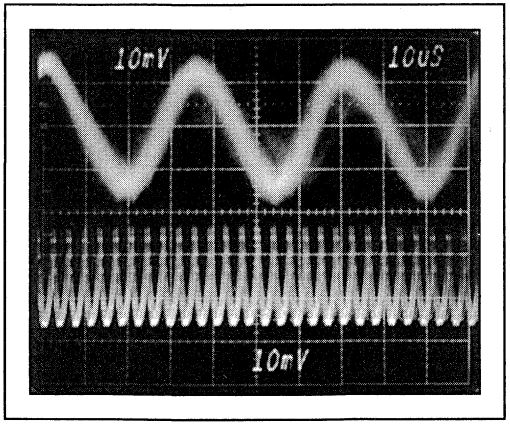


FIGURE 4. Oscilloscope Photograph Showing Typical HPR117 Power Supply Ripple (bottom trace) and Typical 30kHz, 30mVp-p Noise at the ISO122 Output Due to Aliasing of Power Supply Ripple.

cuitry through the power-supply pins resulting in an aliased noise signal within the signal bandwidth of the ISO amp. The 30kHz, 30mVp-p upper trace in Figure 4's scope photo is a typical example. The lower trace in the scope photo is the HPR117 output ripple with the ISO122 plus a 2kΩ load. Adding simple R, C filters in the outputs from the HPR117 as shown in Figure 5 eliminates the problem.

The R,C filter shown in Figure 5 can also be used with either the Figure 1 or Figure 2 circuit. Since the DC/DC converter can induce a substantial amount of ripple on input-side connections, filters may still be needed on both the input-side and output-side power supply connections of the ISO122 to prevent noise due to signal aliasing.

The filter resistors will degrade the load regulation of the DC/DC converters. In addition to the specified HPR117 load regulation, there will be an additional 50mV/mA drop through the 50Ω filter resistors. Although this results in only a 1.25V drop at the full-rated 25mA output, you may want to use smaller value resistors and commensurately larger value filter capacitors if power-supply sensitive ancillary circuitry is needed.

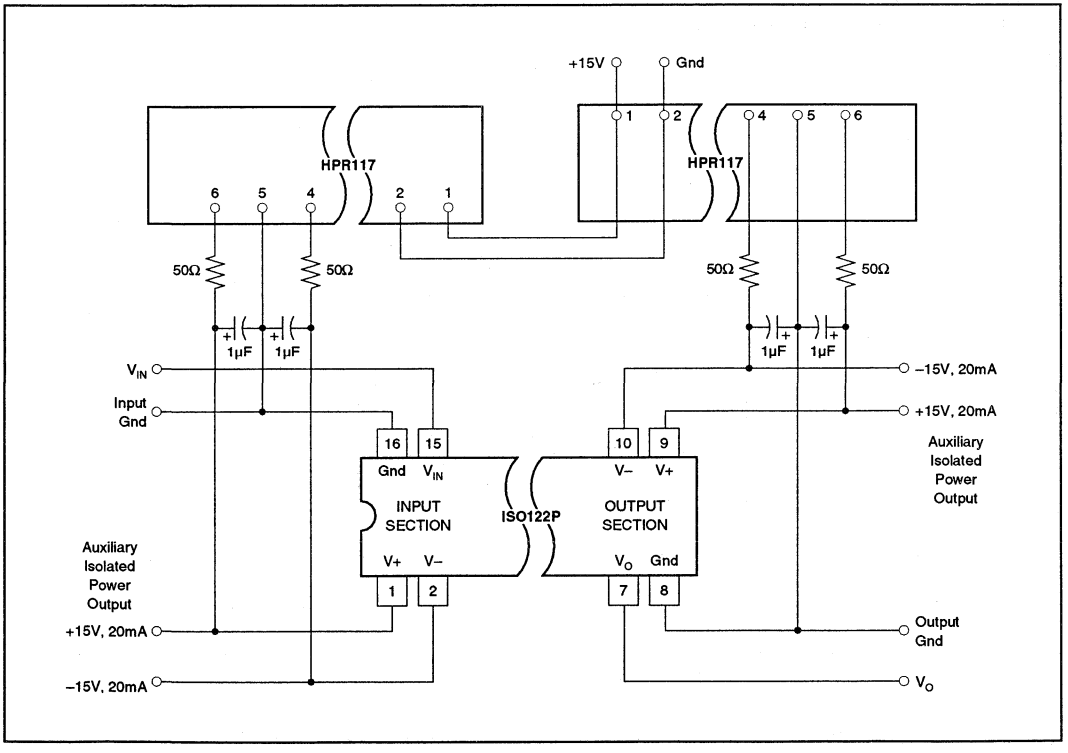


FIGURE 5. Three-Port Isolation Amplifier with R, C Power Supply Filters (eliminates power-supply induced noise).

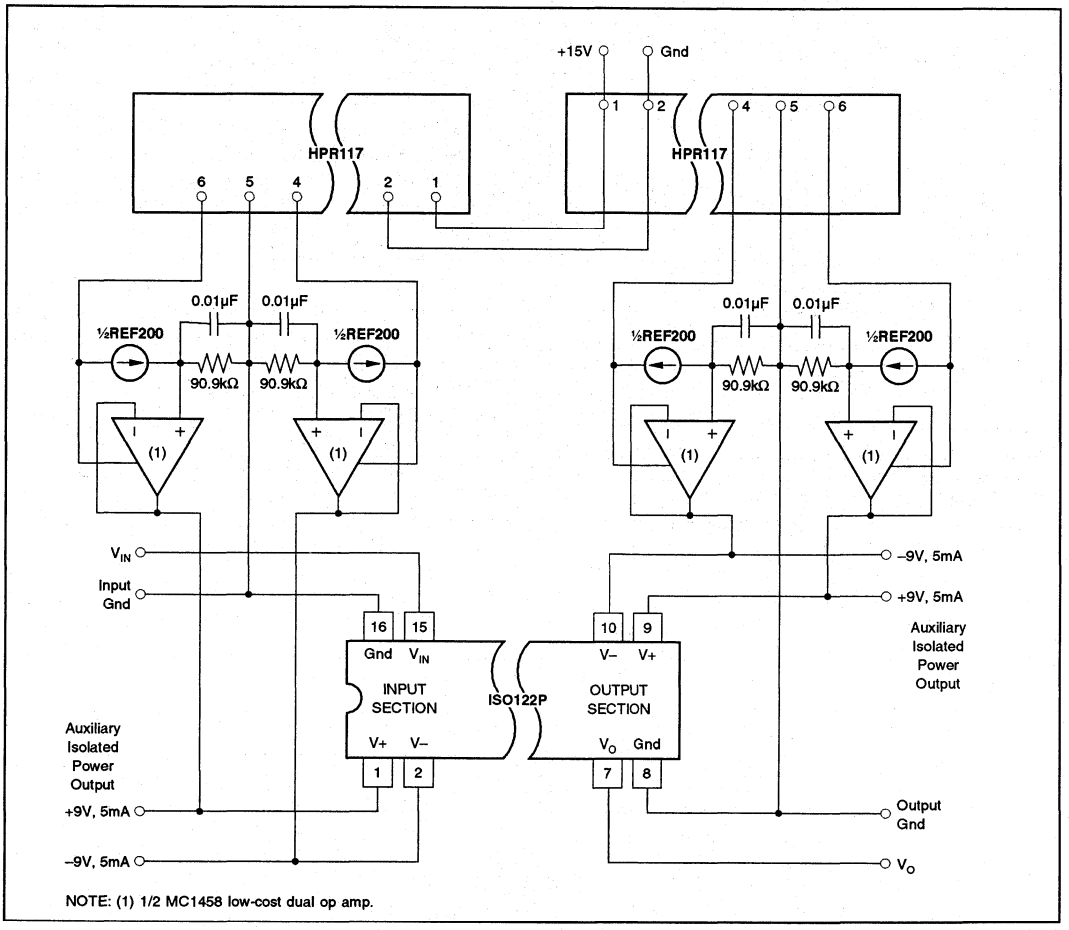


FIGURE 6. Power Supply Regulation in Three-Port Isolation Amplifier (eliminates power-supply induced noise and improves power-supply rejection).

ADD REGULATION FOR IMPROVED POWER-SUPPLY REJECTION

Output ripple can be eliminated and power-supply rejection of the three-port isolation amplifier can be improved as shown in Figure 6. The circuit consists of a dual 100µA current source (the REF200) driving 90.9kΩ resistors to set-up a ±9.09V reference. An inexpensive dual op amp (e.g. Motorola MC1458) is connected as a unity-gain follower to buffer the reference and drive the ISO122. With this circuit, the power-supply rejection is improved from a typical 2mV/V to less than ±1mV for a full 14V to 16.5V input change—(0.4mV/V).

When using the Figure 6 circuit, ISO amp output swing will be reduced. The ISO122 output swing is ±12.5V typ, ±10V min on ±15V supplies. With the ±9V regulated supplies, output swing will be ±6.5V typ, ±4V min.

BURR-BROWN®

APPLICATION BULLETIN

Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

AN ERROR ANALYSIS OF THE ISO102 IN A SMALL SIGNAL MEASURING APPLICATION

High accuracy measurements of low-level signals in the presence of high isolation mode voltages can be difficult due to the errors of the isolation amplifiers themselves.

This error analysis shows that when a low drift operational amplifier is used to preamplify the low-level source signal, a low cost, simple and accurate solution is possible.

In the circuit shown in Figure 1, a 50mV shunt is used to measure the current in a 500VDC motor. The OPA27 amplifies the 50mV by 200X to 10V full scale. The output of the OPA27 is fed to the input of the ISO102, which is a unity-gain isolation amplifier. The 5kΩ and 1kΩ potentiometers connected to the ISO102 are used to adjust the gain and offset errors to zero as described in the ISO102 data sheet.

SOME OBSERVATIONS

The total errors of the op amp and the iso amp combined are approximately 0.6% of full-scale range. If the op amp had not been used to preamplify the signal, the errors would have been 74.4% of FSR. Clearly, the small cost of adding the op amp buys a large performance improvement.

After gain and offset nulling, the dominant errors of the iso amp are gain nonlinearity and power supply rejection. Thus, well regulated supplies will reduce the errors even further.

The rms noise of the ISO102 with a 120Hz bandwidth is only 0.18mVrms, which is only 0.0018% of the 10V full-scale output. Therefore, even though the 16μV/√Hz noise spectral density specification may appear large compared to other isolation amplifiers, it does not turn out to be a significant error term. It is worth noting that even if the bandwidth is increased to 10kHz, the noise of the iso amp would only contribute 0.016% FSR error.

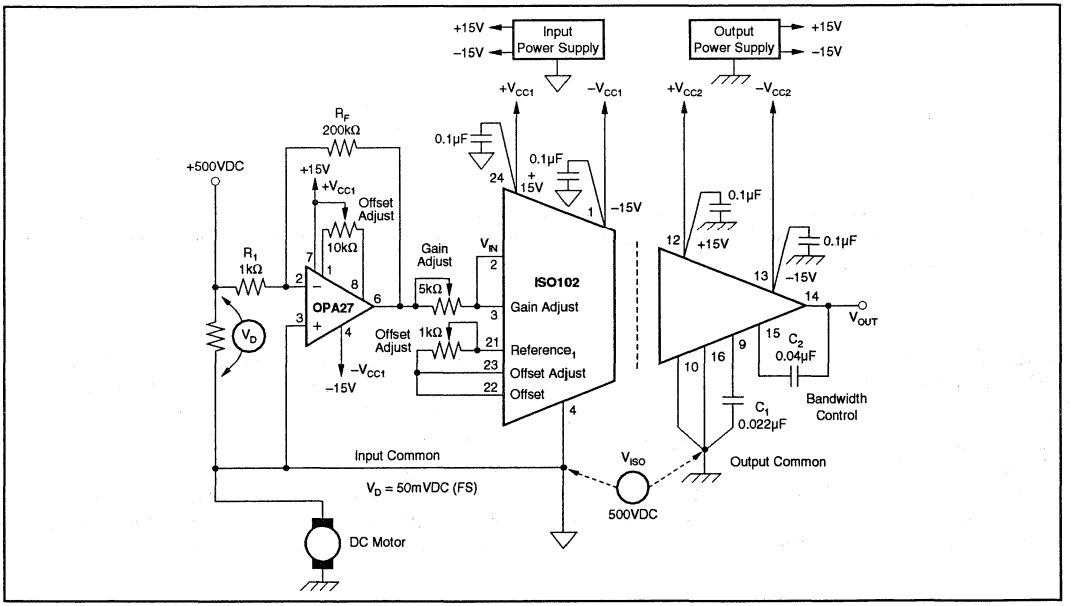


FIGURE 1. 50mV Shunt Measures Current in A 500VDC Motor.

THE ERRORS OF THE OP AMP AT 25°C (Referred to Input, RTI)

$$V_{E\,(OPA)} = V_D\left[1-\frac{1}{1+\frac{1}{\beta\,A_{VOL}}}\right] + V_{OS}\left[1+\frac{R_1}{R_F}\right] + I_B R_1 + PSR + Noise$$

$V_{E\,(OPA)}$ = Total Op Amp Error (RTI)

V_D = Differential Voltage (Full Scale) Across Shunt

$\left[1-\frac{1}{1+\frac{1}{\beta\,A_{VOL}}}\right]$ = Gain Error Due to Finite Open Loop Gain

β = Feedback Factor
A_{VOL} = Open Loop Gain at Signal Frequency
V_{OS} = Input Offset Voltage
I_B = Input Bias Current
PSR = Power Supply Rejection (μV/V) [Assuming a 20% change with ±15V supplies. Total error is twice that due to one supply.]

Noise = 5nV/√Hz (for 1kΩ source resistance and 1kHz bandwidth)

$ERROR_{(OPA)}$ (RTI)		GAIN ERROR		OFFSET		PSR		NOISE
$V_{E\,(OPA)}$	$=50mV\left[1-\frac{1}{1+\frac{1}{10^6/200}}\right]+$		$\left[0.025mV\left(1+\frac{1}{200}\right)+40\times10^{-9}\times10^3\right]$		+ [20μV/V x 3V x 2]	+	[5nV√120 (nVrms)]	
	=	0.01mV	+	[0.0251mV + 0.04mV]	+	0.12mV	+	55nVrms
Error as % of FSR	=	0.02%	+	[0.05% + 0.08%]	+	0.24%	+	0.00011%
After Nulling								
	=	0.01mV	+	[0mV + 0mV]	+	0.12mV	+	55nVrms
	=	0.13mV						
Error as % of FSR(1)	=	0.02%	+	[0% + 0%]	+	0.24%	+	0.00011%
	=	0.26% of 50mV						

NOTE: (1) FSR = Full-Scale Range. 50mV at input to op amp, or 10V at input (and output) of ISO amp.

THE ERRORS OF THE ISO AMP AT 25°C (RTI)

$$V_{E\,(ISO)} = \frac{1}{200}\left[\frac{V_{ISO}}{IMR} + V_{OS} + GE + Nonlinearity + PSR + Noise\right]$$

$V_{E\,(ISO)}$ = Total ISO Amp Error
IMR = Isolation Mode Rejection
V_{OS} = Input Offset Voltage
$V_{ISO} = V_{MV}$ = Isolation Voltage = Isolation Mode Voltage
GE = Gain Error (% of FSR)
Nonlinearity = Peak-to-peak deviation of output voltage from best-fit straight line. It is expressed as ratio based on full-scale range.
PSR = Change in V_{OS}/10V x Supply Change

Noise = Spectral noise density x √bandwidth. It is recommended that bandwidth be limited to twice maximum signal bandwidth for optimum dynamic range.

$ERROR_{(ISO)}$ (RTI)		IMR		V_{OS}		GAIN ERROR		NONLINEARITY		PSR		NOISE
$V_{E\,(ISO)}$	$=\frac{1}{200}\left[\frac{500VDC}{140dB}\right.$		+	70mV	+	20V X $\frac{0.25}{100}$	+	$\frac{0.75}{100}$ x 20V	+	3.7mV x 3V x 2	+	$16\mu V\sqrt{120}$ (rms)$\left.\right]$
	$=\frac{1}{200}\left[\right.$	0.05mV	+	70mV	+	50mV	+	15mV	+	22.2mV	+	0.175mVrms$\left.\right]$
Error as % of FSR(1)	$=\frac{1}{200}\left[\right.$	0.0005%	+	0.7%	+	0.5%	+	0.15%	+	0.22%	+	0.00175%$\left.\right]$
After Nulling												
$V_{E\,(ISO)}$	$=\frac{1}{200}\left[\right.$	0.05mV	+	0mV	+	0mV	+	15mV	+	22.2mV	+	0.175mVrms$\left.\right]$
	$=\frac{1}{200}$	37.2mV										
	=	0.19mV										
Error as % of FSR	$=\frac{1}{200}\left[\right.$	0.0005%	+	0%	+	0%	+	0.15%	+	0.22%	+	0.00175%$\left.\right]$
	=	0.37% of 50mV										
Total Error	=	$V_{E\,(OPA)}$	+	$V_{E\,(ISO)}$								
	=	0.13mV	+	0.19mV								
	=	0.32mV										
	=	0.64% of 50mV										

BURR-BROWN®
APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

HYBRID ISOLATION AMPS ZAP PRICE AND VOLTAGE BARRIERS

Two Hybrid Amplifiers Cut a Novel Path to High-Voltage Isolation. They Spare Designers From Having to Engineer Difficult Solutions Themselves.

If any device tests an analog designer's ingenuity, it is an isolation amplifier. Its job is to pass precise analog signals—safely and without degradation—between two points that may differ by hundreds, even thousands, of volts. Even though the high voltage may be damaging and noisy, it is often there by design, and sometimes because of a fault in the system.

Ideally, an amplifier should be small, hermetically sealed, reliable—and inexpensive. Standard devices have included modular and hybrid isolation amplifiers, now available for more than 10 years. Yet because of the stringent requirements of most applications, some 80% of all amplifiers in use are in-house designs.

A family of isolation amplifiers aims at relieving engineers of the chore of designing their own. The family's first two members, the ISO102 and ISO106, are rated respectively at 1500V and 3500V. Both are unity-gain buffers. Each device is easy to make, electrically and mechanically rugged, inexpensive, and isolates better than any now available by an order of magnitude.

As three-chip hybrids, the amplifiers have from the start been designed to solve economically the problems that up to now have limited the use of off-the-shelf units. Key to keeping costs down is a capacitive-coupling approach to isolation. Any amplifiers so far available with the same capabilities are costly, enlisting magnetic or optical techniques to bridge the high-voltage barrier. Whether hybrids or modules, they are all multidevice circuits requiring complex assembly procedures.

The least expensive competitive device, for example, is rated at half the ISO102's rms voltage, yet costs twice as much.

The two new units, on the other hand, combine innovative packaging to their novel approach to high-voltage isolation. Each of the amplifiers is housed in a low-profile, side-brazed 0.6" wide ceramic DIP. (see "Building a Hermetically Sealed Isolation Amp").

DIFFERENT VOLTAGE, DIFFERENT LENGTH

The only physical difference between the two amplifiers lies in the different lengths needed for withstanding their respective isolation voltages—the voltage across the barrier. The ISO102 is in a 24-pin package, the ISO106 in one for 40 pins. However, to maximize isolation, all but 16 pins—8 at each end of the packages—have been eliminated. External spacing between conductive materials on opposite sides of the barrier is 390 mils for the 1500V ISO102, 1180 mils for the 3500V ISO106.

Because of that construction, their isolation-mode rejection ratio (IMRR), a key specification similar to common-mode rejection ratio (CMRR), is guaranteed to be at least –125dB at 60Hz. (The IMRR is found by taking the change in the amplifier's output-signal voltage caused by a change in the voltage across the barrier, and dividing it by the barrier-voltage change.) While not a function of ambient temperature, IMRR, like CMRR, rolls off with frequency at 20dB per decade. However, unlike that of most other amplifiers, the IMRRs of the ISO102 and ISO106 hold their value at the rated isolation voltage.

Another unusual feature, even among hybrids built on ceramic substrates, is that they are hermetically sealed. Furthermore, many other devices incorporate organic packaging materials and therefore are subject to something called partial discharge, which can degrade a barrier continuously exposed to high AC voltages.

It is important to understand partial discharge when using isolation amplifiers. The phenomenon takes place as a localized breakdown of material, but the breakdown does not bridge the space across the barrier. The discharge-inception voltage depends on the insulation material and can be significantly less than the rated breakdown voltage.

Experiments show that a typical barrier's breakdown voltage will actually decrease with time if continuously exposed to partial discharge. Thus, for maximum reliability the isolation barrier must not be operated at an AC voltage beyond the point at which partial discharge starts.

Voids in the insulating material set the stage for the problem. Alternating electric fields can generate a localized plasma within the voids. A short burst of current flows for about 50ns as the pockets of plasma form, and measurement of this current indicates that partial discharge is taking place. The plasma is usually destructive because ionic bombardment of the walls of the void creates excessive temperature on the wall surface.

Because the barriers of the ISO102 and ISO106 are made of ceramic they are not only virtually free of voids, but also able to stand high temperatures over long periods without damage. Moreover, partial discharge is much more prevalent in barriers insulated with organic materials, which are impossible to fabricate without voids and therefore more damageable by plasma.

In another innovative technique, the ISO102 and ISO106 feature coupling capacitors that jump the isolation barrier by using frequency modulation, a technique previously untried in isolation amps. The capacitors are simply 3pF thick-film devices deposited on the ceramic substrate at the time its tungsten metallization is laid down. The capacitors take the place of transformers or of a combination of LEDs and photodiodes.

The signal through the capacitors is a 1MHz frequency-modulated square wave; in effect, it is a pseudo-digital waveform. It takes three proprietary chips to modulate and demodulate the ±10 input signal—one of them a phase-locked loop, the other two are voltage-to-frequency converters. One of the three, the encoder (which is the FM modulator) to which the floating signal is applied, is a voltage-controlled oscillator (VCO) with a center frequency of 1MHz (Figure 1). The ±10V input modulates the 1MHz signal ±500kHz. The VCO's output is through a pair of complimentary pulse trains, f_o and $\overline{f_o}$, that drive the two tungsten capacitors. The decoder on the other side of the barrier is formed by the phase-locked loop (PLL) and the second VCO.

The PLL chip contains a sense amplifier, the loop circuitry, and an output filter. The sense amplifier reshapes the pulse trains after they have been high-pass filtered by an RC network formed by the barrier capacitors and the chip's 3kΩ input resistors. The sense amplifier drives a digital phase and frequency detector that guarantees rapid phase-locking. The detector's output, in turn, feeds a 70kHz loop filter that drives the feedback VCO.

The pair of VCOs gives virtually identical transfer functions to modulation and demodulation. The accuracy of the isolation buffer thus depends only on the matching of the VCOs, not on their actual transfer function. The PLL forces the feedback VCO to run at the same frequency as the encoder VCO, something that occurs when the two have the same input voltage. The input voltage to the feedback VCO becomes the output (V_{OUT}) of the isolation amplifier after a second-order Butterworth low-pass filter removes residual carrier noise.

Each VCO chip also contains a 5V, 10ppm/°C reference that controls the buffer's input and output offset voltages. The references are in effect independent 5V sources, each of which can supply up to 5mA to external circuits.

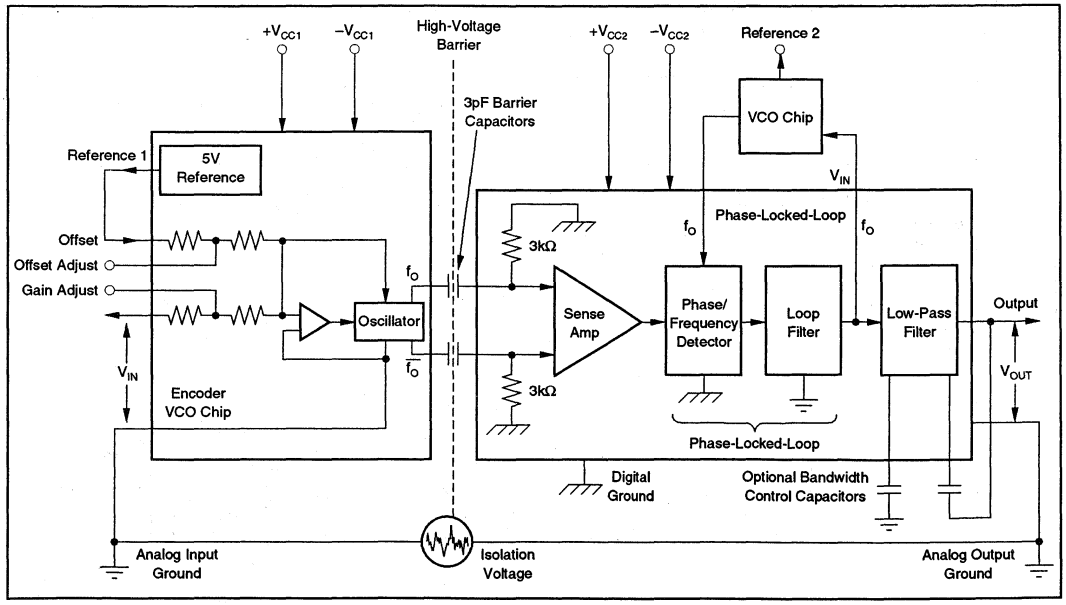


FIGURE 1. The ISO102 and ISO106, Respectively Rated 1500V and 3500V, Transport Their Analog Input Signals Across the High-Voltage Barrier on a Pair of 3pF Tungsten Capacitors. To feed the input signal through the capacitors, the signal frequency modulates a 1MHz carrier in an encoder VCO; The signal is demodulated on the other side of the barrier by a matching feedback VCO and a phase-locked loop.

The easy-to-use buffers have gain and offset trimmed respectively to within 0.1% and 20mV while the chips are still on-wafer. Gain and offset errors may be trimmed through zero with a pair of input potentiometers.

Nominally, the chips on both sides of the barrier operate from split ±15V supplies; in practice they will operate anywhere between ±10 and ±20V. The device can put out 5mA and swing to within 3V of the rails. Indeed, because only the output supplies limit the swing, input voltage can actually exceed input supply voltage.

By adding a pair of small capacitors on the output side of the buffer, in parallel with the low-pass-filter capacitors, the designer can trade off between system bandwidth and system dynamic range—maximum signal swing divided by the noise floor. Doubling the dynamic range quarters the bandwidth (Figure 1 again); adding 0.01 and 0.02µF capacitors boosts the dynamic range to 16 bits while cutting the bandwidth to 280Hz. Without the two capacitors, dynamic range is typically 12 bits, small-signal bandwidth 70kHz, and the 1MHz carrier appears as a 1mVp-p ripple on the output.

One common configuration for an isolation amplifier is a system with multiple channels isolated from each other as well as from their output side. At the output, the signals feed an A/ D converter and a computer.

One of the eight amplifiers drives an eight-channel analog multiplexer. A 5kΩ potentiometer trims the channel's gain to unity, while one of two 1kΩ potentiometers trims offset voltage to as close to zero as possible. The potentiometers can also trim other gain and offset errors in the channel. In addition, with 300pF and 600pF capacitors connected respectively to the C_1 and C_2 pins, small-signal bandwidth is reduced to 10kHz.

Isolated power for the eight separate amplifiers comes from the PWS740 series of DC/DC converter building blocks. One 400kHz PWS740-1 switch-mode control circuit drives eight PWS740-2 transformers in parallel, one for each channel.

Each transformer's output is rectified by a PWS740-3 diode bridge, while 0.1µF bypass capacitors on the isolation amplifier's power pins provide all the filtering needed. An LC π filter in the +15V line to the controller eliminates conducted EMI from the rest of the circuit.

To maintain a system's accuracy, a designer must take several limiting aspects of the amplifiers into consideration. For example, the modulation and demodulation technique imposes a limit on the isolation voltage's permissible slew rate.

Transients across the barrier that exceed 100V/µs can generate enough common-mode current in the capacitors to overdrive the decoding circuit. The effect is to interrupt accurate signal transmission for a moment, but no damage occurs because the devices are protected for transients to 100,000V/µs.

On the other hand, the rated IMRR prevails in the presence of a 7.5kHz, 1500Vrms sine wave because slew rate across the barrier does not exceed 100V/µs. For a rated IMRR, the rms value of the isolation voltage must be less than 11.3MV

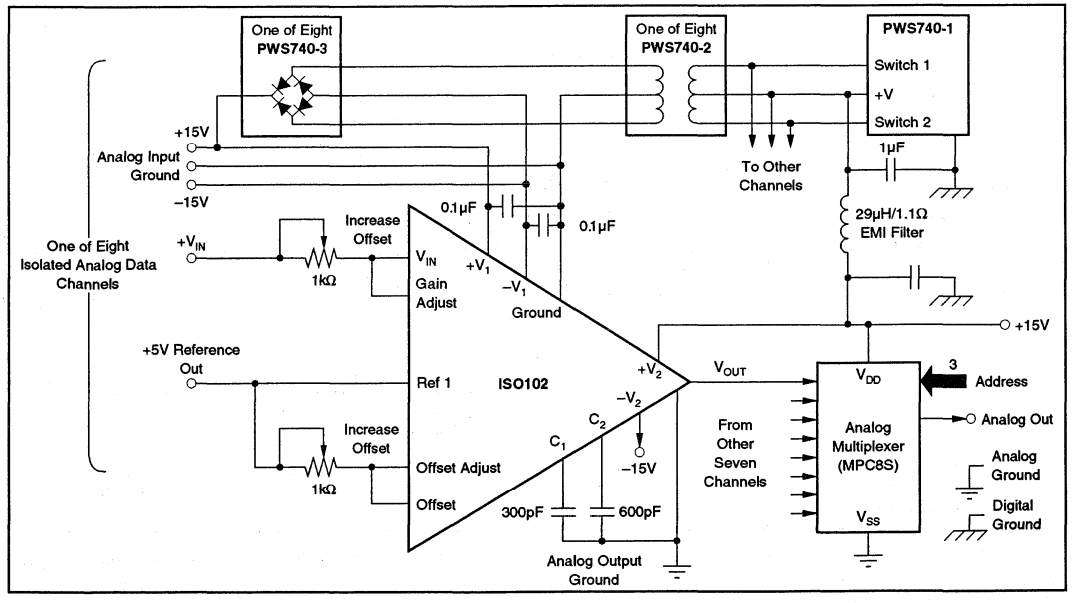


FIGURE 2. The Isolation Amplifiers Lend Themselves to Multichannel Isolated Analog Data Systems. Gain and zero (offset) adjustment potentiometers can handle that job for both amplifier and other channel errors.

divided by the frequency in Hertz, as well as less than the rated isolation voltage.

The slew-rate limit is of concern only when the signal floats continuously on rapidly changing potentials. It need not be considered where isolation is only a factor under fault conditions, as in medical devices.

Typical among isolated systems is the kind with completely floating inputs powered by a high-frequency DC/DC converter, driven in turn by a logic supply on the barrier's output side. The likelihood then is that the supply's ground is the same as the buffer's digital ground.

In such a case, because the primary of the transformer is driven with a fast rising and falling rectangular waveform, the converter capacitively couples a charge to the ground system of its output side (Figure 3). Moreover, the transformer's core and wiring capacitance form a path between the primary and secondary windings.

That path continues through the amplifier and its barrier capacitors to the digital ground. The transformer capacitance in turn forms a voltage divider with the barrier capacitors so that a portion of the switching waveform appears across them.

Any noise spikes between input and output grounds faster than 100V/µs and higher than 1Vp-p, will interfere with the buffer. Spikes can be reduced, however, by using bifilar wire for the transformer's primary and secondary windings; that is, winding each side of the center tap with a pair of twisted wires, rather than one wire. The result is a greater symmetry in the primary to secondary capacitance, reducing the coupled charge. Another method is to use an electrostatic shield between the primary and secondary windings.

BUILDING A HERMETICALLY SEALED ISOLATION AMP

The hardest part of making an isolation amplifier is building the high-voltage barrier. The barrier in the 1500V ISO102 and the 3500V ISO106 is an elegant and simple solution: a pair of 3pF capacitors form an integral part of the DIP that houses the amplifier.

Construction of the package starts with a 0.6" wide ceramic substrate. A layer of tungsten forms the amplifier's pin-to-die and die-to-die connections, as well as the spiral patterns of the barrier capacitors. Capacitance results from the fringing electric fields of adjacent lines of tungsten, which are 0.63mm apart.

Next, a layer of ceramic is fired on top of the substrate, embedding the capacitor in solid ceramic. The material's 15,000V/mm dielectric strength imparts a breakdown voltage in excess of 9000Vrms. The barrier's resistance is typically $10^{14}\Omega$. Windows in this second layer of ceramic form cavities for the amplifier's three integrated circuits—two voltage controlled oscillators and a phase-locked loop.

Metal patterns, including lid-seal rings and lead pads, are screened onto the layer and nickel-plated. The pins are brazed to the sides of the package and all exposed metal is plated with one micron of gold. The chips are then mounted in the finished package. After testing, the lids are soft-soldered over the two cavities, hermetically sealing the amplifier.

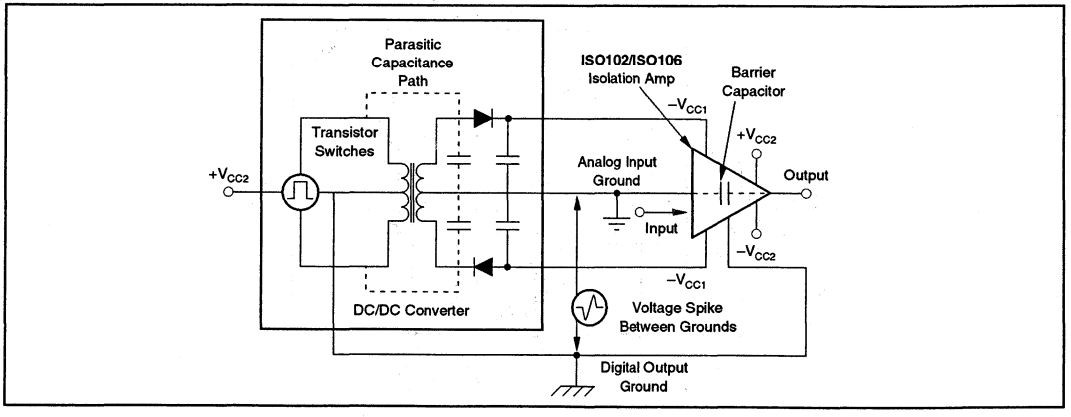


FIGURE 3. In Some Cases, as When a DC/DC Converter Drives the Isolation Amplifier, Voltage Rate of Change is as Important as Voltage Level. The reason is that the transformer's core and the barrier capacitors form a voltage divider, with a portion of the switching waveform appearing across it.

BURR-BROWN®
APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

THE KEY TO UNDERSTANDING SOURCES OF ERROR IN THE ISO100 ISOLATION AMPLIFIER

A Practical Guide to Optimizing Accuracy

While most applications of the ISO100 do not require error correction, being aware of the adjustment options can be beneficial. Provisions for several types of error correction are included to allow the circuit designer to obtain maximum accuracy in a specific application. Adjustments can be made to null errors that are internal to the isolation amplifier, or in other parts of the system.

This application bulletin describes how to quantify the effects of these potential errors, and to help identify the most appropriate means of correction. Each figure has a caption that gives a summary of the important ideas. Subjects to be covered include:

- Theory of operation
- Definition of terms
- Offset current (I_{OS})
- Gain error (A_E)
- Offset voltage (V_{OS})

THE ISO100

The ISO100 has several modes of operation: unipolar or bipolar, voltage or current input, and inverting or noninverting. The product data sheet for the ISO100 includes sections detailing both the error model and the theory of operation. Study of the data sheet is suggested. A simplified block diagram of the ISO100 is shown in Figure 1.

Signal transmission (across the isolation barrier) is accomplished through an optical coupler, which acts as a 1:1 current translator. Current at the input of the device is replicated on the output side of the coupler. The isolated output current (I_{OUT}) is forced to flow through R_F by the summing node action of the output op amp.

At first glance it might seem unusual that the noninverting input of the ISO100 is connected to the inverting input of the input op amp. However, this is due to two inversions in the

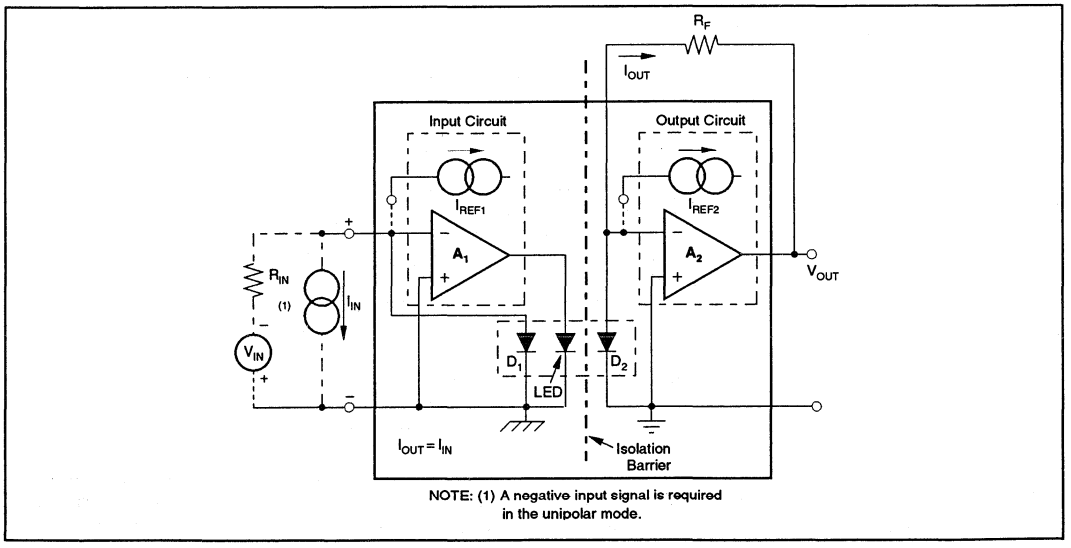


FIGURE 1. Simplified ISO100 Block Diagram. The ISO100 can be thought of as a 1:1 current transistor with its output flowing into a current-to-voltage converter. This isolation amplifier is inherently a current input device. However, since the input is a virtual ground, an input voltage can be converted to a current by simply including R_{IN}. The optional I_{REF} connections are used to produce bipolar operation.

signal path from isolation input to output. Care should be taken not to be confused on this point.

The resulting simplified transfer function for the IS0100 is given by:

$$V_{OUT}/I_{IN} = (R_F)\ (1 + A_E).$$

Gain error (A_E) is defined as the deviation of the ratio, I_{IN}/I_{OUT} from unity. It can be thought of as the "coupling error."

The optical coupler uses a matched pair of photodiodes and a light emitting diode (LED) to produce signal transmission. Since an LED only works when current flows in one direction, the basic mode of operation is unipolar. In the unipolar mode, only negative input currents are allowed (i.e., only currents out of the input produce a positive voltage to turn the LED on). Bipolar operation can be easily produced by internally offsetting the input from zero. Two matched current sources (I_{REF1} and I_{REF2}) are included in the IS0100 for this purpose. By connecting current source, I_{REF1}, on the input side of the coupler, the amplifier is made to operate at half-scale (when the input current is zero). Connecting an equal source, (I_{REF2}) on the output side, shifts the output voltage back to zero. This arrangement maintains a desirable "zero-in/zero-out" relationship, while allowing input currents of either polarity to be accepted.

THE ERROR MODEL

The model used to represent IS0100 errors is shown in Figure 2. Offset current (I_{OS}) is defined as the input current required to make the output voltage zero. In the unipolar mode, it is mainly composed of mismatches in the optical paths. I_{REF1} and I_{REF2} are the current sources that are optionally connected to produce bipolar operation. The major source of bipolar I_{OS} is the mismatch in I_{REF1} and I_{REF2}. The various contributions to the offset current are grouped together and are modeled as a single current source at the input. Keep in mind that I_{OS} has a sensitivity to temperature, supply voltage, common mode voltage and iso mode voltage. However, it would be very rare that all of these factors would be significant. Analysis examples for these terms are found in the data sheet. It will be shown that gain error also introduces an offset current term. Voltage offsets (V_{OS}) are modeled as voltage sources at the inputs of each op amp. I_{D1} and I_{D2} represent the currents being generated by the photodiodes. The currents are related by the equation:

$$I_{D2} = I_{D1}\ (1 + A_E).$$

These are internal currents which mathematically cancel in presenting the total transfer equation. The gain error (A_E) and the unipolar offset current (I_{OS}) cannot be directly altered. However, these terms can be considered constant for each amplifier, allowing their effects to be compensated by simple external means. For instance, the gain error is compensated by adjusting either R_F or R_{IN}. Voltage offset can be trimmed as in most other op amps, using the trim pins provided. Offset current is trimmed by adjusting the magnitude of one of the reference currents (I_{REF1}, I_{REF2}). Because of the on-chip design, sampling or adjusting of the internal references does not have a detrimental effect on the isolation amplifier's performance. I_{OS} trim with an external input current is possible, but careful consideration should be given to the effects of temperature and supply voltage variations. Noise can also be an important error source. While not treated in this application note, information can be found in the product data sheet.

WHAT IS THE OUTPUT?

It is important to be able to calculate total worst case errors for a particular circuit configuration. Clearly, this is important for establishing incoming inspection criteria as well as circuit and system design.

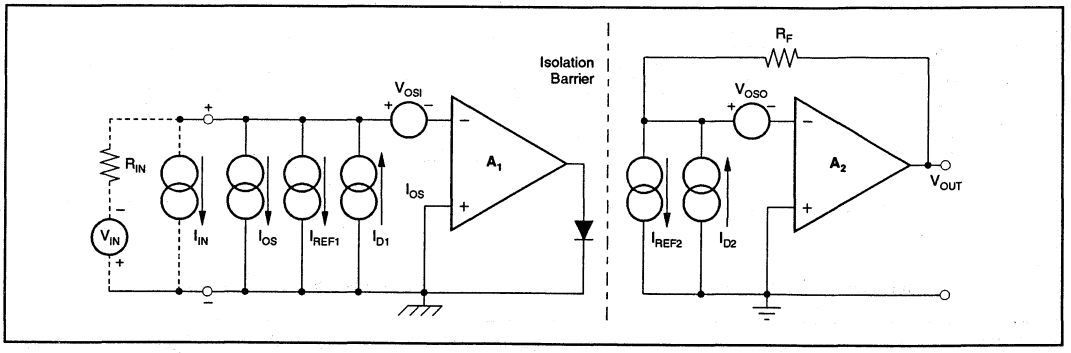


FIGURE 2. DC Error Model. V_{OSI} and V_{OSO} model the respective input offset voltages. There are several possible contributors to offset current. The composite effect is modeled with one current source, I_{OS}, at the input. The gain error (A_E) defines the relationship between I_{D1} and I_{D2} ($I_{D2} = I_{D1}\ [1 + A_E]$). While shown as separate sources, any mismatch in I_{REF1} and I_{REF2} are included in the I_{OS} term.

Equation 2 in the ISO100 data sheet allows the user to solve for the output voltage under any conditions. This transfer equation (for the voltage mode) is repeated here:

$$V_O = R_F[(V_{IN}/R_{IN} + V_{OSI}/R_{IN} - I_{REF1} + I_{OS})(1 + A_E) + I_{REF2}] + V_{OSO}$$

The transfer equation for an input current is:

$$V_O = R_F\left[(I_{IN} - I_{REF1} + I_{OS})(1 + A_E) + I_{REF2}\right] + V_{OSO}$$

By substituting worst case numbers for all the error terms, the maximum error in the value of V_o can be determined as shown in Example 1.

Example 1: An ISO100CP is to be tested at incoming inspection. The part is to be tested in a bipolar unity gain configuration. For the conditions of $R_F = R_{IN} = 1M$ and $V_{IN} = 0$, what output voltage would be within the specification limits?

The maximum values for the error terms are found in the data sheet. Inserting them into the output equation presented above:

$$V_{ERR} = 1M\,[\pm 200\mu V / 1M - 12.5\mu A \pm 35nA)(1 \pm 0.02) + 12.5\mu A] \pm 200\mu V$$

$$V_{ERR} = \pm 286mV\,(\text{maximum})$$

±286mV would then be the range of permissible output voltage in this configuration.

A significant portion of the output error in the bipolar mode is due to the gain error. With no input,

$$V_O \cong R_F[I_{OS} - I_{REF1}(A_E)].$$

The term that dominates is the reference current times the gain error. This error appears as an offset, and must be accounted for if the output is being measured to obtain the actual I_{OS}. Otherwise, the user may wonder why an additional error is present in the output voltage measurement. The next example shows that this is not true for the unipolar mode of operation.

Example 2: Consider a unipolar, non-inverting, gain of one amplifier, as shown in Figure 3A. The output equation can be rewritten for the unipolar case as shown:

$$V_O = R_F[(V_{IN} / R_{IN} + V_{OSI} / R_{IN} - I_{OS})(1 + A_E)] + V_{OSO}.$$

Error analysis proceeds as follows: unipolar operation is not defined at zero input current because the LED could be turned off, disabling the amplifier's internal feedback loop. V_{IN} will be set to the minimum allowed value. The remaining errors are as specified in the data sheet. Note that the $V_{IN\ (MIN)}$ specification of 20mV follows from the 20nA minimum input current specification for linear operation.

$$V_O = 1M\,[(-20mV / 1M \pm 200\mu V / 1M \pm 10nA)(1 \pm 0.02)] \pm 200\mu V$$

$$V_O = -31mV\,(\text{worst case, all errors negative})$$

$$\text{Therefore, } V_{ERROR} = V_O - V_{IN} = \pm 11mV.$$

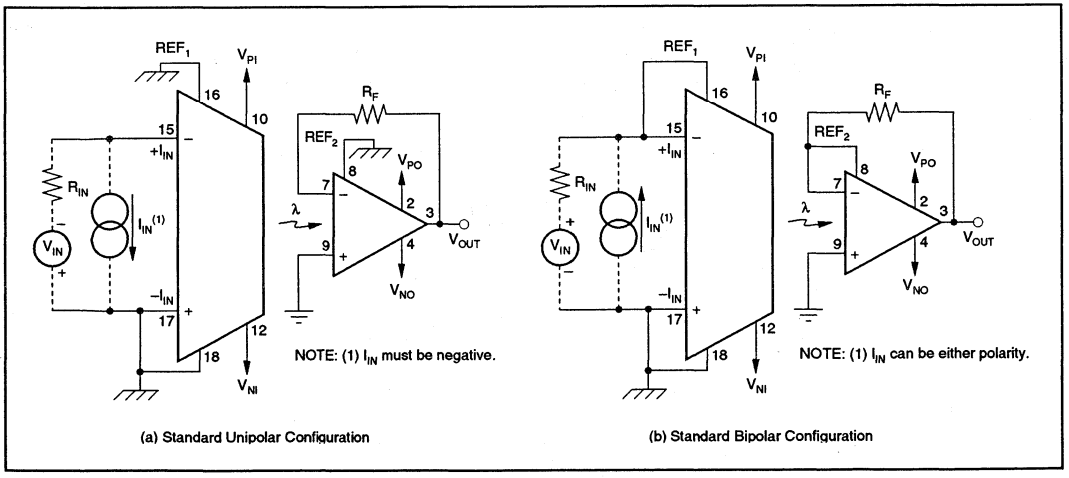


FIGURE 3. Standard Configurations. Most applications of the ISO100 will make use of these configurations, with slight variations. (A) shows the configuration for unipolar operation, which functions for negative inputs only. (B) shows how to use the internal references to provide bipolar operation. The circuits show all necessary connections and indicate the package pin numbers. Note that power supply connections (V_P and V_N) to the input and output and output stages must be "isolated."

CORRECTING THE ERRORS

The next logical step after calculating the errors is to reduce them. In the following discussion, each error is considered by itself. The suggested methods of trimming or adjusting errors are considered, and some general hints are presented.

OFFSET CURRENT ERRORS

Because the ISO100 is a current input device, the dominant error in most configurations will be the input offset current (I_{OS}). As stated above, I_{OS} is defined as the current, injected at the input, necessary to force the output to zero. In the unipolar mode, this definition has a limitation which must be understood. Zero output requires that I_{D2} be zero, implying that the optical feedback path is open. This condition is unsatisfactory for predictable performance. Therefore, a minimum input current must be maintained to assure that the amplifier is operating in its linear region. The transfer function is only defined when the net current at the input node flows out of that node. The unipolar I_{OS} term is extrapolated from this minimum practical current.

In the bipolar mode, no such limitation exists. In this mode the internal references keep the LED and photodiodes running at half-scale when the input is zero. I_{OS} can therefore be measured directly.

I_{OS} ADJUSTMENTS

As suggested above, the internal references can be used to generate a compensation current to cancel I_{OS}. In Figure 4 a current divider is used to divert a small portion of the input stage reference current to the input node. Note that the

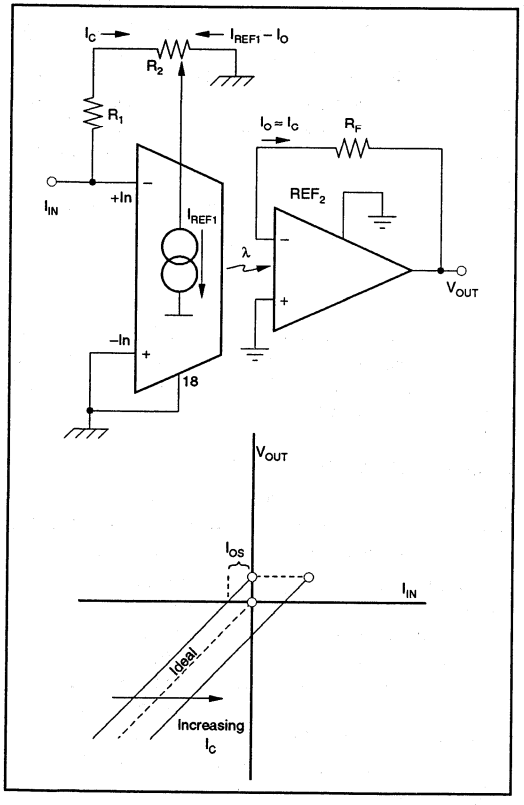


FIGURE 4. I_{OS} Adjustment from the Input Side. If I_{OS} were negative, the ideal transfer curve would be shifted to the left, as shown above. This would cause a positiive output voltage when there was no input current. Connecting a negative correction current, I_C, to the summing node of the first op amp causes the transfer curve to shift to the right. Thus, the effect of I_{OS} can be trimmed out.

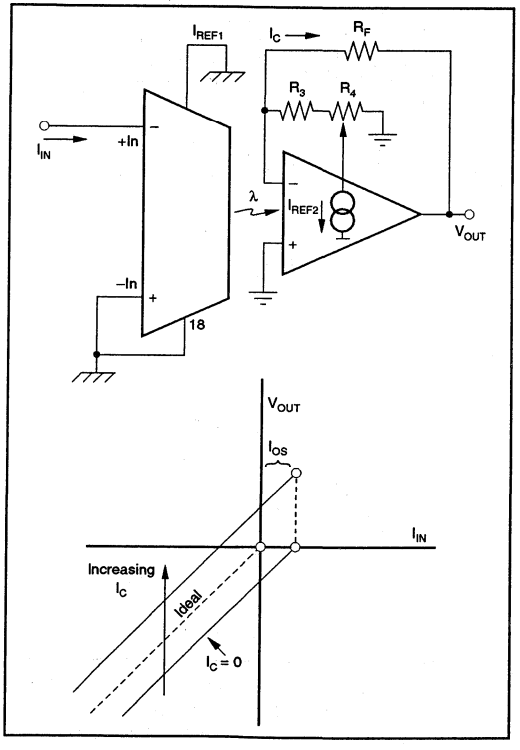


FIGURE 5. I_{OS} Adjustment from the Output Side. Connecting a negative correction current (I_C) to the summing node of the output amplifier causes the transfer curve to shift upward by the amount of I_C. This causes the output to shift back toward zero. Again, a current divider is used to derive the correction current from the internal references. By combining the methods of Figures 4 and 5, a correction current can be generated that will cancel either polarity of I_{OS}.

direction of the current is negative. This additional current flowing out of the summing node behaves like any input signal, and thus causes more current to flow in R_F. The change in V_O is $-I_C$ (R_F), where I_C is the new (offset correcting) current. The graph of the transfer function shows how the curve is shifted by this adjustment.

Since the reference current is of fixed polarity, the curve can only be shifted in one direction with the above connection. However, the curve can be shifted the other way by making use of the output reference ($_{REF2}$). Figure 5 shows the effect of tapping a small current from this source and applying it to the input of the second stage. The nominal value of I_{REF} is 12.5 to 13μA.

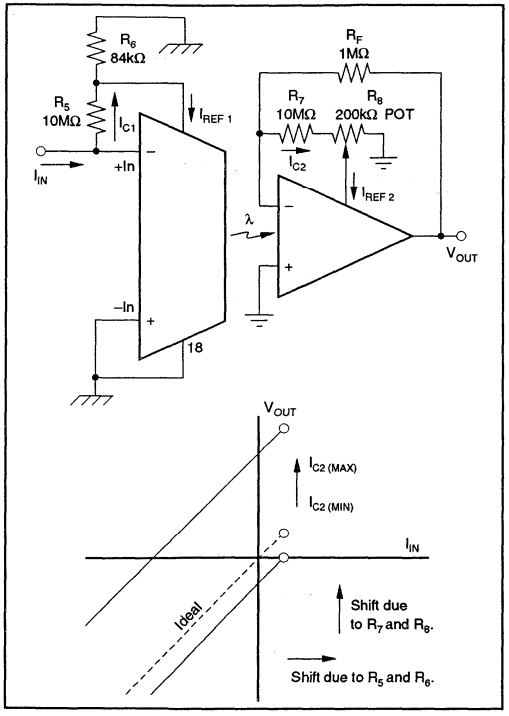


FIGURE 6. Using the Unipolar Amplifier at Zero Input. The unipolar amplifier can be used down to zero input if it is made to be "slightly bipolar." By sampling the reference current with R_5 and R_6 the minimum current required to keep the input stage in the linear region of operation can be established. R_7 and R_8 are adjusted to cancel the offset created in the input stage. This brings the output to zero when the input is zero. While the amplifier can now operate down to zero input votlage, it only has a small portion of the current drain and noise that the true bipolar configuration would have.

By using a combination of these two methods it is possible to always move the transfer curve to the ideal position. In Figure 6, the network in the input stage offsets the system in a known direction. The variable divider network in the output stage has enough range to move the output voltage through zero. It is worth repeating that the correction currents could be generated with resistive dividers connected to the power supplies, but using the internal references takes advantage of their inherent stability, accuracy, and power supply rejection.

Example 3: A common use of the circuit in Figure 6 might be to provide a "keep alive" current for the ISO100. This might be required in a unipolar application where it is possible for the input to go to zero. While it would be a little simpler to use the bipolar configuration, this would result in higher noise and increased quiescent current.

The circuit uses a fixed current divider in the input stage to ensure the direction of I_{OS}. A variable divider in the output stage allows the user to adjust the amplifier to be just "slightly bipolar." Enough current (20 to 30nA minimum) must be drawn from the input to fulfill the minimum unipolar requirement. Since only a small portion of the reference current is being used, a minimal increase in the noise will result.

A suggested value of I_{C1} is about 100nA (1% I_{REF}). Solving the resistive current divider network yields:

$$R_5 / R_6 \cong I_{REF} / I_{C1} = 120.$$

Practical resistor values would be: R_5 = 10M, R_6 = 84kΩ. The adjustment range of I_{C2} should include I_{C1} and the built-in error sources (100nA + 20nA = 120nA). This yields: R_7 = 10M, R_8 = 200kΩ.

GAIN ERROR ADJUSTMENTS

Gain error in the ISO100 is due mainly to mismatches in the optical cavity. These mismatches show up as an error in the ratio of the two photodiode currents (I_{D1} and I_{D2}).

As shown in Figure 7, a gain error will cause the transfer function curve to rotate about the quiescent operating point of the photodiodes. The output stage functions as a current-to-voltage converter with a transconductance (gm) = $1/R_F$. Thus, changing R_F will also cause the line to rotate about the Q point. Therefore, in the unipolar mode, A_E is simply corrected by adjusting R_F.

In the bipolar mode, gain adjustment is not quite so simple. Gain error will still cause the line to rotate about the photodiode Q point, but that point is no longer near the origin. Figure 8 shows that changing either R_F or R_{IN} will cause the transfer curve to rotate about the point where the input current is zero (as it does in the unipolar case). However, if the ratio R_F/R_{IN} is changed to make up for A_E, an I_{OS} term is introduced. This "Apparent I_{OS}" term is due to the fact that I_{REF2} will get divided by the gain error, but I_{REF}

will not. The difference in reference currents, as seen at the input, will be the apparent offset error (see Figure 9). This effect makes the trimming of gain error a two step process for bipolar applications. First, either resistor is adjusted to correct the slope of the line, then the I_{OS} is trimmed using the methods discussed earlier.

V_{os} ADJUSTMENTS

While both the input and output amplifiers of the ISO100 have provisions for adjusting offset voltage, it is generally not necessary to do so because the contribution to total error is small. Only V_{OSI} has practical significance (in most applications), and then only when R_{IN} is small. In most cases the output amplifier is configured so that it has a voltage gain of one, and as such its V_{OS} contribution will be insignificant. The output adjustment range via the V_{OSO} control will be only a few millivolts.

The input offset voltage (V_{OSI}) will affect the output only through its interaction with R_{IN}. V_{OSI} causes a current error equal to V_{OSI}/R_{IN} which is then scaled by R_F. The output voltage is $V_O = V_{OSI}(R_F/R_{IN})$. To adjust V_{OSI} see Figure 10. If R_{IN} is a high value (because the amplifier is in a low gain or has a current source input) the output contribution of V_{OSI} will be minimal. Even in a high gain, where V_{OSI} has a larger effect on the output, the signal/offset ratio is constant.

If the system offset must be adjusted from the output side of the ISO100, the output amplifier can be placed in a gain configuration. As shown in Figure 11, the output voltage

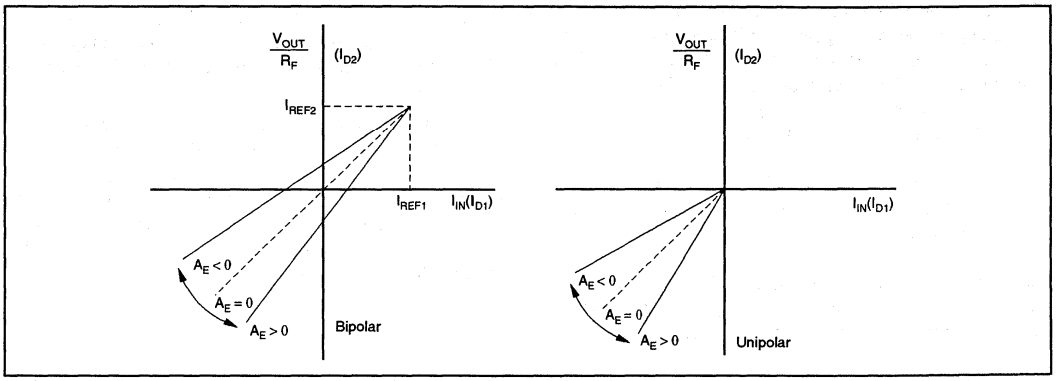


FIGURE 7. Effect of Gain Error (A_E). A_E will cause an error in the slope of the transfer function, rotating the line about a point determined by the quiescent current in D_1 and D_2. Unipolar, this point is near the origin. In the bipolar mode, the internal references cause this point to shift to the right and up as shown above. In either case, the change in slope is the same.

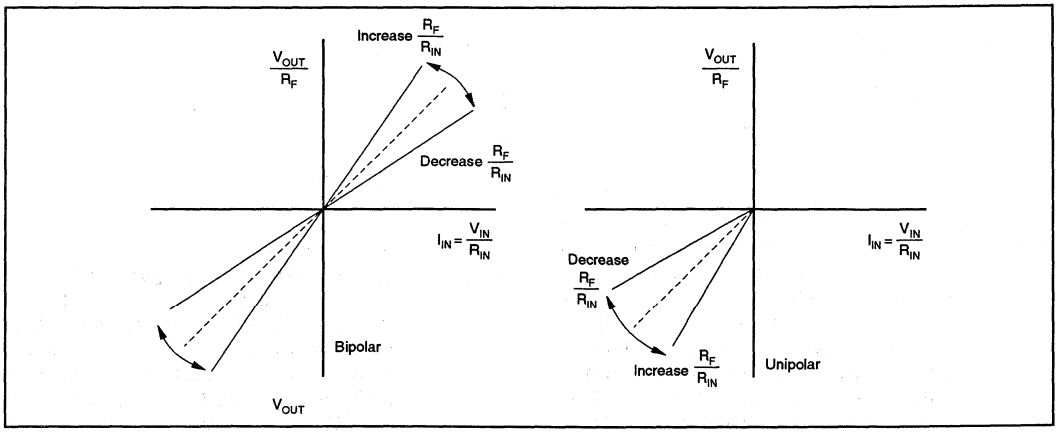


FIGURE 8. Adjusting the Gain. Changing the ratio R_F/R_{IN} will change the gain by rotating the transfer function about the point where $I_{IN} = 0$. This will be true for both the unipolar and bipolar cases. I_{SO} is zero in these examples.

offset (V_{OSO}) is now multiplied by a gain of 1 + (R_F/R_9). If R_F = 1M, and R_9 = 1kΩ, the output will be 1001 times V_{OSO}. This connection does not alter the input signal gain, but it does amplify all output stage errors including V_{OSO} and noise. It is also important to realize that adjusting offset voltage in the ISO100 (and most op amps) causes a change in the offset voltage drift of about 3μV/°C for each millivolt introduced. Offset drift will be amplified by the same gain factors (as the V_{OSI}) above.

Example 4—see Figure 12. Using the methods described previously, the output errors of an ISO100 can be adjusted to zero. In this example, an ISO100BP is in the standard bipolar configuration with a gain of 100. Let R_F = 1M. From the data sheet, the maximum errors are: A_E = 2%, I_{OS} = 70nA, V_{OS} = 300μV.

I_{OS} correction uses a variation of previous techniques. The adjustment not only trims the 70nA of I_{OS}, but also the apparent I_{OS} caused by the gain error. This additional current could be as large as 250nA [A_E (I_{REF}1) = 0.02 (12μA)]. The total trim range should then be 70nA +250nA = 320nA. Because the input of the second amplifier is a virtual ground, R_{12} has the same voltage across it as R_{13}. R_{12} is then:

$$R_{12} = [(R_{13})\ (I_C) \div (I_{REF} - I_C)]$$
$$= 10M\Omega\ (320nA) \div (10.5\mu A - 320nA)$$
$$= 316k\Omega$$

The 10.5μA is the minimum I_{REF} specification on the data sheet. Conservative design allows the R_{10} divider to produce twice the compensation current of the R_{12} divider. Therefore, R_{10} must be twice R_{12}. The calculated value of R_{10} is 632kΩ, so a standard 1M pot is selected.

SUMMARY OF CORRECTION TECHNIQUES—SEE FIGURE 12

To trim I_{OS}, disconnect the input source and let it float. This minimizes voltage offset effects. R_{10} is then adjusted to bring the output to zero.

The gain error can be compensated by adjusting either R_F or R_{IN}. In most circuits it will not matter which is trimmed. In this case R_{IN} will be adjusted via R_G. Allowing for a 2% gain error, R_{IN} should be 2% low with R_G providing a 4% trim range. This makes R_{IN} = 9.8kΩ with 400Ω of trim. Using standard values, R_G would be a 500Ω pot and the fixed resistor will be 9.76kΩ. The gain is corrected by making a known change in the input voltage, and by adjusting R_G for the correct change at the output. Remember that in the bipolar mode there is an interaction between the adjustment of A_E and I_{OS}. Repeat these adjustments until the desired accuracy is obtained.

The last step is to adjust V_{OS}. Because the output stage is in a gain of one, V_{OSO} can be ignored. V_{OSI}, on the other hand, is multiplied by 101 and should be trimmed. R_{14} is adjusted so that there is no shift in the output when the input side of R_{IN} is switched between floating and ground. Any shift is due to the offset voltage causing a current to flow in R_{IN}, which is then gained up to the output .

All errors should now be minimized.

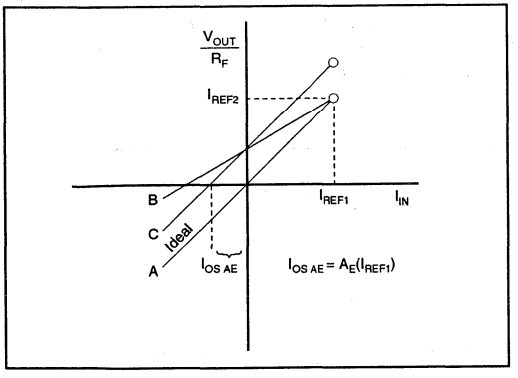


FIGURE 9. Offset Introduced by Gain Error (Bipolar Only). The gain error (A_E) will cause an apparent I_{OS} term to appear when in the bipolar mode. A_E causes the ideal transfer line A to rotate to position B. Adjusting R_F or R_{IN} can correct the slope, as suggested by line C. The line will rotate about the point where I_{IB} = 0. The result is a line with the correct slope, but having an offset equal to I_{REF1} (A_E). This offset term can be adjusted out in the same way as regular I_{OS}.

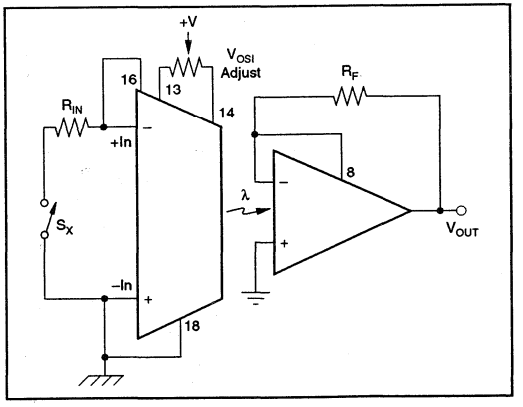


FIGURE 10. Preferred Method for Voltage Offset Trim. In those rare applications where offset voltage is significant, it is best to adjust the input offset voltage, V_{OSI}, as shown above. V_{OSI} and its drift appear at the output multiplied by the factor R_F/R_{IN}. V_{OSO} will usually not be gained up, and thus will not need adjustment. Adjust V_{OSI} until opening up and closing S_X causes no shift in the output voltage.

TEST CIRCUIT

A circuit is shown in Figure 13 that will allow all the major errors of the ISOI00 to be measured.

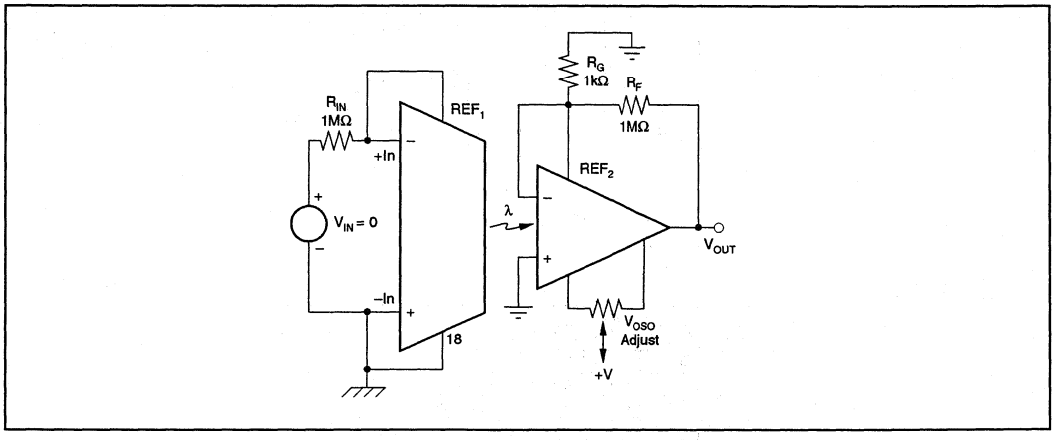


FIGURE 11. Alternate Method for Offset Voltage Trim. If the offset voltage has to be adjusted on the output side of the isolation barrier, the output amplifier can be put in an offset multiplying gain. V_{OSO}, drift of V_{OSO}, and output stage noise appear at the output, multiplied by $(R_F/R_9) + 1$. However, the signal is unaffected. Signal-to-noise ratio could be adversely affected.

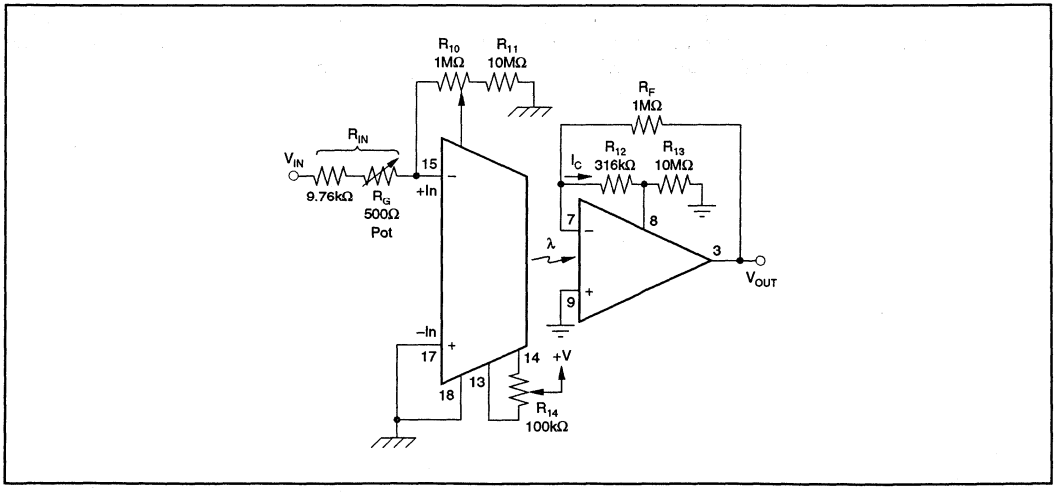
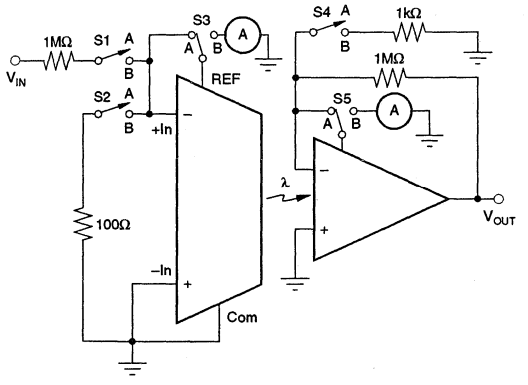


FIGURE 12. Adjusting the Bipolar Errors (Example 4). Each of the errors are adjusted in turn. With V_{IN} = "open," I_{OS} is trimmed by adjusting R_{10} to make the output zero. R_G is then adjusted to trim the gain error. The effects of offset voltage are removed by adjusting R_{14}.



Test	Switches S1	S2	S3	S4	S5	V_{IN}		
A_E	B	A	A	A	A	+10V	$V_{O1} = V_O$	$A_E = (1 - \frac{V_{O2} = V_{O1}}{V_{IN2} - V_{IN1}})$
	B	A	A	A	A	–10V	$V_{O2} = V_O$	
$I_{REF\,2}$	B	A	B	A	B	–10V	$I_{REF\,2}$ = Ammeter Reading	
I_{OS} Bipolar	A	A	A	A	A	—	$I_{OS} = (V_O \div R_I) - (I_{REF1} \times A_E)$	
V_{OSO}	B	A	B	B	B	+1V	$V_{OSO} = V_O/1001$	
V_{OSI}	A	A	A	A	A	—	$V_{O1} = V_O$	$V_{OSI} = \frac{V_{O2} = V_{O1}}{10k\Omega}$
	A	B	A	A	A	—	$V_{O2} = V_O$	

FIGURE 13. Standard Test Configuration. Each of the major errors in the ISO100 can be measured with the circuit shown. The test circuitry is similar in concept to the methods used in the actual production test equipment. To make measurements, the switches are placed in the positions indicated in the table, and the input voltage is set accordingly. The voltage or current reading is then used to compute the error.

BURR-BROWN® APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

IMPROVED DEVICE NOISE PERFORMANCE FOR THE 3650 ISOLATION AMPLIFIER

By Bonnie Baker

The 3650 is an optically coupled, differential input, isolation amplifier having programmable gain. Noise for the 3650 is specified to 4μVrms (typ) on the input stage of the isolation barrier and 65μVrms (typ) on the output stage. The gain of the 3650 is controlled using external resistors on the input stage. In low gains, the noise performance of the 3650 is dominated by the output stage noise figure. The noise performance in high gains is dominated by the input stage noise. By using two OPA627s as a pre-amp to the 3650 isolation amplifier, the noise performance of the isolation circuit is greatly enhanced.

The input bias current noise contribution and the thermal noise of the gain resistors is relatively small and not included in the above calculation. E_{nO} includes the noise contribution due to the optics and the noise currents of the output stage. Because the 3650 uses optics as opposed to a carrier type modulation technique, there is no demodulation ripple at the output of the device.

The output-referred change in total noise vs gain is illustrated in Figure 2. Figure 2 graphically shows the noise performance of the 3650 with gains from 1 to 1000. For high

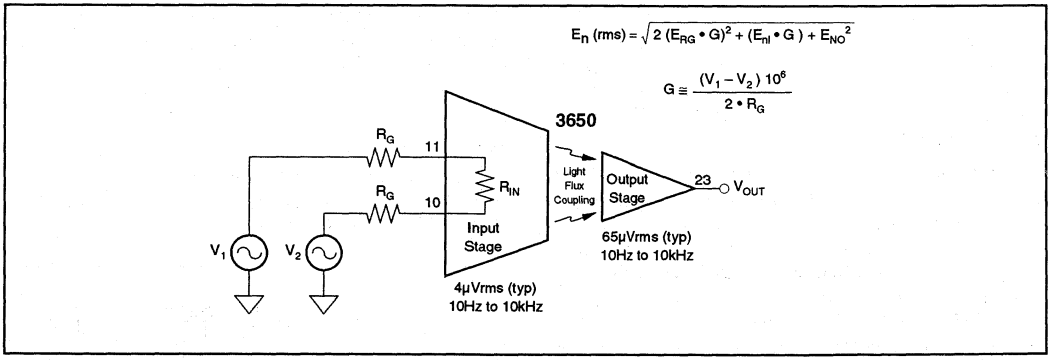


FIGURE 1. The 3650 Isolation Amplifier Has Differential Inputs and Adjustable Gain.

The 3650 has an input section, which can be gained by two external resistors (as shown in Figure 1), and an output section that is essentially kept in a unity gain configuration. The 3650's input noise performance is specified to 4μVrms (typ) times the gain over a 10Hz to 10kHz range. The output stage's noise contribution is 65μVrms (typ) from 10Hz to 10kHz. The 3650 gain can be adjusted from a gain of 1 to a gain of 1000 by adjusting the resistors, R_G. A first order calculation of the noise of the 3650 in various gains is shown below.

$$E_n\ (rms) = \sqrt{(2 \bullet (E_{RG} \bullet G)^2 + (E_{nI}G)^2 + (E_{nO})^2}$$

where:

E_n (rms) = total noise referred to output,
E_{RG} = rms noise of RG,
E_{nI} = rms noise of the input stage of 3650,
E_{nO} = rms noise of the output stage of 3650,

$$G = \frac{10^6}{2 \bullet R_G}$$

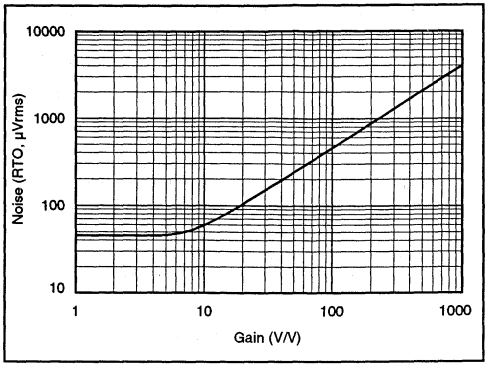


FIGURE 2. 3650 Noise (RTO) vs Gain of the 3650 Isolation Amplifier Shown in Figure 1.

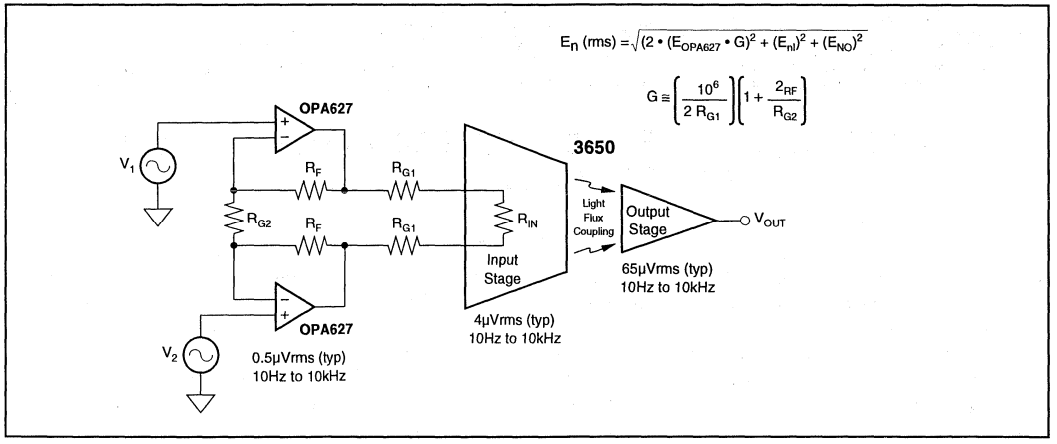


FIGURE 3. By Using Two OPA627s, Noise Performance is Improved for High Gains of the 3650.

values of R_G (or low input stage gains) the total noise referred to the output of the 3650 is dominated by the noise in the output stage, which is specified to 65µVrms (typ). As R_G decreases in value, the gain of the 3650 increases and eventually the noise in the input stage dominates due to the increase in gain. As shown in Figure 2, the effects of the input stage noise starts to dominate as the 3650 gain increases above 10V/V.

If the 3650 is applied in a low gain configuration, the noise referred to output will be optimized; however, it is possible to improve the noise performance in mid to high gains by using a pre-gain stage to the 3650. Figure 3 illustrates a configuration using the 3650 and two OPA627 amplifiers to improve the noise performance of the overall isolation solution. Here the OPA627 is selected because of its low noise performance characteristics; however, a variety of amplifiers could be used instead, depending on the noise requirements of the particular application. Two op amps are configured at the input to the 3650 to preserve the differential input and the programmable gain features that the 3650 offers. The total output noise calculation for this circuit is given by:

$$E_n\ (rms) = \sqrt{(2 \bullet (E_{OPA267} \bullet G)^2 + (E_{nI})^2 + (E_{nO})^2}$$

where:

E_n (rms) = total noise referred to output,

E_{OPA627} = rms noise the OPA627 operational amplifier,

E_{nI} = rms noise of the input stage of 3650,

E_{nO} = rms noise of the output stage of 3650,

$$G = \frac{10^6}{2 \bullet R_{G1}} \bullet \left[1 + 2 \bullet \frac{R_F}{R_{G2}}\right]$$

The change in total noise referred to output vs gain of the circuit in Figure 3 is shown graphically in Figure 4. The effects of the input stage noise starts to dominate as the 3650 gain increases above 50V/V, which is a significant improvement. If the application requires that the isolation amplifier have a gain of 2100, the improvement in noise performance is 3.4.

Noise is a typical problem confronting many isolation applications. By using a differential input stage constructed with two OPA627s, the noise performance of the 3650 is greatly improved for higher gains.

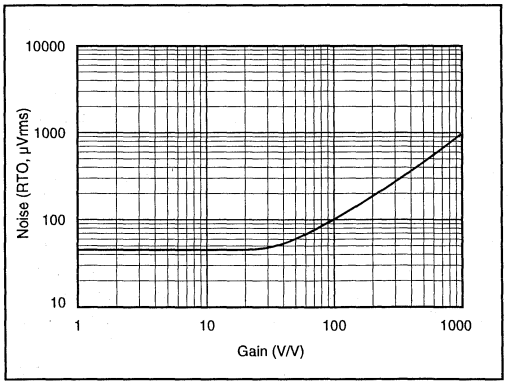


FIGURE 4. 3650 with OPA627 Pre-Amp Noise (RTO) vs Gain of the 3650 Isolation Amplifier with OPA627s Used for Gain as Shown in Figure 3.

BURR-BROWN®
APPLICATION BULLETIN

Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

DESIGN AND APPLICATION OF TRANSFORMER-COUPLED HYBRID ISOLATION AMPLIFIER MODEL 3656

Hybrid-compatible toroid assembly in a flyback-modulated circuit achieves long-term stability, high frequency response, and superior breakdown ratings.

Whenever engineers who need or use isolation amplifiers get together and talk about the improvements they would like to see most, the big three—cost, size, performance—are likely to be mentioned. The industrial or medical equipment manufacturer often has to make a choice of either buying an isolation amplifier or building his own. Cost is the key criterion for such a decision, but there are others as well. For example, the multichannel analog system designer usually runs into printed circuit board space limitations, since he almost always requires a lot of data channels on each PC board. On the other hand, the medical equipment manufacturer is not as concerned with size but encounters very-high breakdown voltages and requires low leakage at a reasonable price.

To meet the widely varying needs of these and other potential users, Burr-Brown has made a radical departure from established design and manufacturing techniques in developing its new isolation amplifier, model 3656. Among the key design features and the resultant benefits for the user are:

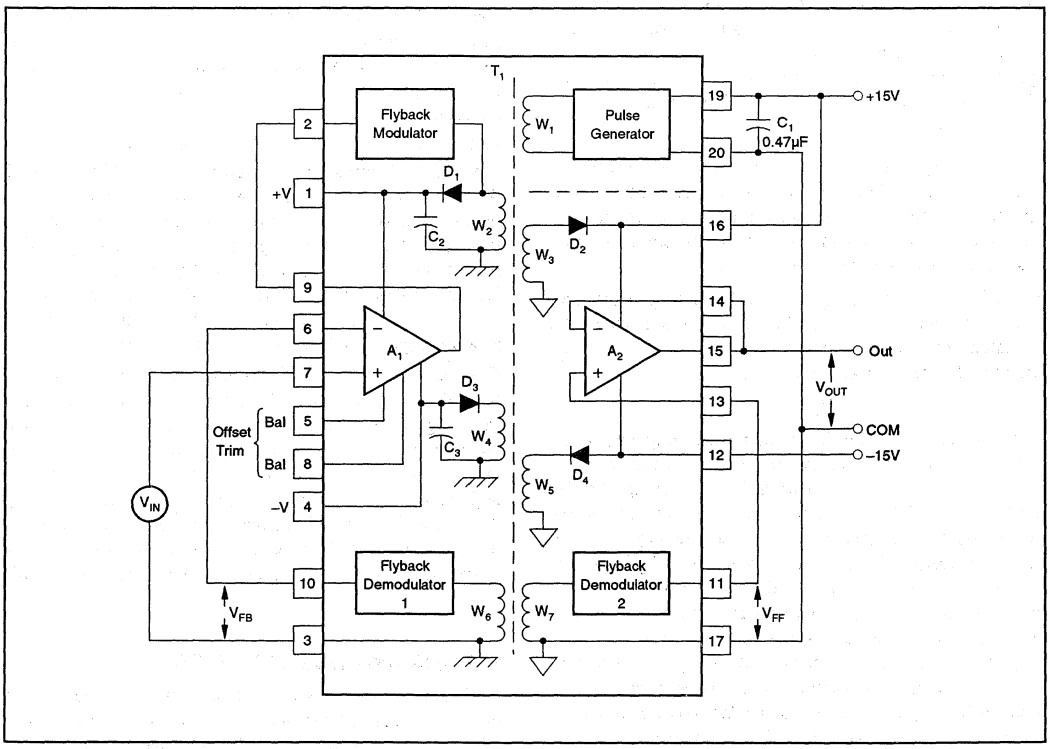


FIGURE 1. Self-contained By Design. Function diagram of hybrid isolation amplifier shows transformer T_1 at its heart and a minimum of external components. Switching rate of 750kHz results in high frequency response and eliminates external filter components.

- A single hybrid-compatible transformer (patents 4,006,974; 4,103,267; 4,082,908) in conjunction with a patented circuit, that couples both signal and power across the isolation barrier, resulting in the industry's smallest and lowest cost isolation amplifier having its own internal isolated power.
- A ceramic thick-film integrated circuit that uses the transformer to provide long-term stability and reliability at low cost.
- True three-port isolator design that achieves unprecedented voltage breakdown ratings and versatility.
- A 750kHz switching rate that results in the highest small-signal frequency response for any isolation amplifier and reduces external filtering requirements.
- A differential design concept that uses two demodulators, one for feedback and one for feedforward, producing accuracies comparable to those of higher priced transformer-coupled devices.

Figure 1 shows the functional diagram of the device in its unity-gain, noninverting configuration with a minimum of external components. A highly inductive transformer, T_1, is excited by the pulse generator containing a solid-state switch that alternately applies an open circuit and the voltage present across filter capacitor, C_1, to transformer winding, W_1, as illustrated in Figure 2a. When the voltage (V) is applied to the winding, the current (i) in the inductance (L) of the winding increases as shown in Figure 2b according to:

$$di/dt = V/ L$$

(Circuit resistances and capacitances have only secondary effects and can be ignored here). At the instant the switch opens, the voltage across the transformer reverses and reaches the magnitude necessary to maintain the current at its previous value. This effect is called flyback.

The flyback voltage (V_F) appears on all windings in the form shown in Figure 2c. Its amplitude is proportional to the instantaneous current and the equivalent resistance (R_p) shunting the transformer inductance:

$$V_F = iR_p$$

The magnitude of V_F can be varied by changing the parallel resistance across any winding of the transformer, resulting in a form of amplitude modulation. This is accomplished by the flyback modulator, which is controlled by input operational amplifier, A_1. Power for A_1 is generated by rectifying the positive energizing pulse appearing across W_2. Rectification is accomplished by diode D_1, and the resultant direct current is smoothed out by C_2 to derive the positive supply voltage. Similarly, the negative supply voltage is derived by diode D_3 and capacitor C_3 from winding W_4. If the isolation amplifier is to be used as a three-port isolator, isolated power voltages for output op amp A_2 can be derived by adding filter capacitors between pins 16 and 17 and between pins 12 and 17.

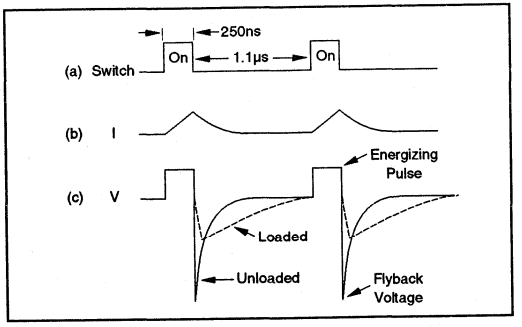


FIGURE 2. Flyback Modulation. The pulsed supply voltage is applied to transformer winding (a). As a result of voltage, V, across winding, current I increases as in (b) until switch opens, producing flyback shown in (c). Rectified positive-going pulses provide power to energize input op amp, A_1, which controls flyback modulator.

At the heart of the isolation amplifier are two identical flyback demodulators. Both compare the positive-going flyback signal at the respective winding at which they are connected with the amplitude of the negative energizing pulse. At minimum modulation (load), they produce a positive output signal; as modulation increases, the demodulator output signal decreases until it is negative at maximum modulation.

Flyback demodulator 1 is used in a closed-loop system by connecting its output to the inverting (feedback) terminal of A_1. This configuration causes A_1, to control the level of the modulator until the output of flyback demodulator 1 equals the signal at the noninverting input of A_1, so that $V_{FB} = V_{IN}$. Flyback demodulator 2, identical to flyback demodulator 1, has the same output, and thus $V_{FF} = V_{IN}$. To prevent loading of demodulator 2, it is buffered by A_2, which is configured as a unity-gain amplifier. As a result, $V_{OUT} = V_{FF} = V_{IN}$.

The accuracy of the transfer equation depends basically on the stability and tracking of the two op amps and the close matching of the demodulator components. With high grade op amps and components matched to within 0.5% or better initially, and a temperature coefficient of 25ppm/°C, a very high gain accuracy can be achieved. Nonlinearity caused by differences in demodulator outputs is very low because of the repeatable matching of the resistors and stray capacitances made possible by thick-film hybrid-circuit technology.

HYBRIDS AND TRANSFORMERS

Until now, transformers and large chokes were to be avoided in hybrid integrated circuits. The few hybrids manufactured with such components are hard to produce and very costly because of the difficulties with size, uneven mounting surfaces, and substrate-to-magnet-wire interconnections. When

Burr-Brown moved to enter the rapidly expanding market for isolation amplifiers and isolated DC/ DC converters with low cost transformer-coupled hybrid circuits, it decided that these shortcomings had to be eliminated. As a result, it developed a new approach to implementing a toroidal transformer on a hybrid substrate that eliminates the manufacturing problems.

Table I is a step-by-step comparison of the new technique with the conventional (but rarely used) approach. At present, the hybrid-compatible transformer is well suited for low-cost, low-power transformers, with the overall cost of the transformer assembly about 60% to 80% of the mounted transformer. However, it does not yet provide the same performance as the conventional transformer in all respects. Although coupling capacitance IC lower and accuracy is better, the resistive losses are higher and the achievable inductance is lower.

COMPARING PAST AND PRESENT

Table II is a comparison of features and specifications of the new isolation amplifier with previously available component-type units. (Note that previously available transformer-coupled isolation amps were built as printed circuits most often housed in plastic modules.) Amplitude-modulated isolation amplifiers were the first to appear. High accuracy pulse-width-modulated types were introduced in 1973, and optical ones have been available since 1976.

It can be seen that the single-transformer, flyback modulated amplifier performs well in most areas. Its nonlinearity is in line with that of all the other types and exceeds that of the low-cost amplitude-modulated types. Its isolation-voltage pulse rating is higher than that of any other amplifier and conforms with the requirements specified in medical applications for protection against defibrillator pulses.

Also, its isolation barrier capacitance is the lowest of any transformer-coupled device available today—a highly desirable feature in medical applications where the leakage from the standard 115VAC equipment power outlets to the patient must be kept at a minimum. Actually, the single transformer design keeps the leakage current below 0.5μA, 20 times lower than the limit specified by Underwriters Laboratories.

Another big advantage of low barrier capacitance is that the isolation-mode rejection degradation is kept at a minimum in applications where the source impedance is high and the isolation amplifier does not have a balanced front end. The isolation-mode rejection of the new unit also compares well with that of previous designs. Another strong point of this device is its small-signal frequency response—an order of magnitude better than any other transformer-coupled isolation amp and even better than optically coupled devices.

CONVENTIONAL TRANSFORMERS	HYBRID-COMPATIBLE TRANSFORMERS
To be mounted into a hybrid package, a small toroid transformer not only must be wound by hand, but all wire must be accurately placed and dressed.	Turns are completed using a manual or automatic wire bonder, cutting labor by 50% to 90%.
The mounting surface of a toroid transformer is formed by the magnet wire, causing problems of tolerance and flatness.	The flat surface of the toroid itself is used for mounting, giving a high degree of uniformity.
The magnet wire bonded to the substrate must hold the core in place and take g stress.	The core is bonded directly to the substrate, resulting in better adhesion and device integrity.
Magnet wire is hard to position accurately on small pads for soldering. The difficultly in making connections and required substrate area increases with the number of connections.	Connections are made with wire bonds. The number of connections does not affect complexity or cost.
Magnet wire must be held in place and soldered.	No soldering is required.

TABLE I. Comparison of Conventional and Hybrid-Compatible Transformers.

INSOLATION METHOD	SINGLE TRANSFORMER	DUAL TRANSFORMER	DUAL TRANSFORMER	DIFFERENTIAL OPTICAL
Package	Ceramic-IC	Plastic - Module	Plastic - Module	Ceramic - IC
Modulaton	Flyback	Amplitude	Pulse - Width	Light-Intensity
Nonlinearity max. specified (%)	0.05 - 0.1	0.03 - 0.3	0.005 - 0.025	0.05 - 0.2
Isolation voltage pulse rating (kV)	8	up to 7.5	up to 5	5
Isolation barrier capacitance (pF)	6.0	20 - 100	16	1.8
Isolation-mode rejection (dB) at 60Hz and Gain = 10V/V	125	115 - 130	140 - 150	120
Frequency response small signal (kHz)	35	1 - 2.5	1.5 - 2.5	15
Size (in^3)	0.33	1.4 - 10	5.6	0.44

TABLE II. Comparison of Isolation Amplifiers.

The innovation that makes it economically feasible to put this isolation amplifier into a ceramic hybrid package is the hybrid-compatible transformer design. Figure 3, a photograph of an uncapped isolation amplifier, shows the location of the transformer, the rest of the components (the op amps, resistors, capacitors, and diodes) and the gold-plated pins. The toroid transformer assembly is the dominant feature in the center. Its turns are made of gold rather than magnet wire—a sharp departure in construction from the state-of-the-art until now. To further illustrate the construction details of the transformer, Figure 4a gives an X-ray type view through the transformer structure from the top, and Figure 4b shows a sectional cut of the assembly.

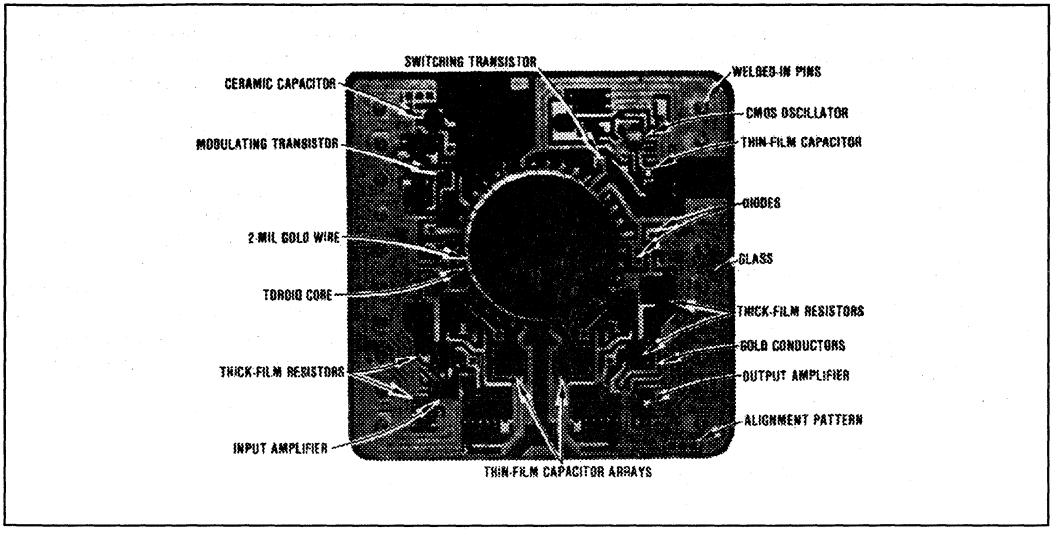


FIGURE 3. Dominant Feature of This Hybrid Integrated-Circuit Isolation Amplifier is Compatible Transformer, Which in Conjunction with the Flyback-Modulation Technique, is Used to Achieve Isolation of Signal and Power with a Single Transformer.

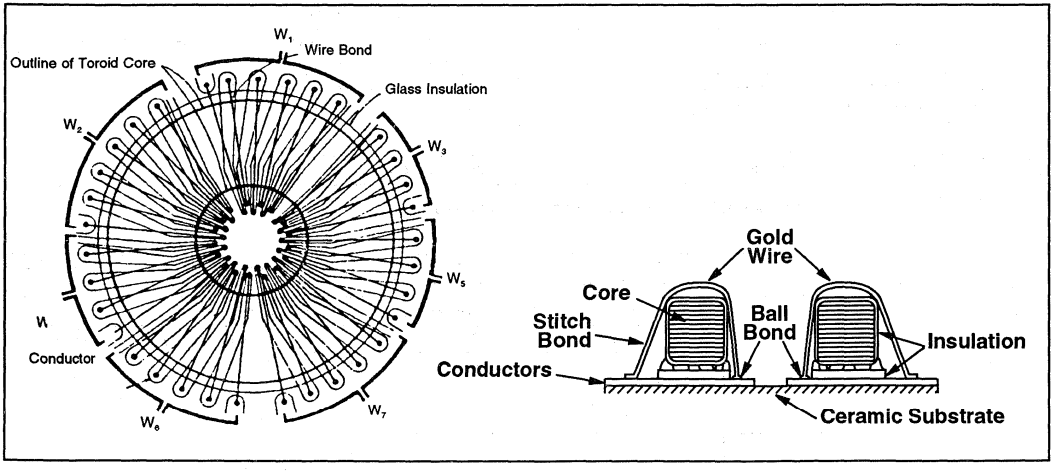


FIGURE 4. Transformer Views. Top X-ray view (a) and cross section (b) show construction of toroid assembly, which provides coupling of signal and power across amplifier's isolation barrier. Turns are of gold wire instead of usual magnet wire and are bonded to screened gold interconnection pattern on ceramic substrate.

MANUFACTURE

Manufacture of the isolation amplifier begins by screening gold conductors onto the ceramic substrate to provide circuit interconnection patterns and the transformer conductor patterns shown in Figure 4a. The gold conductor is then fired in accordance with Burr-Brown's standard thick-film process. The layer of glass insulation is also screened on and fired using thick-film technology. Further processing completes the substrate, which contains 20 laser-trimmed cermet resistors and 19 gold-plated pins, swaged and welded in place.

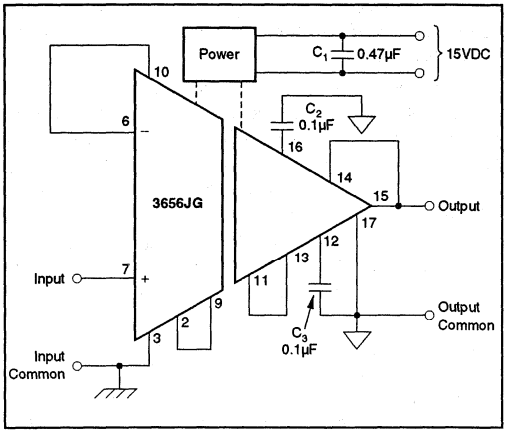


FIGURE 5. Three-port. The 3656, shown here in unity-gain configuration, has a dynamic input and output range of 5V with internally generated power. With external dual-polarity supply, capacitors, C_2 and C_3, can be eliminated.

The first step on the assembly line is the bonding of the insulation-coated toroid to the glass insulation layer. All the other circuit components are then bonded to the substrates. Chip-to-conductor interconnectors are made with 1-mil gold wire and transformer turns are completed with 2-mil gold wire in accordance with the pattern shown in Figure 4a.

Next, the unit is actively laser-trimmed, tested, and insulation-coated with a high dielectric constant insulating material.

The integrity of the transformer under high voltage stress is ensured by the use of several insulation steps. The glass layer on top of the conductors and the insulator coating on the toroid core each have a minimum dielectric strength of 8kV.

Finally, the package is sealed by applying a ceramic cap over the top of the unit under pressure and heat in a nitrogen atmosphere. The heat cures an epoxy ring prescreened onto the ceramic cap to form an airtight seal.

APPLICATIONS

In the two-port unity-gain isolator of Figure 1, only one external filter capacitor (C_1) and a ±8V to ±15V supply are required. With a standard ±15V supply and at unity gain, this circuit provides a dynamic input and output voltage range of ±5V. With two additional resistors, A_2 can be programmed for a noninverting gain of 2, providing a minimum dynamic output voltage range of ±10V.

Figure 5 shows the 3656 connected as a unity-gain, three-port isolator. All isolated supplies are internally generated. C_2 and C_3 filter the internal supplies for output buffer op amp, A_2. If a dual-polarity supply is available at the output port, these capacitors can be eliminated. With the internal supplies as configured, the dynamic input and output voltage range is ±5V.

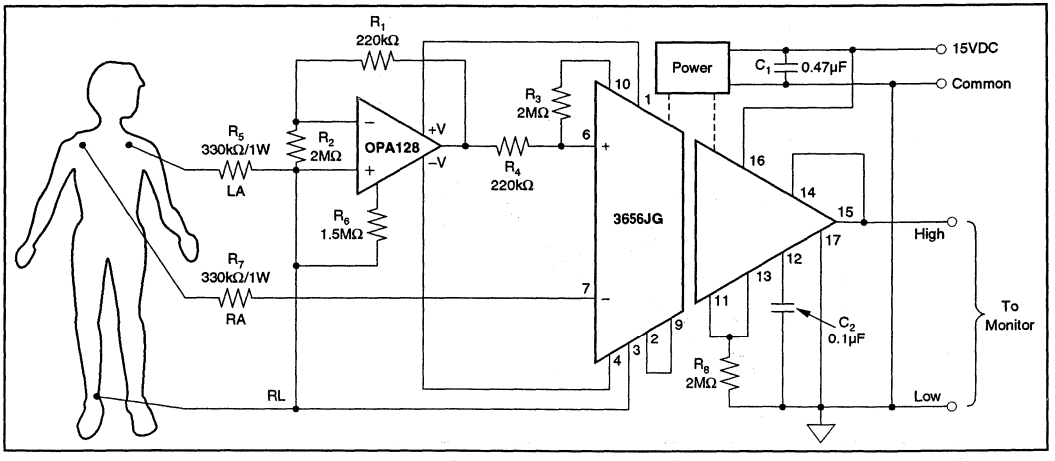


FIGURE 6. Medical Beat. Because of its high isolation, the 3656 is ideal as an electrocardiograph amplifier. It can withstand inadvertent applications of defibrillation pulses while the patient is being monitored. Heart pulses are accurately amplified with a frequency response of DC to 3kHz.

As a result of increased public awareness and increasing government involvement in patient safety, isolation amplifiers have become a must for most electrical patient-monitoring devices marketed today. The 3656 is well suited to such applications because of its low noise, low isolation capacitance, and a high isolation breakdown.

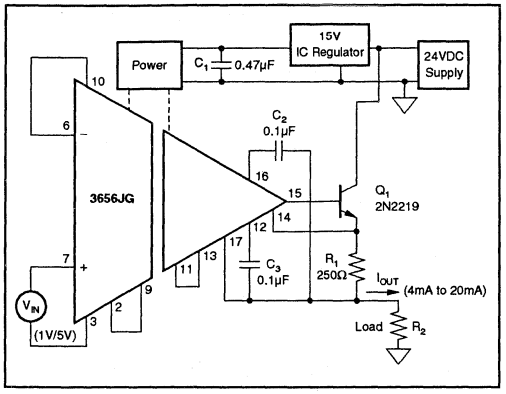


FIGURE 7. Industrial Control. Current-mode signal transmission, often used in industrial control loops, is conveniently implemented with the 3656, here used as a three-port isolator to control current-source transistor, Q_1. Circuit converts 1V or 5V input into a 4mA or 20mA signal.

The electrocardiograph amplifier in Figure 6 is implemented with an instrumentation input stage by using a second low power, low noise op amp (OPA128) in addition to the internal device. Resistors R_3 and R_4 set the noninverting gain of the internal op amp to 10, and resistors R_1 and R_2 provide matching of the external op amp inputs in accordance with standard practice for designing instrumentation amplifiers.

Resistors R_5 and R_7 protect against the peaks of defibrillation pulses, which might be inadvertently applied to the input if a defibrillator is used to restore the patient's heart function while he is being monitored. These resistors must be carbon composition types, because film types of the same rating cannot survive defibrillator impulse energy, which can range up to 2W/s (8kV).

Resistor R_6 sets the quiescent current of A_1, and R_8 equalizes the load of the output demodulator with that of the input demodulator for maximum gain accuracy. Capacitor C_2 filters the internal negative supply for the output buffer op amp, but if a ±15V supply is connected to the output buffer op amp, C_2 can be eliminated.

This circuit accurately amplifies heart pulses with a frequency response of DC to 3kHz. A bandpass filter between amplifier and monitor can select out the desired frequency range.

For electroencephalography, or brain wave monitoring, where defibrillator protection is not required, R_5 and R_7 can be eliminated, resulting in lower noise. But in order for the frequency band to be monitored, the gain must be increased,

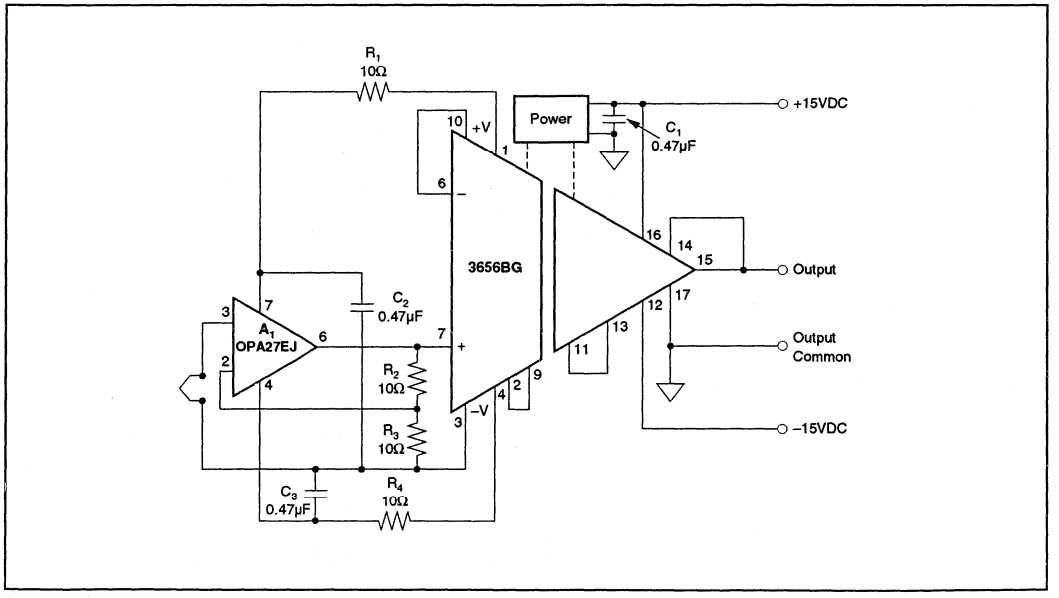


FIGURE 8. Stability. For applications like this thermocouple, where DC stability is important, the isolation amplifier can be supplemented with a high-performance op amp, using the internal isolated power supply, for which capacitors C_2 and C_3 provide additional filtering.

since brain waves are an order of magnitude smaller in amplitude than heart pulses. Increasing the gain is accomplished by bypassing both R_1 and R_4 with an appropriate RC series network. For example, to monitor alpha and theta waves (4Hz to 13Hz) with a gain of 200, two 10kΩ resistors and two 10μF capacitors should be used.

INDUSTRIAL CONTROL LOOPS

Analog signal transmission for industrial control circuits is typically done with 4mA to 20mA loops, where 4mA represents zero or quiescent level and 20mA represents maximum signal. Current-mode signal transmission eliminates inaccuracies that are caused by attenuation in cables, intrinsic safety barriers, and multiple sensors. The shifted zero inherent in the 4mA to 20mA range also makes it easy to recognize abnormal operating conditions such as power down or open circuits. If the transmitted current is not between 4mA and 20mA, an error condition is generally assumed.

Figure 7 shows an isolated 1V-5V to 4mA-20mA converter. All power is derived from a single 24VDC supply. The voltage for the isolation amplifier is regulated to 15V using a standard three-terminal regulator. The isolation amplifier is used with a floating output (three ports) to control current-source transistor, Q_1, and feed its emitter current into grounded load resistor, R_2. The feedback voltage for the internal output buffer is derived across sense resistor R_1 and is proportional to the output current.

For increased DC stability when required in applications like a thermocouple amplifier, the front end of the 3656 can be supplemented with a high performance op amp by using the available isolated supply. Figure 8 shows such a configuration. Resistors R_2 and R_3) set the gain of the front end amplifier to 1000. Capacitors C_2 and C_3 provide additional filtering for the isolated supply—recommended if A_1 draws more than 0.1mA of supply current.

GETTING FULL ISOLATION-MODE REJECTION

A recent analysis of an isolation amplifier to determine the effect of internal- and external-component and stray capacitances on isolation-mode rejection shows that only the capacitances of the input wires to the output circuits are critical. Thus, the major factors for the user are specified isolation-barrier capacitance (C_{ISO}), and the external capacitance between any of the input and output pins.

Designing for high isolation-mode rejection becomes very simple if the isolation amp includes an instrumentation or balanced front end or one is added externally. The balanced front end makes it easy to maintain the full isolation-mode rejection specified because the barrier capacitances from each input-to-output common can be easily balanced. To maintain an isolation-mode rejection close to 120dB with a capacitance unbalance of 0.5pF, a source impedance unbalance of up to 50kΩ can be tolerated.

Maintaining full isolation-mode rejection with a single-ended or unbalanced front end is more difficult. The source resistances in this case must be no more than a few hundred ohms. With large source impedances, degradation can occur in degrees that depend on the circuit, the isolation capacitance, and external stray capacitances.

A simple model of an isolation amplifier with an operational amplifier input stage is shown in Figure 9. Amplifier, A_1, represents the input op amp, and A_2 the unity-gain isolation stage. Specified isolation-mode rejection is achieved if common-mode signal V_{CM} produces no differential input signal between the inputs of A_1, A_2, or both. This is the case if both R_2, R_4, and R_5, and C_1, C_2, and C_{ISO}, are zero. However, when these resistors and capacitors have finites values, they form three low-pass filters, each with the general attenuation function:

$$A = [R + (1/j\omega C)]j\omega C$$

For example, if R_5 = 1kΩ and C_{ISO} = 6pF, the calculated attenuation A at 60Hz is 2.2×10^{-6} or 2.2ppm. Though a few ppm of attenuation seems trivial, note that 1ppm is equivalent to 120dB (20 log 1ppm).

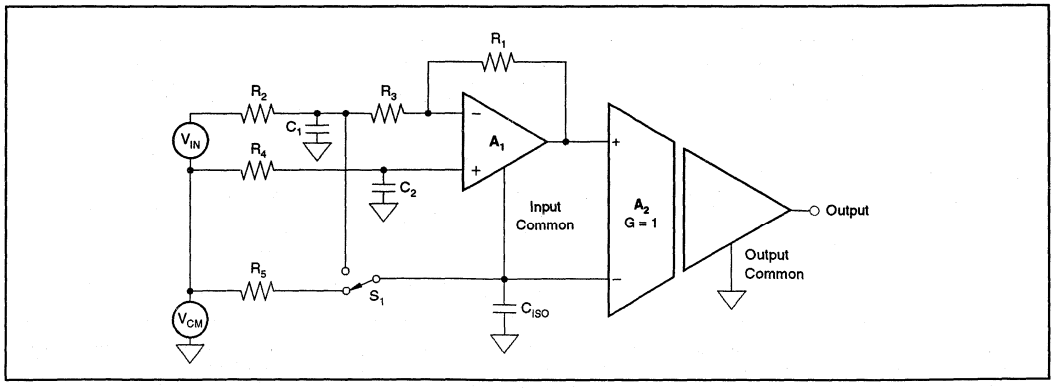


FIGURE 9. Isolation Amplifier Model For Analyzing Isolation-Mode Rejection.

Any differential signal appearing at the input of A_1, because of unequal attentuation of V_{CM} by network C_1-R_2 loaded with R_5 on the one hand, and C_2-R_4 loaded with the noninverting input of A_1 on the other, will be amplified the same as an input signal (V_{IN}). Thus, unequal attentuation can be directly translated into a limit on isolation-mode rejection referred to the input. Any attenuation of V_{CM} caused by low-pass filter R_5-C_{ISO} with respect to the common portion of V_{CM} across the input of A_1 appears across the input of A_2. The gain for this signal is only unity regardless of gain of A_1, causing an isolation-mode rejection degradation with reference to the output.

The three-wire input system in the figure maximizes the isolation-mode rejection of the 3656 or other isolation amplifiers with an unbalanced input, because C_{ISO} becomes less critical with high gain and C_1 and C_2 can be kept small. But, the value of R_2 affects the circuit gain.

If a two-wire system is chosen and the input common is connected to the junction of R_2 and R_3 (S_1 switched), the gain is no longer affected by R_2, but the degradation of balance caused by network C_1-R_2 loaded by R_3 in conjunction with the largest capacitance C_{ISO} is amplified by A_1 and causes much poorer isolation-mode rejection at gains higher than unity.

WHAT IS AN ISOLATION AMPLIFIER?

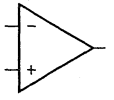
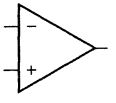
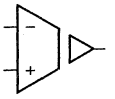
Isolation amplifiers resemble operational amplifiers but are designed to have a galvanic discontinuity between their input and output pins. This discontinuity, called an isolation barrier, must have high breakdown voltage, low DC leakage (high barrier resistance), and low AC leakage (low barrier capacitance).

The isolation barrier sets the isolation amplifier apart from operational and instrumentation amplifiers in cost and complexity, as well as in application. So called three-port isolation amplifiers have an additional isolation barrier between the power supply connection and the signal connections. This feature increases versatility, because it allows the user to connect power in common with either the amplifier's input or its output. In some cases, it may be advantageous to isolate the power supply from the input or the output and thereby eliminate additional error sources that may be present in a system.

Isolation amplifiers generally serve the following functions not achievable with operational or instrumentation amplifiers:

- Sensing small signals in the presence of very high (>10V) or unknown common-mode voltages.
- Protecting patients undergoing medical monitoring or diagnostic measurements.
- Completely breaking ground loops.

Below is a comparison of the three basic amplifier types. The isolation amplifier, as well as offering isolation, increases accuracy because of its floating input. In contrast to the instrumentation amplifier, it not only eliminates ground loop errors, but further reduces the total system error because its isolation mode rejection ratio is generally one or two orders of magnitude higher than the common-mode rejection of an instrumentation amplifier.

	OP AMP	INSTRUMENTATION AMP	ISOLATION AMP
SYMBOL			
FEEDBACK CONFIGURATION	User defined feedback such as voltage, current dV/dt; ∫ Vdt, log V, etc.	Committed feedback. Gain adjustable within fixed limits.	
BASIC APPLICATION	1. General purpose gain element. 2. Buffer. 3. Analog computer.	High accuracy analog sense amplifier when common-mode potentials are smaller than the supply voltage.	1. High accuracy analog sense amplifier for common-mode potentials in excess of supply voltage. 2. Analog safety isolator. 3. Break ground loops.
MAJOR ERRORS	Offset, noise, and common-mode errors independent of gain.	Input and output offset and noise. Total error depends on gain. One set of common-mode specifications.	Input and output offset and noise. Separate common-mode and isolation mode errors except for single-ended input devices.

BURR-BROWN®
APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

ISOLATION AMPS HIKE ACCURACY AND RELIABILITY

Isolation Amplifiers Protect Critical Circuitry From Damage and Enhance Performance

Fault tolerance, transient protection, and interference rejection are valuable features that isolation amplifiers bring to critical circuitry. Two useful examples of how designers can employ isolation amplifiers to improve their systems' performance and reliability are process temperature controllers and electrocardiogram (ECG) amplifiers.

In the case of process control, isolation amplifiers galvanically isolate both the input channel and the current-loop output driver from the controller hardware. Consequently, neither accidental faults from line-powered manufacturing plant equipment to the control system circuitry nor ground loop voltages can compromise the process. In ECG amplifiers, a low-capacitance isolation barrier limits 60Hz leakage current to safe levels, and a high barrier voltage rating protects the monitoring equipment from defibrillator transients and electrosurgery (ESU) interference.

Process control loops, in particular, illustrate a number of ways that isolation amplifiers improve performance and reliability. In unisolated control systems, the long ground lines can develop error potentials across the common impedance that can cause component failure and/or inaccurate control. In contrast, isolating the distributed control systems (DCS) inputs and outputs close to the controller interrupts the dc path, replacing it with the large impedance of the isolation amp's high-voltage barrier (Figure 1).

Similarly, isolation protects the loop from interruption or damage. In the example loop, which is a temperature controller, isolation protects the circuit if the resistance-temperature detector (RTD), a PT100, is accidentally shorted to a grounded metal case or high-voltage conductor. Another possible problem is a fault from the high-potential wire of a twisted pair to earth ground. In addition, high current transients from motors and relays sharing an unisolated system ground can create voltages that exceed the ±1V maximum rating of the two-wire transmitter (XTR).

Isolated control loops also benefit from improved rejection of 60Hz line interference, because low-level transducers are especially susceptible to inductive-loop coupling to the 60Hz magnetic field and capacitive coupling to the electric fields. Not only can the isolation amp prevent system damage, but also the component's isolation-mode rejection (IMR) can attenuate the effect on the output by over 1 million to one.

High dv/dt from inductive current and from radiated electromagnetic interference (EMI) caused by relay arcing are

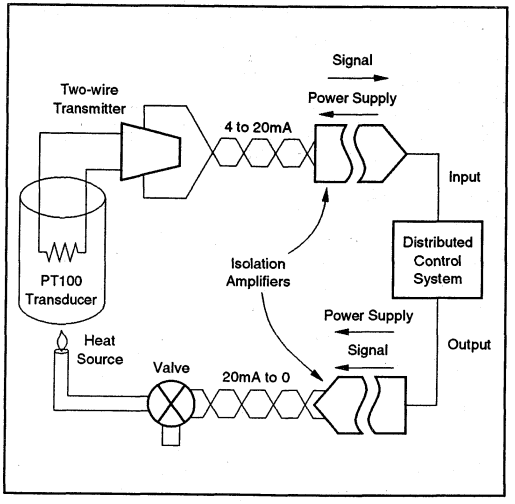


FIGURE 1. Isolating the Distributed Control System in a Process Control Loop Interrupts the DC Path, Blocking Possible Error Potentials that Could Cause Component Failure and Control Inaccuracy.

more difficult to deal with. An isolation amp, however, can reduce their effect on system accuracy, depending on the amplifier's transient immunity. This parameter is defined as the greatest dv/dt that can appear between isolated and unisolated ground before accuracy is lost at the amplifier's output. Few data sheets specify transient immunity, which can vary from 0.1 to 10,000V/µs.

Choosing the best isolation amplifier from process-control applications isn't a simple matter. The common use of 4-to-20mA current loop transmitters and receivers requires an isolated power supply that can supply at least 25mA for the loop and any signal conditioning circuitry. Another consideration is the input supply-voltage range. Some isolation amps need a regulated 15V supply, while others can tolerate sharing an unregulated system supply. The IMR needed depends on the 60Hz line voltage encountered. Most isolation amps specify greater than 100dB rejection at 60Hz, which is adequate for the majority of process-control applications.

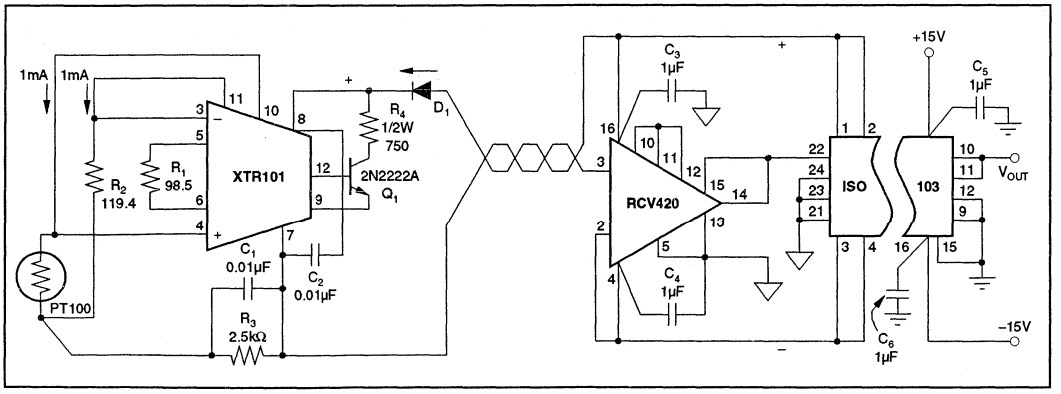


FIGURE 2. In an Example Process Temperature Controller, the Isolated Input Channel Runs from the PT100 Transducer to the XTR101 Two-Wire Transmitter.

TESTS MAY BE NEEDED

As noted, transient immunity is important in process control, with the character of the ground noise determining the level required. If the immunity isn't specified, or is specified at a low barrier voltage, designers must test the amplifier to determine its suitability.

Reliability testing of the barrier integrity varies between manufacturers and their products. For process-control applications, the UL1244 standard calls for 100%, 60Hz ac breakdown testing at the rated voltage for 1 minute. By comparing the isolation amp's test-voltage condition with its continuous rating voltage, designers can judge how conservative the rating is.

Accuracy specifications, however, are relatively uniform. At one time, only expensive discrete modules or in-house custom designs offered better than 0.05% linearity. But recently, small and inexpensive (less than $30) hybrids with comparable performance became available. In some cases, surface-mounting techniques have reduced size and cost. Other designs include custom ICs and high-frequency ferrite transformers that reduce complexity, as well as size and cost.

The isolated input channel of the example control loop runs from the PT100 transducer to the DCS input, beginning with the XTR101 two-wire transmitter configured for the required process temperature of 50°C to 150°C (Figure 2). The PT100 temperature resistance table indicates a resistance of 119.4Ω at 50°C and 157.31Ω at 150°C. One of the XTR101's two 1mA current sources flows through the PT100, so the input amplifier voltage span is 37.9mV.

The span resistor, R_1, is calculated from the input voltage and output current span (4 to 20mA from 50°C to 150°C):

$$R_1 = 40/[(20mA - 4mA)/37.91mV - 0.016m\Omega] = 98.5\Omega$$

The offset resistor, R_2, is equal the PT100's resistance at 50°C: 119.4Ω. The 5V common-mode bias needed for the XTR101's inputs is supplied by R_3 (2mA x 2.5kΩ).

To minimize the temperature rise in the XTR101, the external 2N2222A conducts all but 4mA of the transmitter current. The 750Ω, 1/2W resistor limits the worst-case power dissipation in the transistor to 19.6 x 16mA = 314mW, where 19.6V is V_{CE} and 16mA is determined by the transistor and XTR. Thus, the dissipation is below the TO-18 limit of 400mW at room temperature. For applications at higher ambient temperatures, a 2N6121 in a TO-220 package is a more reliable substitute. This small, current-mode transmitter can be located close to the RTD, with signal and power conducted through one twisted-wire pair from the remote monitoring point to the central controller. At the controller, a proportional analog voltage is reconstructed.

The RCV420 current-loop receiver has an output of 0 to 5V for a 4-to-20mA output. The maximum voltage drop across the receiver's input is 75Ω (the internal resistance between pins 2 and 3) times 20mA, or 1.5V.

ERROR COMPENSATION

The isolation amp, an ISO103, creates both an isolated signal buffer and an isolated dc-dc converter power supply that energizes the XTR101 and RCV420, as well as the ISO103's internal input amplifier. By adjusting R_1 and R_2 for input-temperature-to-voltage accuracy, designers can compensate for gain and offset-voltage errors in the ISO103 and RCV420. The ISO103's high continuous-voltage rating means that the circuit can tolerate line voltages to 1500Vrms. The amplifier's isolation-mode rejection is 130dB at 60Hz, high enough to limit the interference of a 1500Vrms fault to 0.5mVrms, or an error of 0.014°C referred to the input.

Designers can verify the input-channel linearity by measuring the temperature-to-voltage error. The resulting 0.2% error, which equates to a maximum 0.2°C error, is due almost entirely to the temperature-to-resistance nonlinearity of the PT100. If greater accuracy or a wider temperature range is needed, designers can apply an RTD resistance

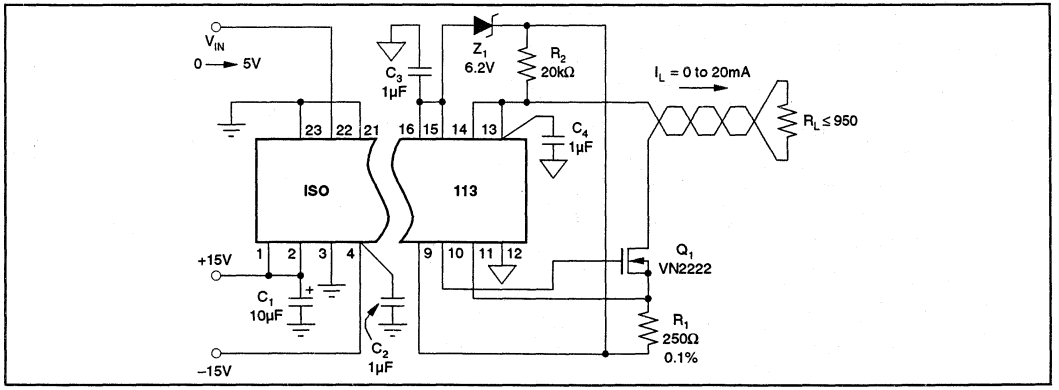


FIGURE 3. On the Output Side, the Process Control Loop Includes an Isolated 0-20mA Loop Driver.

correction factor in the controller, leaving only the 0.04% error from the ISO103.

The output half of the process control loop consists of the isolated 0-to-20mA loop driver (Figure 3). The circuit receives a 0-to-5V input from the controller in the DCS. The driver output current energizes an actuator valve that controls the steam pressure, which regulates the process temperature. Thus, the process control loop is closed by an isolated current-to-pressure converter built around the ISO113 internally powered output isolation amp.

The circuit operates by closing a voltage feedback loop, such that V_{IN} is developed across R_1. This is done by connecting the common pin to one end of R_1 and the sense pin to the other, with V_{OUT} connected to the gate of the VN2222 MOSFET.

To use the maximum compliance voltage at the output, the common pin voltage is referenced off the negative supply with a 6.2V zener diode, Z_1. To keep the zener active when the output current is zero, the driver output current flows through the diode to the negative supply, along with a 1.5mA current from the positive supply through R_2. For the 30V supply in the example, 19V remains across the MOSFET and load, allowing for a maximum load resistance of 950Ω.

The ISO113's input offset voltage, which can be compensated by the controller's transfer function, determines the accuracy of the output offset current ($I_{OS} = V_{OS}/R_1$). Gain accuracy depends on the accuracy and stability of R_1. If adequate care isn't taken, power dissipation in R_1 can degrade the transfer function's linearity.

For example, the temperature change in R_1, for a resistor thermal resistance of 300°C/W is 30°. Consequently, a resistor temperature coefficient of 50ppm/°C causes a 0.15% nonlinearity. To reduce this error, either the resistor thermal resistance or temperature coefficient must be reduced. The thermal resistance can be lowered by connecting four separate 1kΩ resistors in parallel to form the 250Ω resistance, or by using a large wire-wound resistor.

As with the ISO103, the ISO113 is rated for 1500Vrms continuous isolation voltage. Under this maximum interference condition at 60Hz, the 130dB isolation-mode rejection results in a 2µA output-current error, only 0.01% of full-scale and negligible in this application.

Medical instrumentation, although a totally different class of application from process control, illustrates an extreme example of isolation protection that may also be needed in process control, automated test equipment, and data acquisition systems. An ECG amplifier, for instance, is designed to accurately amplify the heart muscle's action potential sensed by surface skin electrodes. A specific design example is an amplifier configured for measuring the difference between the left arm (LA) electrode and the right arm (RA) electrode while driving the right leg (RL) with a small current. This is referred to as the "Lead I" configuration (Figure 4).

AVOIDING INTERFERENCE

Corrupting interference from nearby 60Hz line-operated equipment is minimized by the RL drive amplifier (IC_{2A}), the high input impedance and common-mode rejection ratio (CMRR) of the instrumentation amplifier (IC_1), and the low barrier capacitance of the isolation amp (IC_2). The barrier capacitance, 13pF, also ensures patient safety by limiting 60Hz leakage current from 240Vrms power-line coupling to below 2µArms, which is one-tenth of the Underwriters Laboratories' standard for medical and dental equipment. The electrode input-current limiting resistors (R_1-R_3), the transistor clamps (Q_1 and Q_2, both 2N3904s), and the isolation amp's internal insulation protect the amplifier from defibrillator and ESU high-voltage transients.

The bandwidth needed to faithfully amplify the ECG waveform is 0.05Hz to 100Hz. The low-frequency limit is needed to attenuate slowly varying potentials caused by chemical reactions at the electrode-skin interface. Therefore, the gain of the dc-coupled instrumentation amplifier is set at 10 to prevent the amplified electrode potentials from creating an

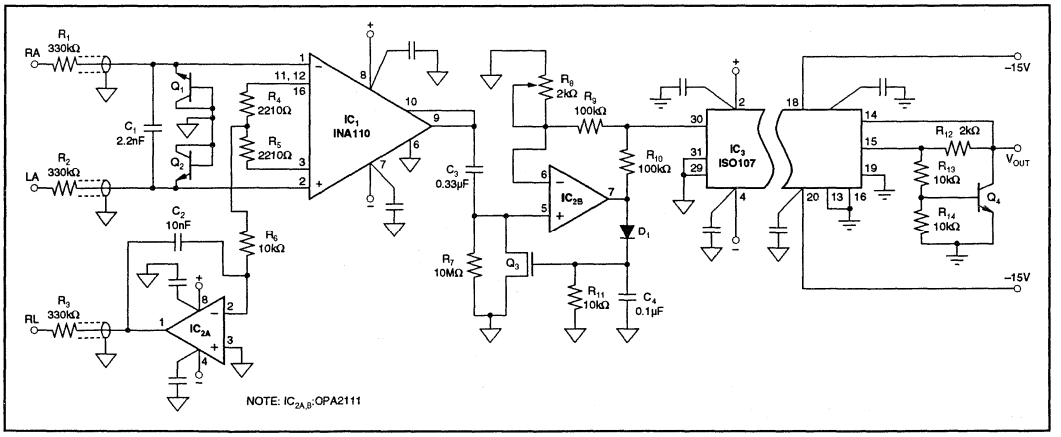


FIGURE 4. In an ECG Amplifier, an Isolation Amplifier Protects the Circuitry and the Patient from Leakage Current from 60Hz Line Operated Equipment and From High-Voltage Transients Caused By Other Equipment.

overload. Input low-pass filtering for differential inputs is performed by R_1, R_2 and C_1. The upper 3dB frequency:

$$= (1/2\pi)/[R_1 + R_2)(C_1)]$$
$$= (0.159)/[(600k\Omega)(2.2nF)] = 110Hz$$

An important consideration is the ECG amplifier's common-mode input impedance. Because the LA and RA electrode impedances can be imbalanced by as much as 100kΩ, the differential signal seen by IC_1 may be in error if the impedance is below 10MΩ. However, the common-mode input impedance of the instrumentation amplifier used, an INA110, is large enough, $2 \times 10^{12}\Omega$, so the cable shield's capacitance of 100pF dominates the ECG amplifier's common-mode input impedance. The resulting reactance of 26MΩ at 60Hz is high enough to prevent errors due to electrode impedance mismatching.

The RL amplifier reduces the 60Hz noise resulting from the magnetic and electric fields surrounding line-voltage sources. Typically, this noise voltage is 0.1 to 1Vp-p, about 100 to 1000 times the ECG signal. The RL amplifier helps reject the noise by reducing the common-mode voltage with negative feedback through the op amp integrator (IC_{2A}).

The amount of loop gain available at 60Hz depends on the compensation needed to stabilize the loop. The isolation supplied by IC_3 reduces the required compensation by adding series barrier capacitance between the patient and earth ground, thereby maximizing the available 60Hz noise rejection.

A pair of gain-setting resistors (R_4 and R_5) create an ac common-mode voltage sense point for the RL drive amplifier. The dc voltage at this point is 1V lower than the inputs, so the driver amplifier floats the patient to +1V relative to isolated ground as a consequence of forcing the common-mode point to zero. The design aims to maximize the RL drive amplifier's gain at 60Hz while maintaining the feedback loop's stability. Using the INA110's gain equation, the gain-setting resistance for a gain of G is:

$$R_4 = R_5 = [20k\Omega/(G - 1) - 25]\Omega.$$

The second amplifier stage (IC_{2b}) is an ac-coupled, variable gain, noninverting amplifier. The lower 3dB frequency is 0.05Hz. The unit used is an OPA2111 JFET input op amp with a $10^{14}\Omega$ input resistance and a 3pA input bias current. These values allow the use of a 10MΩ input resistor without introducing dc errors. With the variable gain feature, designers can set a nominal 1V/mV gain or adjust the output waveform amplitude for patient ECG variations.

This stage includes an automatic-gain-control feedback loop that ensures a rapid recovery from ESU interference. The loop caps the amplifier's output at 2V, a level determined by the MOSFET's threshold voltage (0.8 to 3V), the diode peak detector, and value of R_9. By limiting the output to 2V, the input is kept below 20mV, so C_2 can quickly discharge during transient recovery.

TWO SOURCES OF TRANSIENTS

The ECG amplifier must deal with two sources of high-voltage transients. One is the ESU, essentially a high-voltage RF generator. The other is the defibrillator, which generates electrical pulses.

The ESU has two modes: coagulate and cut. In the coagulate mode, the unit applies a gated 1MHz damped sinusoid to close small ruptured blood vessels with RF heating. In the cut mode, a lower frequency (300kHz) sinusoid with less damping is applied to tissue with a scalpel electrode, facilitating "bloodless" surgery (Figure 5).

The patient lies on a large electrode, supplying a return path for the high-frequency current. Another current path is created by the stray capacitance coupling the primary and secondary windings of the power-supply transformer, which

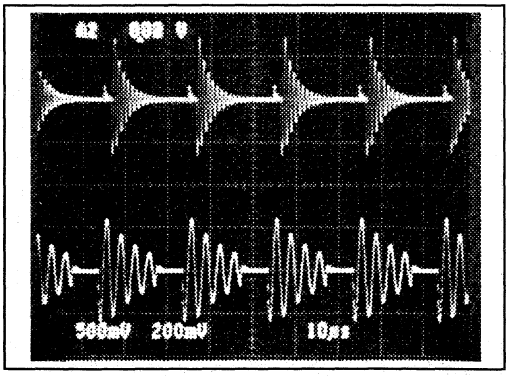


FIGURE 5. An Electrosurgery Unit Generates Two Damped Sinusoids that Can Cause Transients in the ECG Amplifier. The coagulate waveform is at 1MHz (top), and the cut waveform is at 300kHz (bottom).

is connected to line voltage. The isolation amp completes this second path through its power-supply winding capacitance and barrier capacitance.

The defibrillator, on the other hand, charges a 16µF high-voltage capacitor to an adjustable voltage level calibrated in terms of energy (watt-seconds). The capacitor is discharged against the patient's chest through a 100mH inductor and two large metal electrodes, or paddles. The result is an underdamped transient known as the Lown waveform.

The value of this transient is derived by completing the LCR circuit with a 50Ω resistor model for the human body. The voltage that appears between the paddles is the voltage across the 50Ω resistor. For a setting of 400Ws, the capacitor is charged to 7kV, and the frequency of the damped sinusoid is 126Hz. The peak current and voltage turn out to be 69A and 3460V. Some fraction of this transient appears at the ECG electrodes and between the isolated patient ground and the output (earth) ground.

During ESU and defibrillator operation, the two 2N3904 transistors clamp the INA110's inputs at +8V and –0.7V. With no overvoltages present, the transistor's leakage current is less than 100pA. The 330kΩ input resistors limit the peak defibrillator input current to less than 10mA, but they must dissipate 41W of instantaneous power. Fortunately, the defibrillator charges slowly enough to avoid significant resistor heating and damage.

Larger ESU generators, however, can deliver 300W of RF power to the patient. The result is a worst case of 300mW dissipated in the 1/2W input resistors.

The ISO107 supplies an isolated gain of one for the ECG signal and an isolated supply for the INA110 and OPA2111. Besides limiting the 60Hz leakage current, the unit's barrier capacitance limits barrier RF current during ESU operation. The path of the RF leakage current is through the 50pF stray capacitance of the ESU line transformer, the amplifier's power-supply transformer capacitance, and the ISO107 isolation barrier (Figure 6).

The 13pF barrier capacitance conducts a transient current of 57mA peak. Though this level doesn't damage the isolation amp, it corrupts the output signal, because the slew rate of the interference is 4400V/µs. As a result, an output latch is used to ground the output during the interference. When the output exceeds 1.4V, Q_4 (also a 2N3904) conducts, forcing the output to V_{SAT}, which the output sense sees as positive feedback. To release the clamp, the input voltage of the isolation amp must go below ground.

The performance of the ECG amplifier is determined by the frequency response, the common-mode rejection, and the

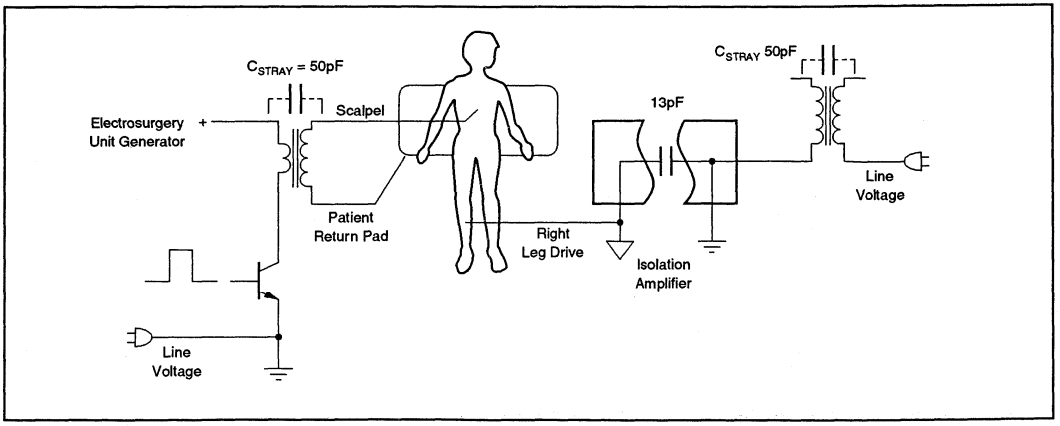


FIGURE 6. Stray Capacitances Coupling the Windings of the ESU and Amplifier Power Transformers Supply Paths for RF Leakage Current.

response to ESU interference and defibrillator pulses. Using the isolation circuitry described, the amplifier's 3dB bandwidth is 0.05 to 100Hz and CMRR ranges from 95dB at 0.05Hz to 80dB at 100Hz.

To simulate a patient load, a 50Ω resistor was placed across the defibrillator output. With a 400Ws defibrillator pulse applied directly between the amplifier's isolated and output grounds, the output clamps and briefly oscillates during the transient, but settles back before the transient ends.

To test the ESU interference response, an ECG simulator was used to apply a test input waveform of 1mV amplitude, and 240beats/min. The isolation barrier RF interference voltage and the ECG output were then displayed on an oscilloscope. The output clamp effectively zeroes the output during the transient, as expected, then releases during the first negative-going input once the RF ceases (Figure 7).

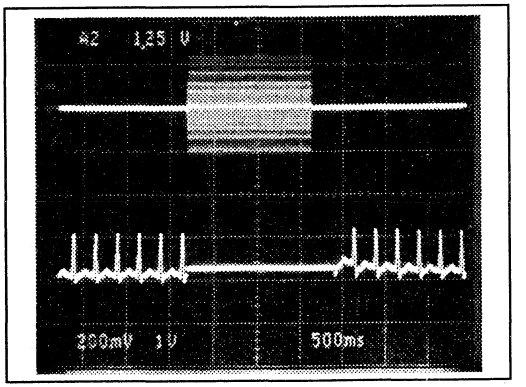


FIGURE 7. With an Isolation Barrier RF Interference Voltage Applied (top), the Amplifier's Output Clamp Zeroes the Output (bottom).

Reprinted from *Electronic Design*, February 22, 1990.

BURR-BROWN®
APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

IMPROVED NOISE PERFORMANCE OF THE ACF2101 SWITCHED INTEGRATOR

By Bonnie C. Baker (602) 746-7984

The signal-to-noise ratio and bandwidth of the combination of the ACF2101 dual, switched integrator and a low-level input current is exceptional when compared to the performance of a classical transimpedance amplifier (Figure 1). To further improve the ACF2101 signal-to-noise ratio, a resistor can be added in series with the input sensor.

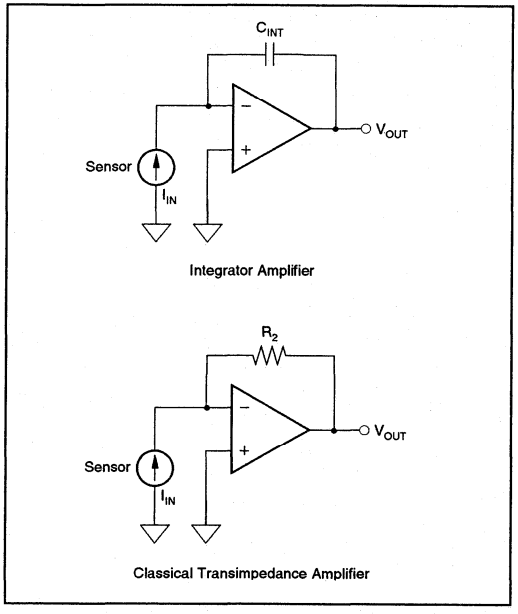


FIGURE 1. Typical Circuits Used to Convert Current Signals to Voltage.

The ACF2101 is a dual switched integrator, as shown in Figure 2. The current from the sensor is integrated by the capacitor (C_{INT}) in the feedback loop of the amplifier. Since the inverting input of the amplifier is kept at a virtual ground, the output of the integrator changes in a negative direction over time. The resulting transfer function of the switched integrator is:

$$V_{OUT} = \frac{-1}{C_{INT}} \int_0^t I_{IN}\, dt$$

Where:

V_{OUT} = output voltage of op amp
C_{INT} = integration capacitor
I_{IN} = sensor current

The output of the ACF2101 switched integrator is a time averaged representation of the input.

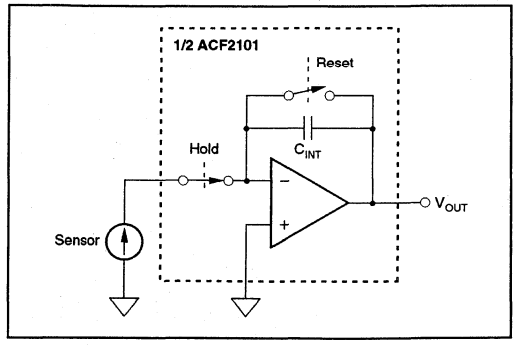


FIGURE 2. The ACF2101 Switched Integrator Block Diagram.

Once the ACF2101 has integrated the input signal over a predetermine period, the HOLD switch is opened, allowing the user to read the output of the switched integrator at a held voltage. The HOLD switch performs a sample/hold function on the signal. Once the signal is read, the RESET switch is closed in order to discharge the integration capacitor, C_{INT}, and bring the output back to the same potential as the inverting input of the amplifier. Once the output returns to ground, the RESET switch is opened. Shortly after the RESET switch is opened, the HOLD switch closes to start the integration cycle again.

Typically, a photodiode is used as the sensor for both circuits shown in Figure 1. A photodiode can be modeled using the sensor model shown in Figure 3. This model includes a current source (I_{IN}), parasitic resistor (R_1), and parasitic capacitor (C_1). Typical values of R_1 range from 100kΩ to 100GΩ. Typical values of C_1 range from 20pF to 1000pF. C_1 can be higher if the sensor is placed at a remote location, and a cable, with parasitic capacitance to ground, is used to transmit the signal to the input of the switched integrator.

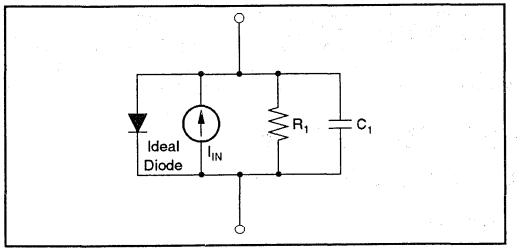


FIGURE 3. Photodiode Model Used in Noise Analysis.

The noise model for the complete photodiode/switched integrator application is shown in Figure 4. In most applications the switched integrator is in the integrate mode for most of the total integration cycle. The model in Figure 4 represents the ACF2101 with the HOLD switch closed and the RESET switch opened. The typical on-resistance of the HOLD switch is 1.5kΩ, and the typical open-resistance of the RESET switch is 1000GΩ.

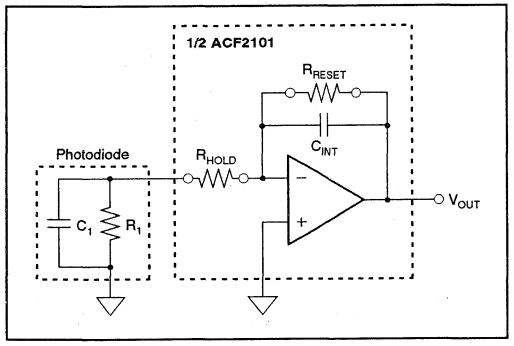


FIGURE 4. ACF2101 Switched Integrator and Photodiode Model Used for Noise Analysis.

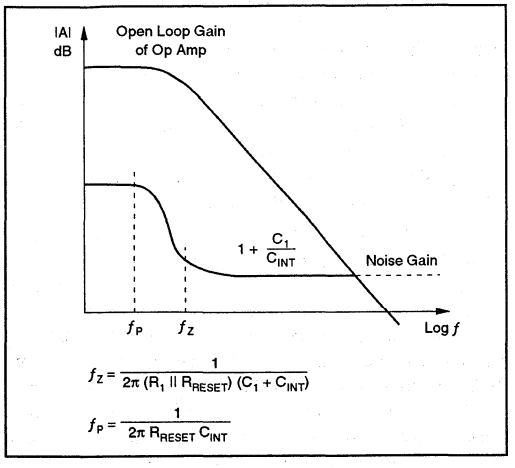


FIGURE 5. Noise Gain of the ACF2101, Switched Integrator.

The three dominate sources of noise at the output of the switched integrator are the gained op amp noise, the charge injection noise of the switches and the $^{KT}/_{C}$ noise of the integration capacitor. A bode plot of the op amp noise gain of the switched integrator is shown in Figure 6. The low-frequency pole of the noise gain is equal to:

$$f_P = \frac{1}{2\pi R_{RESET} C_{INT}}$$

This pole is usually found at very low frequencies. For example, if R_{RESET} = 1000GΩ and C_{INT} = 100pF, the pole would occur at 0.00159Hz.

The zero of the noise gain plot is equal to:

$$f_Z = \frac{1}{2\pi (R_1 \,||\, R_{RESET})(C_1 + C_{INT})}$$

This zero is also usually found at very low frequencies. For example, if R_1 = 100MΩ, C_1 = 50pF, R_{RESET} = 1000GΩ, and C_{INT} = 100pF, f_Z would equal 10.6Hz.

As a consequence, the op amp output noise of the switched integrator is dominated by the high frequency op amp noise multiplied by:

$$\text{High frequency noise gain} = \left(1 + \frac{C_1}{C_{INT}}\right)$$

The total rms noise can be estimated as equal to:

$$\text{NOISE}_{\text{OP AMP}} = 10 \left(1 + \frac{C_1}{C_{INT}}\right) \mu\text{Vrms}$$

The charge injection noise of the switches and the integration capacitor noise both have broad band noise equivalent to 10μVrms. The total characterized noise of the ACF2101 switched integrator with various input capacitance and integration capacitance is shown in Figure 6.

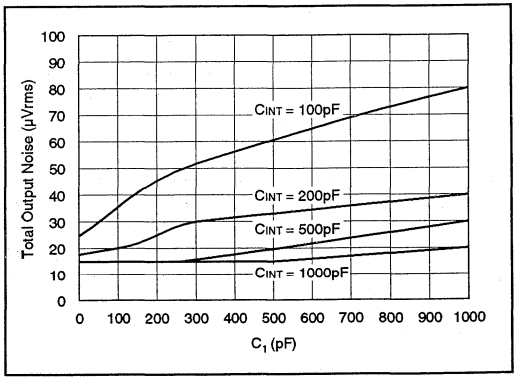


FIGURE 6. Total Output Noise of the ACF2101 Switched Integrator vs Parasitic Photodiode Capacitance, C_1, and the ACF2101 Integration Capacitor, C_{INT}.

To further improve the signal-to-noise ratio of the ACF2101 switched integrator, a resistor can be added in series with the sensor, as shown in Figure 7. This additional resistor, R_N, in series with R_{HOLD}, adds a pole/zero pair at higher frequencies. When R_N equals 0Ω, the pole/zero pair generated by HOLD switch on-resistance (R_{HOLD} = 1.5kΩ) occurs at frequencies close to the open loop gain of the amplifier. As shown in the bode plot in Figure 8, R_N plus R_{HOLD} attenuates high frequency noise.

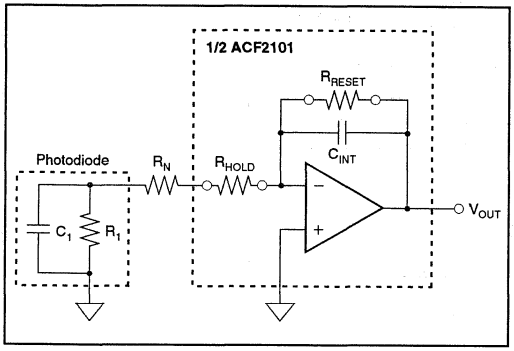


FIGURE 7. The ACF2101 Switched Integrator with an Additional Resistor, R_N, Added in Series with the Photodiode to Reduce Noise.

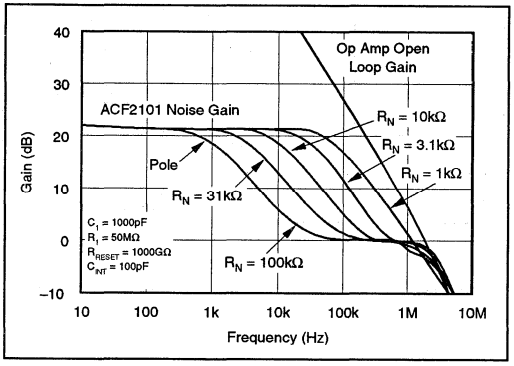


FIGURE 8. Noise Gain Plots of ACF2101 with an Additional Resistor, R_N, in Series with the Photodiode.

An application example is shown in Figure 9. The photodiode is modeled with a parasitic capacitance of 1000pF and parasitic resistance of 50MΩ. The integration capacitor used in the feedback loop of the op amp in the ACF2101 is equal to 100pF. The 20-bit, 40kHz ADC750 A/D converter block diagram is shown in Figure 10. Extreme care should be taken to properly guard the high impedance input pins of the ACF2101 in order to reduce the possibility of coupled noise into the signal.

The design trade-off for improved noise performance of the switched integrator is a slight degradation in the linearity performance of the photodetector. The current from the sensing device will cause an IR drop across R_N. This IR drop will impress a voltage across the sensor, causing a small degree of dark current to start to conduct. As shown in Figure 8, the pole generated by the additional resistor, R_N, is equal to:

$$\text{Pole} = \frac{R_N + R_1 + R_{HOLD}}{2\pi R_1 (R_N + R_{HOLD}) C_1}$$

The pole is directly affected by the value of R_N and C_1 (photodetector parasitic capacitance). Higher values for C_1 will reduce the noise without compromising the linearity performance of the photodetector. The overall circuit performance is best optimized when the photodetector parasitic capacitance, C_1, is 200pF or greater.

The ACF2101 switched integrator is optimized for good noise and bandwidth performance for low-level input currents. The addition of a resistor in series with the photodiode further improves the noise performance without sacrificing bandwidth.

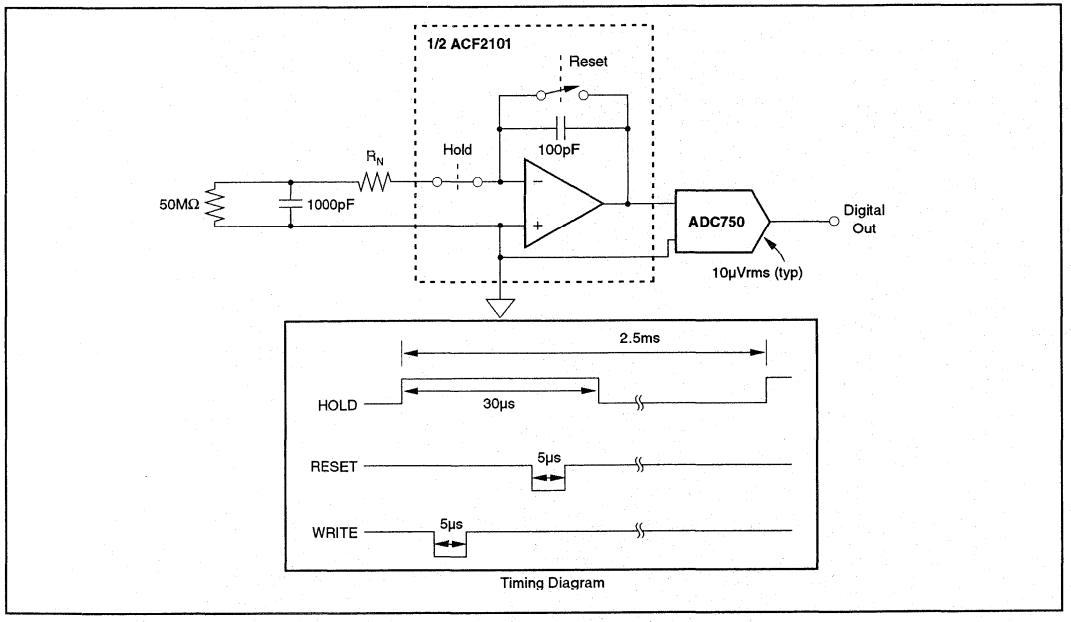


FIGURE 9. Circuit and Timing Diagram used to Test the Noise Performance of the ACF2101 with and without R_N.

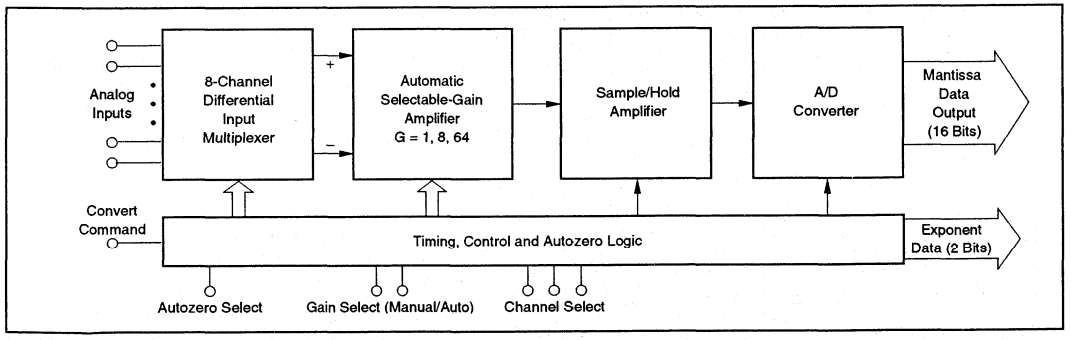


FIGURE 10. Block Diagram of ADC750 A/D Converter.

BURR-BROWN® APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

NOISE ANALYSIS OF FET TRANSIMPEDANCE AMPLIFIERS

The availability of detailed noise spectral density characteristics for the OPA111 amplifier allows an accurate noise error analysis in a variety of different circuit configurations. The fact that the spectral characteristics are guaranteed maximums allows absolute noise errors to be truly bounded. Other FET amplifiers normally use simpler specifications of rms noise in a given bandwidth (typically 10Hz to 10kHz) and peak-to-peak noise (typically specified in the band 0.1Hz to 10Hz). These specifications do not contain enough information to allow accurate analysis of noise behavior in any but the simplest of circuit configurations.

Noise in the OPA111 can be modeled as shown in Figure 1. This model is the same form as the DC model for offset voltage (E_{OS}) and bias currents (I_B). In fact, if the voltage $e_n(t)$ and currents $i_n(t)$ are thought of as general instantaneous error sources, then they could represent either noise or DC offsets. The error equations for the general instantaneous model are shown in Figure 2.

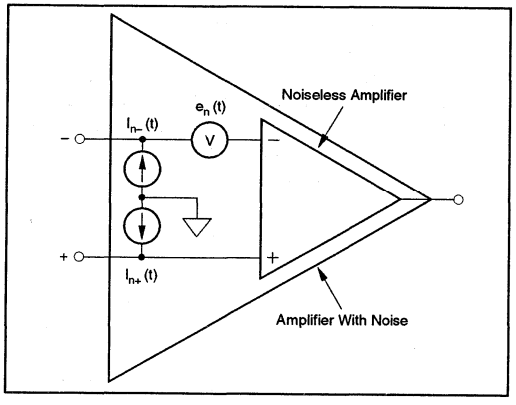


FIGURE 1. Noise Model of OPA111.

If the instantaneous terms represent DC errors (i.e., offset voltage and bias currents) the equation is a useful tool to compute actual errors. It is not, however, useful in the same *direct* way to computer noise errors. The basic problem is that noise cannot be predicted as a function of time. It is a random variable and must be described in probabilistic terms. It is normally described by some type of average—most commonly the rms value.

$$N\ \text{rms} \overset{\Delta}{=} \sqrt{1/T \int_Q^T n^2(t)\,dt} \qquad (1)$$

where N rms is the rms value of some random variable n(t). In the case of amplifier noise, n(t) represents either $e_n(t)$ or $i_n(t)$.

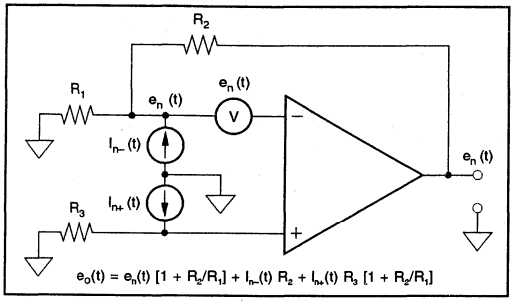


FIGURE 2. Circuit With Error Sources.

The internal noise sources in operational amplifiers are normally uncorrelated. That is, they are randomly related to each other in time and there is no systematic phase relationship. Uncorrelated noise quantities are combined as root-sum-squares. Thus, if $n_1(t)$, $n_2(t)$, and $n_3(t)$ are uncorrelated then their combined value is

$$N_{TOTAL}\ \text{rms} = \sqrt{N_1^2\ \text{rms} + N_2^2\text{rms} + N_3^2\ \text{rms}} \qquad (2)$$

The basic approach in noise error calculations then is to identify the noise sources, segment them into conveniently handled groups (in terms of the shape of their noise spectral densities), compute the rms value of each group, and then combine them by root-sum-squares to get the total noise.

TYPICAL APPLICATION

The circuit in Figure 3 is a common application of a low noise FET amplifier. It will be used to demonstrate the above noise calculation method.

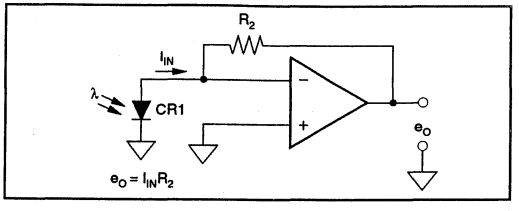


FIGURE 3. Pin Photo Diode Application.

CR1 is a PIN photodiode connected in the photovoltaic mode (no bias voltage) which produces an output current i_{IN} when exposed to the light, λ.

A more complete circuit is shown in Figure 4. The values shown for C_1 and R_1 are typical for small geometry PIN diodes with sensitivities in the range of 0.5 A/W. The value of C_2 is what would be expected from stray capacitance with moderately careful layout (0.5pF to 2pF). A larger value of C_2 would normally be used to limit the bandwidth and reduce the voltage noise at higher frequencies.

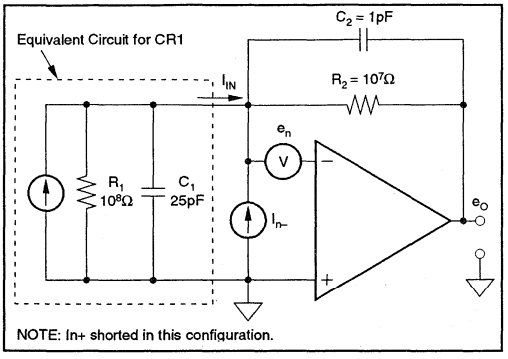


FIGURE 4. Noise Model of Photodiode Application.

In Figure 4, e_n and i_n represent the amplifier's voltage and current spectral densities, $e_n(\omega)$ and $i_n(\omega)$, respectively. These are shown in Figure 5.

Figure 6 shows the desired "gain" of the circuit (transimpedance of $e_O/i_{IN} = Z_2(s)$). It has a single-pole rolloff at $f_2 = 1/(2\pi R_2 C_2) = \omega_2/2\pi$. Output noise is minimized if f_2 is made smaller. Normally R_2 is chosen for the desired DC transimpedance based on the full scale input current (i_{IN} full scale) and maximum output (e_O max). Then C_2 is chosen to make f_2 as small as possible consistent with the necessary signal frequency response.

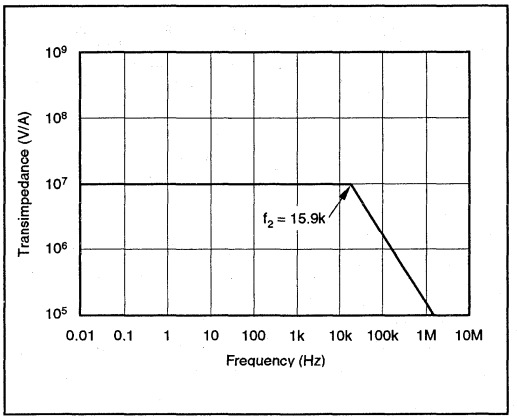


FIGURE 6. Transimpedance.

VOLTAGE NOISE

Figure 7 shows the noise voltage gain for the circuit in Figure 4. It is derived from the equation

$$e_O = e_n\left[\frac{A}{1+A\beta}\right] = e_n\frac{1}{\beta}\left[\frac{1}{1+\frac{1}{A\beta}}\right] \qquad (3)$$

where:

A = A(ω) is the open-loop gain.

β = β(ω) is the feedback factor. It is the amount of output voltage feedback to the input of the op amp.

Aβ = A(ω) β(ω) is the loop gain. It is the amount of the output voltage feedback to the input and then amplified and returned to the output.

Note that for large loop gain (Aβ >> 1)

$$e_O \cong e_n\frac{1}{\beta} \qquad (4)$$

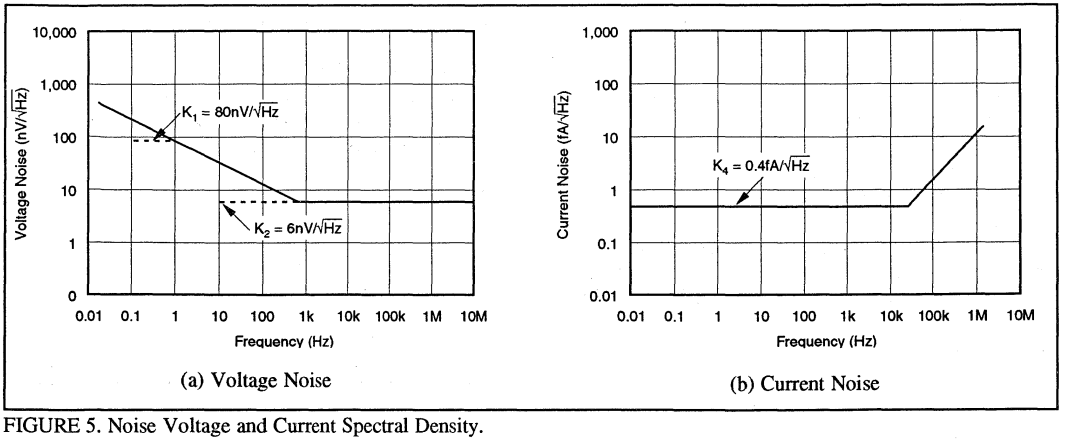


FIGURE 5. Noise Voltage and Current Spectral Density.

For the circuit in Figure 4 it can be shown that

$$\frac{1}{\beta} = 1 + \frac{R_2(R_1C_1s + 1)}{R_1(R_2C_2s + 1)} \quad (5)$$

This may be rearranged to

$$\frac{1}{\beta} = \frac{R_2 + R_1}{R_1'}\left[\frac{\tau_A s + 1}{\tau_2 s + 1}\right] \quad (5a)$$

where $\tau a = (R_1 \parallel R_2)\,(C_1 \parallel C_2)$

$$\frac{1}{\beta} = \left[\frac{R_1R_2}{R_1 + R_2}\right](C_1 + C_2) \quad (5b)$$

and $\tau_2 = R_2C_2$. (5c)

$$\text{Then, } f_a = \frac{1}{2\pi\tau_a} \text{ and } f_2 = \frac{1}{2\pi\tau_2} \quad (5d)$$

For very low frequencies ($f << f_a$), s approaches zero and equation 5 becomes

$$\frac{1}{\beta} = 1 + \frac{R_2}{R_1}. \quad (6)$$

For very high frequencies ($f >> f_2$), s approaches infinity and equation 5 becomes

$$\frac{1}{\beta} = 1 + \frac{C_1}{C_2}. \quad (7)$$

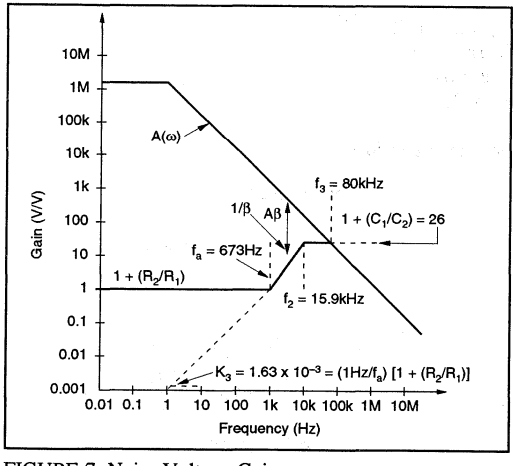


FIGURE 7. Noise Voltage Gain.

The noise voltage spectral density at the output is obtained by multiplying the amplifier's noise voltage spectral density (Figure 5a) times the circuits noise gain (Figure 7). Since both curves are plotted on log-log scales, the multiplication can be performed by the addition of the two curves. The result is shown in Figure 8.

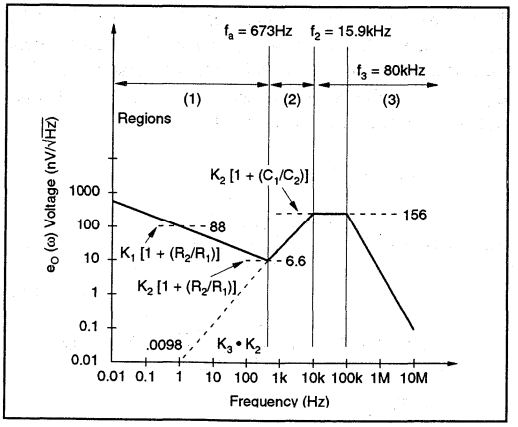


FIGURE 8. Output Voltage Noise Spectral Density.

The total rms noise at the amplifier's output due to the amplifier's internal voltage noise is derived from the $e_O(\omega)$ function in Figure 8 with the following expression:

$$E_O \text{ rms} = \sqrt{\int_{-\infty}^{+\infty} e_O^2(\omega)\, d\omega} \quad (8)$$

It is both convenient and informative to calculate the rms noise using a piecewise approach (region-by-region) for each of the three regions indicated in Figure 8.

Region 1; $f_1 = 0.01\text{Hz}$ to $f_C = 100\text{Hz}$

$$E_{n1} \text{ rms} = K_1\left[1 + \frac{R_2}{R_1}\right]\sqrt{\ell n\left(\frac{f_C}{f_1}\right)} \quad (9)$$

$$= 80\text{nV}/\sqrt{\text{Hz}}\left[1 + \frac{10^7}{10^8}\right]\sqrt{\ell n\left(\frac{100}{0.01}\right)} \quad (9a)$$

$$= 0.267\mu\text{V}$$

This region has the characteristic of 1/f or "pink" noise (slope of –10dB per decade on the log-log plot of $e_n\omega$). The selection of 0.01Hz is somewhat arbitrary but it can be shown that for this example there would be only negligible additional contribution by extending f_1 several decades lower. Note that $K_1\,(1 + R_2/R_1)$ is the value of e_o at f = 1Hz.

Region 2; $f_a = 673\text{Hz}$ to $f_2 = 15.9\text{kHz}$

$$E_{n2} \text{ rms} = K_2 \bullet K_3\sqrt{\frac{f_2^3}{3} - \frac{f_a^3}{3}} \quad (10)$$

$$= \left(6\text{nV}/\sqrt{\text{Hz}}\right)(1.63 \times 10^{-3})\sqrt{\frac{(15.9\text{kHz})^3}{3} - \frac{(673)^3}{3}} \quad (10a)$$

$$= 11.3\mu\text{V} \quad (9)$$

This is the region of increasing noise gain (slope of +20dB/decade on the log-log plot) caused by the lead network formed by the resistance $R_1 \parallel R_2$ and the capacitance (C_1 + C_2). Note that $K_3 \bullet K_2$ is the value of the e_o (ω) function for this segment projected back to 1Hz.

Region 3; f > 15.9kHz

$$E_{n3}\ \text{rms} = K_2\left(1+\frac{C_1}{C_2}\right)\sqrt{\left(\frac{\pi}{2}\right)f_3 - f_2} \qquad (11)$$

(11a)

$$= \left(6\text{nV}/\sqrt{\text{Hz}}\right)\left(1+\frac{25}{1}\right)\sqrt{\left(\frac{\pi}{2}\right)(80\text{k}) - 15.9\text{k}}$$

$$= 51.7\mu\text{V}$$

This is a region of white noise with a single order rolloff at f_3 = 80kHz caused by the intersection of the 1/β curve and the open-loop gain curve. The value of 80kHz is obtained from observing the intersection point of Figure 7. The $\pi/2$ applied to f_3 is to convert from a 3dB corner frequency to an effective noise bandwidth.

CURRENT NOISE

The output voltage component due to current noise is equal to:

$$E_{ni} = i_n \times Z_2(s) \qquad (12)$$

where $Z_2(s) = R_2 \parallel X_{C2}$ (12a)

This voltage may be obtained by combining the information from Figures 5 (b) and 6 together with the open loop gain curve of Figure 7. The result is shown in Figure 9.

Using the same techniques that were used for the voltage noise:

Region 1; 0.1Hz to 10kHz

$$E_{ni1} = 4\times10^{-9}\sqrt{10\text{k} - 0.1} \qquad (13)$$

$$= 0.4\mu\text{V}$$

Region 2; 10kHz to 15.9kHz

$$E_{ni2} = 4\times10^{-13}\sqrt{\frac{(15.9\text{kHz})^3}{3} - \frac{(10\text{kHz})^3}{3}}$$

$$= 0.4\mu\text{V} \qquad (13a)$$

Region 3; f > 15.9kHz

$$E_{ni3} = 6.36\times10^{-9}\sqrt{\frac{\pi}{2}(80\text{kHz}) - 15.9\text{kHz}}$$

$$= 2.1\mu\text{V} \qquad (13b)$$

$$E_{ni\,\text{TOTAL}} = 10^{-6}\sqrt{(0.4)^2 + (0.4)^2 + (2.1)^2}$$

$$= 2.2\mu\text{Vrms} \qquad (13c)$$

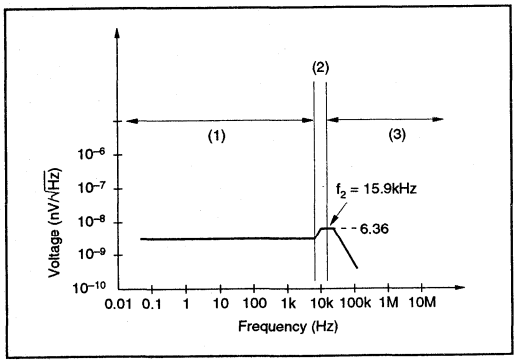


FIGURE 9. Output Voltage Due to Noise Current.

RESISTOR NOISE

For a complete noise analysis of the circuit in Figure 4, the noise of the feedback resistor, R_2, must also be included. The thermal noise of the resistor is given by:

$$E_R\ \text{rms} = \sqrt{4\text{kTRB}} \qquad (14)$$

K = Boltzmann's constant = 1.38 x 10^{-23} Joules/°Kelvin
T = Absolute temperature (°K)
R = Resistance (Ω)
B = Effective noise bandwidth (Hz) (ideal filter assumed)

At 25°C this becomes

$$E_R\ \text{rms} \cong 0.13\sqrt{\text{RB}}$$

E_R rms in μV
R in MΩ
B in Hz

For the circuit in Figure 4

$$R_2 = 10^7\Omega = 10\text{M}\Omega$$

$$B = \frac{\pi}{2}(f_2) = \frac{\pi}{2}15.9\text{kHz}$$

Then

$$E_R\ \text{rms} = \left(411\text{nV}/\sqrt{\text{Hz}}\right)\sqrt{B}$$

$$= \left(411\text{nV}/\sqrt{\text{Hz}}\right)\sqrt{\frac{\pi}{2}15.9\text{kHz}}$$

$$= 64.9\mu\text{Vrms}$$

TOTAL NOISE

The total noise may now be computed from

$$E_{n\,TOTAL} = \sqrt{E_{n1}^2 + E_{n2}^2 + E_{n3}^2 + E_{nR}^2 + E_{ni}^2} \quad (15)$$

(15a)

$$= 10^{-6}\sqrt{(0.293)^2 + (11.3)^2 + (51.7)^2 + (64.9)^2 + (2.2)^2}$$

$$= 83.8\mu Vrms$$

CONCLUSIONS

Examination of the results in equation (16b) together with the curves in Figure 8 leads to some interesting conclusions.

The largest component is the resistor noise E_{nR} (60% of the total noise). A lower resistor value decreases resistor noise as a function of $\sqrt{R}$, but it also lowers the desired signal gain as a direct function of R. Thus, lowering R reduces the signal-to-noise ratio at the output which shows that the feedback resistor should be as large as possible. The noise contribution due to R_2 can be decreased by raising the value of C_2 (lowering f_2) but this reduces signal bandwidth.

The second largest component of total noise comes from E_n^3 (38%). Decreasing C_1 will also lower the term $K_2(1 + C_1/C_2)$. In this case, f_2 will stay fixed and f_a will move to the right (i.e., the +20dB/decade slope segment will move to the right). This can have a significant reduction on noise without lowering the signal bandwidth. This points out the importance of maintaining low capacitance at the amplifier's input in low noise applications.

It should be noted that increasing C_2 will also lower the value of $K_2(1 + C_1/C_2)$, and the value of f_2 (see equation 5b). This reduces signal bandwidth and the final value of C_2 is normally a compromise between noise gain and necessary signal bandwidth.

It is interesting to note that the current noise of the amplifier accounted for only 0.1% of the total E_n. This is different than would be expected when comparing the current and voltage spectral densities with the size of the feedback resistor. For example, if we define a characteristic value of resistance as

$$R_{CHARACTERISTIC} = \frac{e_n(\omega)}{i_n(\omega)} \text{ at } f = 10kHz$$

$$= \frac{6nV/\sqrt{Hz}}{0.4fA\sqrt{Hz}}$$

$$= 15M\Omega$$

Thus, in simple transimpedance circuits with feedback resistors greater than the characteristic value, the amplifier's current noise would cause more output noise than the amplifier's voltage noise. Based on this and the 10MΩ feedback resistor in the example, the amplifier noise current would be expected to have a higher contribution than the noise voltage. The reason it does not in the example of Figure 4 is that the noise voltage has high gain at higher frequencies (Figure 7) and the noise current does not (Figure 6).

BURR-BROWN®
APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

PHOTODIODE MONITORING WITH OP AMPS

With their low-input currents, FET input op amps are universally used in monitoring photodetectors, the most common of which are photodiodes. There are a variety of amplifier connections for this purpose and the choice is based on linearity, offset, noise and bandwidth considerations. These same factors influence the selection of the amplifier with newer devices offering very low-input currents, low noise and high speed.

Photodetectors are the bridge between a basic physical indicator and electronics resulting in the largest single usage of FET op amps. As a measure of physical conditions, light is secondary to temperature and pressure until the measurement is made remotely with no direct contact to the monitored object. Then, the signals of a CAT scanner, star-tracking instrument or electron microscope depend on light for the final link to signal processing. Photodiodes have made that link economical and expanded usage to detector arrays that employ more than 1000 light sensors. Focus then turns to accurate conversion of the photodiode output to a linearly related electrical signal. As always, this is a contest between speed and resolution with noise as a basic limiting element. Central to the contest is the seemingly simple current-to-voltage converter which displays surprising multidimensional constraints and suggests alternative configurations for many optimizations.

CURRENT-TO-VOLTAGE

The energy transmitted by light to a photodiode can be measured as either a voltage or current output. For a voltage response, the diode must be monitored from a high impedance that does not draw significant signal current. That condition is provided by Figure 1a. Here, the photodiode is in series with the input of an op amp where ideally zero current flows. That op amp has feedback set by R_1 and R_2 to establish amplification of the voltage diode just as if it was an offset voltage of the amplifier. While appealing to more common op amp thinking, this voltage mode is nonlinear. The response has a logarithmic relationship to the light energy received since the sensitivity of the diode varies with its voltage.

Constant voltage for a fixed sensitivity suggests current output instead and that response is linearly related to the incident light energy. A monitor of that current must have zero input impedance to respond with no voltage across the diode. Zero impedance is the role of an op amp virtual ground as high-amplifier loop gain removes voltage swing from the input. That is the key to the basic current-to-voltage converter connection of Figure 1b. It provides an input resistance of R_1/A where A is the open-loop gain of the op amp. Even though R_1 is generally very large, the resulting input resistance remains negligible in comparison to the output resistance of photodiodes.

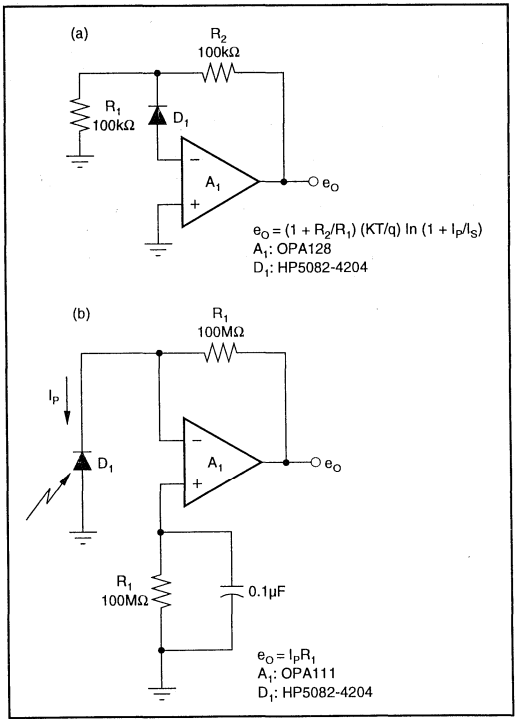


FIGURE 1a. Photodiode Output Can be Monitored as a Voltage; or, 1b, as a Current.

Diode current is not accepted by the input of the op amp as its presence stimulates the high amplifier gain to receive that current through the feedback resistor, R_1. To do so, the amplifier develops an output voltage equal to the diode current times the feedback resistance, R_1. For that current-to-voltage gain to be high, R_1 is made as large as other constraints will permit. At higher resistance levels, that resistor begins to develop significant thermal DC voltage

drift due to the temperature coefficient of the amplifier input current. To compensate this error, an equal resistance R_2 is commonly connected in series with the op amp noninverting input, as shown, and capacitively bypassed to remove most of its noise. The remaining DC error is determined by the mismatches between the amplifier input currents and between the two resistors. A drawback of this error correction is the voltage drop it creates across the diode and the resulting diode leakage current. That leakage can override the correction achieved with R_2, as photodiodes typically have large junction areas for high sensitivity. Leakage current is proportional to that area which can become much larger than the op amp input currents.

Only zero diode voltage can eliminate this new error source but that is in conflict with control of a second attribute of large diode area. Large parasitic capacitance is also present creating often severe amplification of noise as will be described. To reduce that capacitance, a large reverse-bias voltage is sometimes impressed on the diode greatly complicating DC stability and making current noise from the photodiode an additional error factor. Larger diode area may actually degrade overall accuracy and higher photo sensitivity should first be sought through optical means such as a package with an integral molded lens. Monitor-circuit configurations that maintain zero diode voltage are also candidates in this optimization and are described with Figures 6, 7 and 9.

The value of the feedback resistor in a current-to-voltage converter largely determines noise and bandwidth as well as gain. Noise contributed directly by the resistor has a spectral density of $\sqrt{4KTR}$[1] and appears directly at the output of a current-to-voltage converter without amplification. Increasing the size of the resistor not only raises output noise by a square root relationship but also increases output signal by a direct proportionality. Signal-to-noise ratio, then, tends to increase by the square root of the resistance.

Noise from the op amp also influences the output with a surprising effect introduced by high feedback resistance and the diode capacitance. The amplifier noise sources are modeled in Figure 2a as an input noise current, i_n, and the input noise voltage, e_n. The current noise flows through the feedback resistor experiencing the same gain as the signal current. It is the shot noise of the input bias current, I_B, and has a noise density of $\sqrt{2qI_B}$[1]. Choice of an op amp having input currents in the picoamp range makes this noise component negligible for practical levels of feedback resistance. Input noise voltage of the amplifier would at first seem to be transferred with low gain to the output. That is true at DC where its gain $1 + R_1/R_D$ is kept small by the large diode resistance, R_D. Capacitance, C_D, of the diode alters the feedback at higher frequencies adding very significant gain to e_n. As both the capacitance and the feedback resistance are commonly large, the effect can begin at fairly low frequencies. Figure 2b illustrates the effect with an op amp gain magnitude curve plotted with the reciprocal of the feedback factor or the "noise gain." That gain curve first experiences a response zero due to C_D and begins a rise that is terminated only because of a second parasitic capacitance. Stray capacitance, C_S, shunts the feedback resistor resulting in a response pole leveling the gain at $1+ C_D/C_S$. For large area diodes C_D can be hundreds of picofarads causing the noise gain to peak in the hundreds as well. That gain continues to higher frequencies until rolled off by the op amp bandwidth limit. As feedback resistance increases, the pole and zero of this gain peaking move together to lower frequencies encompassing a greater spectrum with high gain.

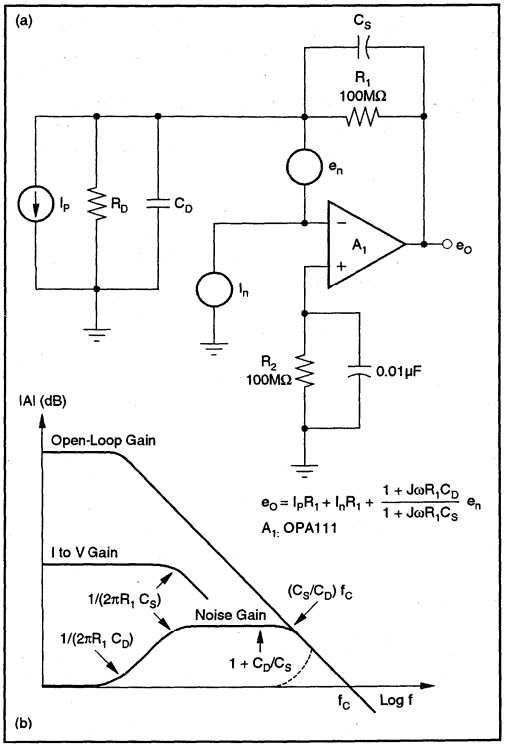


FIGURE 2a. Due to Diode Capacitance in the Feedback of the Basic Current-to-Voltage Converter, 2b, Op Amp Noise Receives Gain and Bandwidth Not Available to the Signal.

First signs of this gain peaking phenomena are familiar to anyone who has used high resistance op amp feedback in more general circuits. High output to input resistance with an op amp results in overshoot, response peaking, poor settling or even oscillation all due to the resistance interaction with amplifier input capacitance. Together the resistance and capacitance form another pole in the feedback loop resulting in the classic differentiator feedback response. Shown by the dashed line for more general op amp cases, the associated feedback factor reciprocal intercepts the amplifier open loop magnitude response with a 12dB/octave rate

of closure corresponding to feedback phase shift approaching or equal to 180°. The common cure for this condition is a capacitor across the feedback resistor, which for the very high resistances of current-to-voltage converters, automatically results from stray capacitance. Such capacitance degenerates the added feedback pole to control phase shift in the feedback loop.

In understanding current-to-voltage converter noise performance it is important to note that the signal current and the noise voltage encounter entirely different frequency responses. The current-to-voltage gain is flat with frequency until the feedback impedance is rolled off by stray capacitance as shown. Gain received by the amplifier noise voltage, on the same graph, extends well beyond that roll-off and is high in that extended region. The majority of the op amp's bandwidth often serves only to amplify that noise error and not the signal. This is typically the dominant source of noise for higher feedback resistances.

Relative effects of the major noise sources of a current-to-voltage converter can be seen with the curves of Figure 3. Those curves show output noise for the basic current-to-voltage converter of Figure 1b including the effects of the noise gain represented in Figure 2b. Plotted are total output noises for three cases as a function of feedback resistance and each is the rms sum of the components produced by the feedback resistor and an op amp. Represented are three FET op amps having different performance specialties that cover the spectrum of photodiode applications with low noise, low-input bias current and high speed. While all three types have low-noise designs and low-input currents, the OPA111 offers the lowest noise in the FET op amp class at $6nV/\sqrt{Hz}$, and the OPA128 has the lowest input current at 0.075pA. Without neglecting performance in these categories, the OPA404 design pushes bandwidth to 6.4MHz. Noise due to the op amp is found by integrating the amplifier noise density spectral response over the noise gain response[2]. Also shown, by a dashed line, is the noise due to the resistor alone for the OPA111 and OPA2111 case. This resistor noise curve is different for the other op amps as each amplifier has a different bandwidth rolling off noise due to the resistor.

Different factors control the noise curves for different ranges of feedback resistance. At low resistance levels, the noise curves are largely flat with the op amp voltage noise the dominant contributor. That domination makes initial resistance increases have little effect except for the case of the very low-voltage noise of the OPA111/ OPA2111. In this region noise gain peaking has not yet been encountered so the output noise remains small. Between 10kΩ and 1MΩ, resistor noise is dominant and the curves track that error source as the dashed line shows for the OPA111/OPA2111. Here, the curves demonstrate the square root relationship with the resistance and differ only because of amplifier bandwidths. At still higher resistance, noise gain peaking takes effect returning the op amp noise to dominance and boosting the curves higher. That effect is first demonstrated by the increased slope of the OPA404 curve as that amplifier's wide bandwidth first encompasses the peaking. The noise curves level off when essentially the full amplifier bandwidth is encompassed by the gain peaking. Moving to yet higher resistance, resistor noise would return the curves to rising slopes, but resistor bandwidth is by then rolled off by stray capacitance. In this upper region, any increase in resistance is accompanied by a matching reduction in noise bandwidth so that the total resistor noise becomes a constant. Variables of diode and stray capacitances alter the point of onset of gain peaking errors, but the characteristic shape of the output noise curves remains the same for any case. Each will display ranges dominated by op amp noise, resistor noise and gain peaking effects.

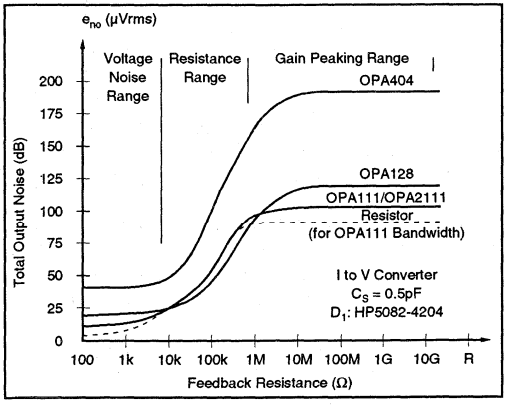


FIGURE 3. As the Feedback Resistance of a Current-to-Voltage Converter Increases, the Dominant Noise Source Changes from the Op Amp to the Resistor and Back to the Op Amp under Gain Peaking Conditions.

Comparing the curves shows that the OPA111/OPA2111 provide the lowest noise in two of the characteristic ranges. While the OPA128 shows a lower noise curve in the middle range, that is due to the amplifier's lower bandwidth and a bandwidth reduction technique to be described, removes that difference for the OPA111. Where the OPA128 excels is in very low DC error as its input currents are a mere 0.075pA which is 1/20th that of its low-noise contender. The third op amp, OPA404, produces higher total output noise overall, but that again is largely a bandwidth phenomenon. The 6.4MHz response of that amplifier accommodates noise over a much greater frequency range. While the noise curve for this amplifier is consistently higher than that of the OPA128, the OPA404 actually has lower noise density but it has six times the bandwidth. That 6.4MHz bandwidth is available to signals for feedback resistances up to 50kΩ and the amplifier still offers the best bandwidth for resistances up to 150kΩ. As the OPA404 is a quad op amp, its economy suggests consideration for use at even higher resistances along with bandwidth reduction that provides more competitive output noise.

Only a five dimensional graph could display the output noise, resistance, DC error, diode area and signal bandwidth considered in current-to-voltage converter design. Each specific application's requirements are evaluated separately with respect to these factors. To avoid suboptimizing a given design for one factor such as gain, the various effects of increasing feedback resistance are anticipated at each step. Choices such as large diode area are made considering the related capacitance and its effect on output noise and overall circuit sensitivity.

NOISE CONTROL

Gain peaking effects are the primary noise limitation with the commonly preferred high feedback resistances. To limit this effect, or to eliminate the gain rise entirely, additional capacitance is commonly added to bypass the feedback resistor. The capacitance level required can be very small for some values of R_1 and the relative significance of unpredictable stray capacitance make tuning desirable. Combined, these requirements are a challenge better resolved with a capacitor tee network as described in Figure 4a. It is capable of even subpicofarad tunable capacitance with little effect on stray capacitance in the tuning operation. The tee uses a capacitive divider formed with C_2 and C_3 to attenuate the signal applied to C_1 at the circuit input. With only a fraction of the output signal on C_1, it supplies far less shunting current to the input node as would a much smaller capacitor. Controlling the attenuation ratio is the tunable C_3, which is the largest of the capacitors, so its capacitance value is more readily available in tunable form. Since that capacitor is grounded, it has a shielding advantage to reduce stray capacitance influence while tuning.

Another option for practical feedback bypass exists with a resistor tee which is a commonly considered replacement for the high value feedback resistor. The latter is replaced in Figure 4b by elements of more reasonable value but introduces greater low frequency noise. Its operation is the dual of the capacitor tee above with R_2 and R_3 attenuating the signal to R_1 so that the latter appears as a much larger resistor to the input node. A similar opportunity for the DC error compensation resistor R_2 does not exist. DC error due to amplifier input current is no different with the tee so the large compensation resistor is still needed.

Stray capacitance across the feedback is somewhat reduced with the resistor tee by the added physical spacing of the feedback with three elements. Also, stray capacitance across each individual element has much less effect with their lower resistances. Sensitivity to other stray capacitance from the op amp output to its input has the same effect as before.

In the attenuation network of the feedback is the opportunity for intentional bypass with reasonable capacitor values. Bypassing the moderate resistance of R_2 removes the attenuation at higher frequencies leaving the net feedback resistance at the level of R_1. This operation differs from true feedback bypass in that impedance levels off, rather than continuing to fall with frequency, but the dramatic drop in

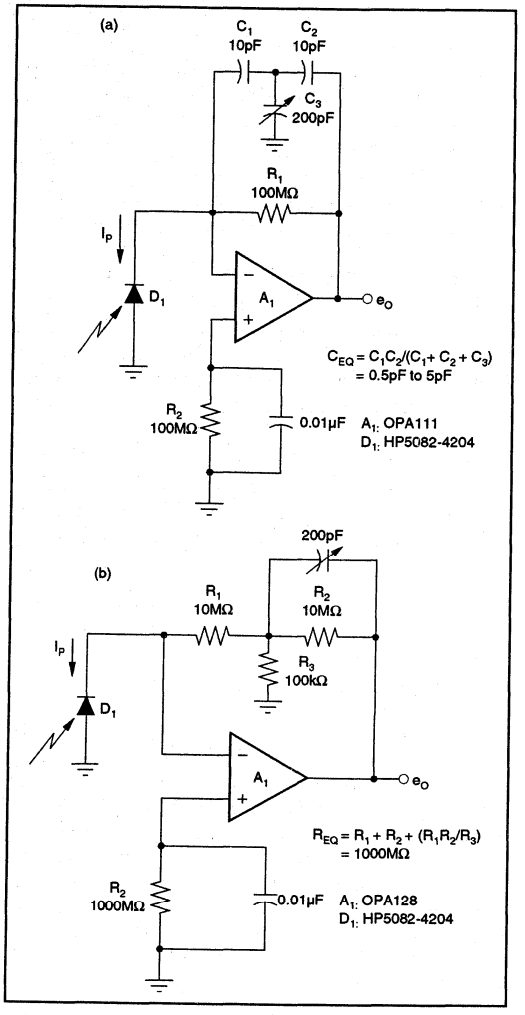


FIGURE 4a. Removal of Amplifier Gain Peaking Through Small Capacitive Bypass of Large Feedback Resistance is More Feasible with a Capacitor Tee; or, 4b, Bypass of One Element of a Feedback Resistor Tee.

equivalent resistance serves the circuit requirement. Another benefit offered by the resistor tee is more accurate DC error compensation.

Reduced high frequency noise with the tee element bypass is accompanied by an opposing increase at lower frequencies. Below the frequency of the bypass, noise gain is increased by the feedback attenuation of the tee network. That amplifies the noise and offset voltages of the op amp as well as the noise of resistor R_1 by a factor of $1 + R_2/R_3$. Countering the latter is the resistor's smaller value so that

this effect is increased only by the square root of the new noise gain. Most important, however, is the bypass capacitor removal of high frequency gain as it eliminates the greatest portion of previous noise bandwidth. In the absence of other means to remove the high frequencies, the bypassed resistor tee provides lower total output noise for the higher ranges of feedback resistance.

Adding feedback capacitance is an effective means of reducing noise gain but it also decreases signal bandwidth by the same factor. That bandwidth is already low with high feedback resistance and the end result can be a response of a kilohertz or less. A more desirable solution to the noise problem is to limit amplifier bandwidth to a point just above the unavoidable signal bandwidth limit. Then, the high frequency gain which only amplifies noise is removed. Op amps with provision for external phase compensation offer this option, but those available lack the low-input currents and low-voltage noise needed for photodiode monitoring.

To achieve this bandwidth limiting with better suited op amps, a composite amplifier uses two op amps with the added one for phase compensation control as in Figure 5a. Note the reversal of the inverting and noninverting inputs of A_1 needed to retain a single phase inversion with two amplifiers in series. With the composite structure, internal feedback controls the frequency response of the gain added by A_2. At DC, that feedback is blocked by C_1 and overall open-loop gain is the product of those of the two amplifiers or 225dB for those shown. That gain is rolled off by the open-loop pole of A_1 and by the integrator response established for A_2 by C_1 and R_3. As this is a two pole roll-off, it must be reduced before intercepting the noise gain curve to establish frequency stability. A response zero does this due to the inclusion of R_4. Above the frequency of that zero, R_4 also replaces the integrator response with that of an inverting amplifier having a gain of $-R_4/R_3$. Making that gain less than unity drops the net gain magnitude curve below that of a single amplifier at high frequencies. Graphically, the noise gain response of Figure 5b is moved back in frequency much as if the op amp bandwidth had been reduced.

Eliminated is the shaded area of noise gain, which visually may not appear dramatic, but that is because of the logarithmic-frequency scale. Actually, the associated noise reduction is large because most of the amplifier's bandwidth is represented in this upper end of the logarithmic-response curve. Moving the unity gain crossover of the noise gain from 2MHz to 200kHz, as shown, drops the output noise due to A_1 by about a factor of three. To achieve the same result with feedback bypass, the signal bandwidth would have been reduced a factor of ten. That bandwidth is unaffected with the Figure 5a approach. No noise, or offset, is added by A_2 as this amplifier is preceded by the high gain of A_1. With the exceptionally low noise of the OPA111 input amplifier, this improvement reduces noise to the fundamental limitation imposed by that of the feedback resistor. This condition is retained for all practical levels of high feedback resistance. For the second amplifier, the wideband OPA404 is shown to continue its attenuating amplifier action well beyond the unity gain crossover of A_1. This avoids a second gain peak that could cause oscillation. Signal bandwidth of the current-to-voltage conversion is essentially unaffected as R_1 has not been influenced .

Where the Figure 5 technique is most useful is with lower level signals that have greater sensitivity to noise. In higher level applications that circuit can encounter a voltage swing limitation but another use of the second amplifier offers similar noise improvement. The swing limitation results from the maximum output voltage limit of A_1 and its attenuation by A_2. If the output of A_1 has a peak swing of 12V and A_2 has the gain of –1/10 illustrated, the final output is limited to a 1.2V peak swing. For lower-level signals this will be acceptable as the maximum practical level of feedback resistance already limits output swing.

Higher-level signals are not as sensitive to noise and better tolerate a more straight forward approach to filtering. An active filter following the conventional current-to-voltage converter also removes the high frequency noise. Setting filter poles at the frequency of the signal bandwidth results

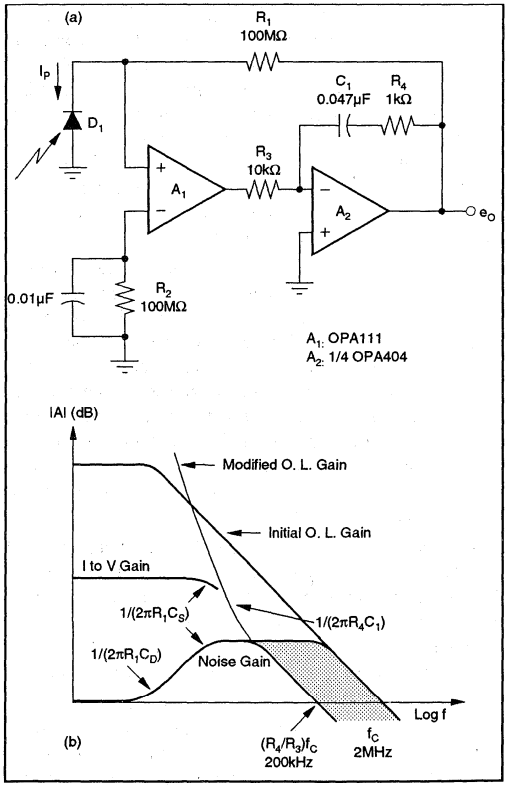


FIGURE 5a. Noise Reduction Results with a Composite Amplifier that, 5b, Restricts Noise Bandwidth Without Reducing that of the Signal.

in a system bandwidth that does not extend beyond that of useful information. Such a filter is not enclosed in a feedback loop with the converter so the input noise and offset voltage of the second amplifier are added to the signal.

BANDWIDTH

Signal bandwidth requirements are an integral part of the current-to-voltage converter noise considerations for two reasons. Total output noise increases in proportion to the square root of system bandwidth simply because a broader noise spectrum is encompassed. Added is conflict between optimum signal-to-noise ratio and signal bandwidth. That optimum occurs for very high gain but high gain current-to-voltage converters are bandwidth limited far below the roll-off of the op amp. To the signal current, the amplifier feedback factor is unity which would normally make the full amplifier unity gain bandwidth available. Yet the very high-feedback resistances that produce the desired gain are shunted by stray capacitances at much lower frequency. Just 0.5pF stray capacitance around a 100MΩ feedback resistor pulls signal bandwidth from megahertz level unity gain crossovers down to 3.2kHz. To minimize the stray shunting, low capacitance resistors and assembly precautions are used. Mounting the feedback resistor on standoffs reduces capacitive coupling with printed circuit boards and such standoffs are normally Teflon™ insulated to reduce leakage currents. That mounting must be rigid to avoid introduction of noise through the microphonic effects of mechanical stress from vibrations.

There is an ultimate limit to the effects of such measures as capacitive coupling through the air around the resistor body always remains. Bandwidth beyond that imposed by such residual limits requires lower feedback resistance and accompanying lower converter gain. To restore gain, several options are available with a first shown in Figure 6a. A second amplifier with voltage gain is simply added following the current-to-voltage converter to retain the net input to output transimpedance for $R_T = A_V R_1$. Then, the high-value resistance is reduced by a factor equal to the voltage gain for a bandwidth increase by as much as the same factor.

While an obvious alternative, its overall effect on bandwidth and noise are not so immediate. Bounding the upper end of the bandwidth increase is the response limitation of the second amplifier. The bandwidth of the two op amp circuit for a net transimpedance of 100MΩ is plotted in Figure 6b as a function of the voltage gain involved in the overall conversion. Bandwidth initially increases linearly with the voltage gain as the reduction in R_1 diminishes the roll-off effect of stray capacitance. However, the added demands of the voltage gain on A_2 eventually make that amplifier's bandwidth the controlling factor. For a given set of conditions there is an optimum gain. A_V produces the peak bandwidths shown for the three example amplifiers. That peak occurs when the amplifier closed loop bandwidth equals the stray limited bandwidth of R_1. Variables affecting this peak are the net transimpedance, R_T, and the second op amp unity gain bandwidth, f_C. Interrelating the controlling factors at the optimum bandwidth point is the expression defining the choice of R_1:

$$R_1 = \sqrt{R_T / 2\pi C_S f_C}$$

Bandwidth is extended to 100kHz from the original 3kHz using the wideband OPA404 for the second amplifier. That wideband op amp offers the best frequency response in Figure 6 and, although its total output noise result is greater, that is again largely due to the greater available bandwidth. If even greater bandwidth is required, either a faster op amp, with typically poorer noise performance, or lower transimpedance are the choices. Less bandwidth demands are encountered by A_1 with its unity feedback factor so an FET amplifier focused on low noise is used there like the OPA111 shown.

The price paid for improved bandwidth through voltage gain is increased output noise from that gain as well as from the presence of the added amplifier. While the lower value of R_1 does reduce its noise density, that effect is counteracted by the increase in bandwidth for a net zero change is resistor noise. That noise is now amplified by the voltage gain of the

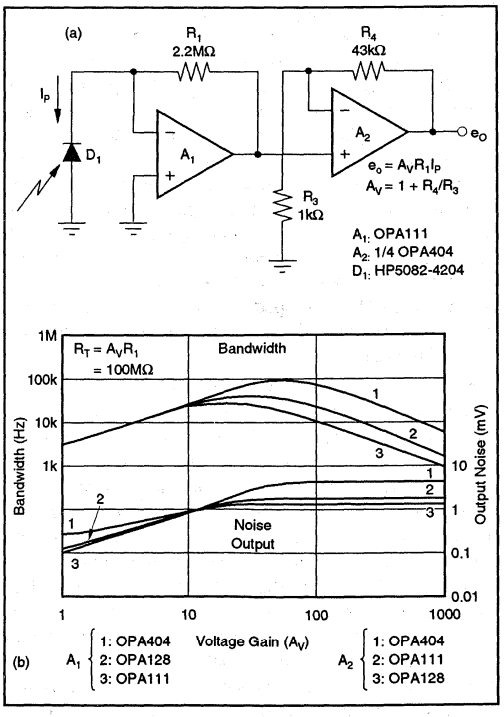


FIGURE 6. For Greater Bandwidth and the Same Net Transimpedance, (a) Voltage Gain is Added Providing (b) Bandwidth That Increases Faster Than Noise.

second amplifier causing an associated increase in output noise proportional to the voltage gain. Added to that is the noise from the op amps with the net result also shown in Figure 6b. Those noise curves are continuations of the ones presented in Figure 3 with the transition beginning at the 100MΩ level for the present example. In the lower gain ranges from one to ten, the noise is first determined largely by the op amps and their gain peaking but those effects give way to resistor noise dominance before the end of this range. Also in that range, the associated signal bandwidth plotted in Figure 6b is controlled by stray capacitance and shows a linear increase with increasing gain due to the corresponding decrease in resistance. Above the gain of ten and before 100, bandwidth begins to drop due to the encounter of A_2 limits. Simultaneous with this drop is a flattening of the output noise curve. Roll-off of the amplifier bandwidth and the simultaneous resistance drop nullify the effect of increasing voltage gain leaving output noise a constant. In the voltage gain range from 100 to 1000, these trends continue and degrade optimum performance since bandwidth is lost while noise remains constant.

While it is accepted that noise degrades with the voltage gain replacement of resistance, the overall circuit figure of merit gains. Including bandwidth in that measure shows that its improvement more than offsets the drop in signal-to-noise ratio. Mentioned before was the fact that the simple current-to-voltage converter suffers from greater bandwidth for the amplifier voltage noise than for the signal current. That discrepancy is removed with Figure 6 as the voltage gain increases and A_2 begins to filter out the higher frequencies. Evidence of this is in the noise curves that increase more gradually than the bandwidth curves—Figure 6b—up to the optimum bandwidth point. At this optimum point, no bandwidth is afforded to noise that is not also available to signal. In effect, A_2 now also serves as the output active filter discussed earlier. While each of these curves is drawn for a specific 100MΩ transimpedance and the amplifiers and photodiode specified, similar optimums are considered for any design case.

For some of the more common photodiode applications, a significant drawback of the above circuit is the need for two op amps per photodetector. Often hundreds of detectors are employed in a large arrays. As a compromise, one op amp can be made to provide the same transimpedance, still without the very large resistors, if some bandwidth and noise degradations can be accepted. A single op amp can both perform the current-to-voltage conversion and provide the subsequent voltage gain. With traditional techniques the task would be performed as in Figure 7a using R_2 for the conversion and R_3 and R_4 to set voltage gain. Current from D_1 flows in R_2 resulting in a signal voltage at the input of a noninverting amplifier. However, that signal voltage is also across the photodiode and this condition produces a nonlinear response as described before.

Instead, the diode is connected directly between the op amp inputs where zero diode voltage is maintained. Shown in Figure 7b, the resistors perform the same functions as in the last circuit but a linear response results. Current from the photodiode still flows in R_2 developing the same signal voltage. That current also flows into the feedback network but has little effect with the low resistances there. For the resistor values shown, an equivalent transimpedance of 100MΩ results—just as with the two op amp example, but bandwidth improvement is less. At 20kHz, it is increased a factor of seven rather than a factor equal to the voltage gain as in Figure 6a. A new bandwidth limitation accounts for the difference and occurs due to the new placement of the high-value resistance. That resistor is now shunted by the common-mode input capacitance of the op amp instead of just the smaller stray capacitance. To maximize bandwidth, this new shunting effect is made to coincide with the amplifier roll-off through choice of R_2 and the voltage gain. A second benefit from this choice is that resistor noise beyond the signal bandwidth encounters a two pole roll-off.

Final output noise from the resistor has the expected increase over the basic circuit by the square root of the voltage gain. Added to that would have been a small component due to the op amp as the normal source of gain peaking is

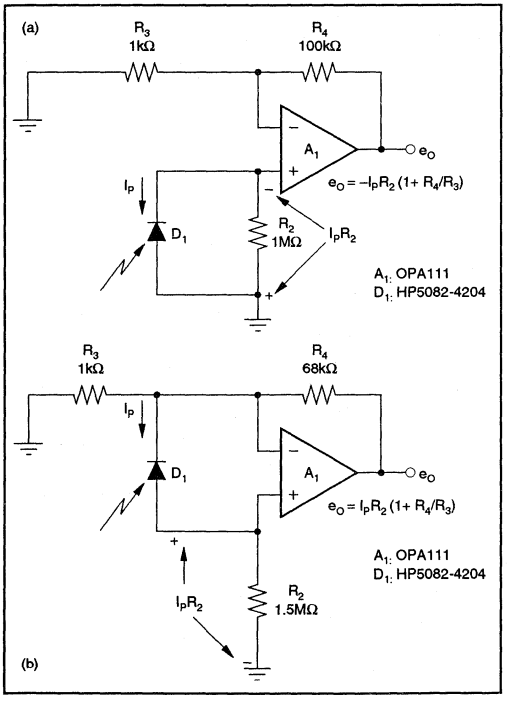


FIGURE 7. Combining Current-to-Voltage Conversion and Voltage Gain Using One Op Amp, (a) Impresses Unwanted Voltage on the Diode that (b) is Removed by Connecting the Diode Between the Op Amp Inputs.

removed. However, a new source is included in the circuit of Figure 7b, again due to the diode capacitance, as modeled in Figure 8a. Amplifier voltage noise, e_n, is impressed directly across that capacitance developing a noise current that is supplied to R_2. That creates a noise voltage at the input of the noninverting amplifier which is a multiple of e_n. The capacitive feedback network of C_D and C_{ICM} produces a noise gain that peaks at $1 + C_D/C_{ICM}$ and which exists in addition to the normal voltage gain of the noninverting amplifier.

Effects on frequency response are plotted in Figure 8b and they again produce a high-frequency peak in the noise gain. Its incidence is at a much higher frequency than with the basic current-to-voltage converter because of the lower resistance involved and it is truncated earlier by the op amp roll-off. For the low capacitance diode used in both example circuits, it now encompasses little area in the response plot corresponding to less noise effect. Larger diodes do not escape the effect, however, as represented by the dashed line for a capacitance around 200pF. Even still, the spectrum covered by the peaking is not the high end of the op amp bandwidth as it was for the basic circuit. Hence, op amp noise does not become the overriding source.

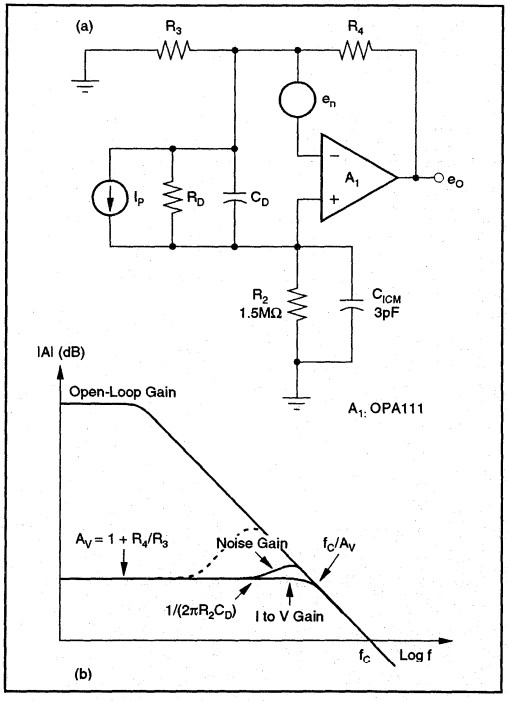


FIGURE 8. Photodiode Capacitance (a) Adds a Positive Feedback Path to Figure 7b for (b) a New but Lesser Source of Gain Peaking.

INTERFERENCE

Once diminishing returns impose a limit on reduction of the noise due to the circuit itself, consideration must be given to external noise sources. With its very high resistance, a current-to-voltage converter is extremely sensitive to noise coupling from electrostatic, magnetic and radio frequency sources. Those sources require attention to shielding, grounding, and component physical location[3], or they could otherwise become the dominant noise contributors. In each case, physical separation of the noise source from the sensitive circuitry is the most important step, but this becomes a compromise warranting other measures as well.

Electrostatic coupling, such as from the power line, supplies noise signals through the mutual capacitances that exist between any two objects. Voltage differences between the objects are impressed on those capacitances and any voltage variation couples a noise current from one to the other. To avoid that error signal, electrostatic shielding is used to intercept the coupled current and shunt it to ground. In this case, ground must be earth ground as that is the common reference for the separate objects. Such shields, however, create parasitic capacitances between the components shielded and the shields must also be returned to the signal common to avoid that coupling. Then shield carried capacitive currents from the output of a current-to-voltage converter are also shunted to ground and represent no bandwidth restriction to the feedback resistor. Even still, the shield produces a capacitance from the converter input to ground, possibly adding to gain peaking and its effect on total output noise.

As electrostatic coupling is most often of power line frequency and common to all points, it is a natural candidate for removal through the common-mode rejection of an op amp. At the line frequency, op amp CMR is very high but it is not utilized by the conventional current-to-voltage converter. This is a result of single-ended rather than differential input configurations, but that can be altered for improved noise rejection and DC error benefits as well. Op amp CMR is not a total replacement for shielding as electrostatic coupling will not perfectly common-mode to amplifier inputs. As a second defense, that rejection capability is most useful in removing the residual coupling that passes through shield imperfections.

The differential input capability of an op amp fits exactly with the signal from a photodiode. Since the diode signal is a current, it is available at both terminals of that sensor and can drive both amplifier inputs as in Figure 9a. Here, the diode current is no longer returned directly to common, but drives the amplifier noninverting input in that path. That creates a second signal voltage to double the circuit gain when $R_2 = R_1$ for, compensation. For a given gain level, the resistor value need be only one-half the normal for a similar reduction in error sensitivity to amplifier input currents. This also removes DC voltage from the diode as it is now directly across the inputs of an op amp. With the voltage between those inputs being essentially zero, photodiode leakage current is avoided.

Aside from these benefits is the added improvement in the common-mode rejection of coupled noise. Electrostatic coupling to this current-to-voltage converter is modeled in Figure 9b along with the converter's parasitic capacitances. Zero signal is assumed there to illustrate only the electrostatic coupling effects. The electrostatic noise source, e_e, couples error currents, i_e, through mutual capacitances, C_M, to the circuit's two inputs. It might seem that the coupling effects would be different to the two points because feedback makes the R_1 input node a virtual zero impedance and the other node is high impedance. Yet, the noise coupling is via currents through capacitances that only depend on voltage signals on the capacitances. Both input nodes have the same voltage due to amplifier feedback, and thus receive the same level of noise current i_e. Those equal currents develop canceling e_{ne} noise voltage effects on the two circuit resistors for a zero final output signal.

Accuracy of the error cancellation is determined by three matching conditions involving the mutual capacitances, the resistors and the parasitic capacitances shunting them. Matched mutual capacitances are best assured by locating the resistors equidistant from any significant noise source not effectively blocked by a shield. Equal resistance values assure accurate cancellation of error signals until frequencies are reached where capacitive shunting imbalances net impedances. Shunting R_1 will be only about 0.5pF of stray capacitance but across R_2 is the much larger common-mode input capacitance of the op amp. For the 3pF of the OPA111 and the 50MΩ resistance shown, a pole occurs at about 1kHz, leaving the impedances of interest unbalanced. This shunting by C_{ICM} also imposes a signal bandwidth limitation at a lower frequency than normally encountered. The bandwidth of R_2 is rolled off earlier than that of R_1 creating a response with two plateaus separated by a factor of two in gain.

For the most common electrostatic coupling at power line frequency, the above capacitive shunting has little effect. To better reject higher frequencies, capacitance can be added around R_1 to restore impedance matching, or signal swing on the common-mode input capacitance can be avoided. The latter option offers a more accurate solution and avoids the bandwidth limitation of C_{ICM} as well by using a second differential connection. Shown in Figure 10, the photodiode is connected between the inputs of two current-to-voltage converters whose outputs drive an INA105 difference amplifier. Again the diode current flows in two equal resistances that will receive equal electrostatic noise coupling. The diode current creates a differential output on the resistances, but the noise coupling generates a common-mode signal. Supplied to the INA105, those signals are separated with the diode signal passed to the output and the noise rejected.

Retained with the new differential input circuit are the 2:1 lower individual resistance and a zero diode voltage. The latter is assured by the grounded noninverting inputs of both current-to-voltage converters which establishes zero voltage on both diode terminals. These connections also avoid signal swing on common-mode input capacitances for improved bandwidth in electrostatic suppression and signal gain. Note that those noninverting inputs are not connected through high resistances for input current error correction. That is not necessary, as the input currents of A_1 and A_2 produce matching voltages at their amplifier outputs. Those voltages are a common-mode signal to the input of the INA105, so they too are rejected.

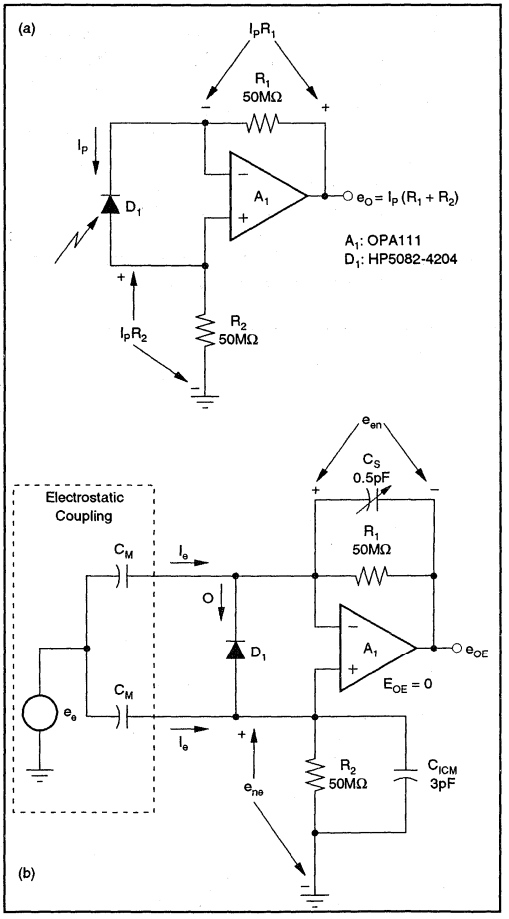


FIGURE 9. Exploiting the CMR Capabilities of the Op Amp, (a) the Differential Inputs are Driven Giving (b) Rejection of Electrostatic Coupling.

Another function available with the differential structure of Figure 10, is difference monitoring of two photodiodes. Instead of D_1, the two diodes shown in dashed lines are connected separately to the two input current-to-voltage converters. Their currents produce independent voltages at

the outputs of A_1 and A_2 where they are processed by the difference amplifier to remove any common-mode portion. Left is an output proportional to the difference between the two input photocurrents as a measure of relative light intensity. A relative intensity measure is the type of signal used in position sensing or optical tracking control to direct feedback correction.

Magnetic coupling of noise can be more difficult to eliminate than the electrostatic, but its effects are also reduced by the differential input connections. Coupling is through mutual inductances in this ease, so minimum sensitive loop area is key to its control, along with shielding and maximum separation of source and receiver. Its effects are not removed by the electrostatic shield, so the first step is control of the source itself.(3) Power transformers that cannot be placed at a distance are internally shielded to largely terminate their magnetic fields at the transformer boundaries. Remaining magnetic coupling is addressed through physical and circuit configurations. High value resistors used in photodiode monitoring are sensitive to this coupling and connections must be kept short between those resistors and high impedance op amp inputs. Coupling effects that remain are made common-mode to be rejected by the op amp through loop size and distance matching. In Figure 9 and Figure 10, the high resistance is divided into two equal elements that are then physically mounted with the same orientation to and spacing from magnetic coupling sources. Noise coupled to the two resistors then causes equal signals that have canceling effects at the circuit output.

With the third class of noise coupling, radio frequency interference, less can be removed by the amplifiers so shielding and filtering are the best defenses. Sources of RFI may be close to the photodiode monitor because of digital circuitry that is most likely co-resident in the system. Due to the high frequencies involved, op amps have little gain or common-mode rejection remaining for rejection of such signals. Because of this same amplifier limitation, and the basic voltage-to-current converter bandwidth restriction, desired signals will not exist in the radio frequency range. Filtering can then be used to largely remove the unwanted signal if applied in front of the op amp. Later filtering is less effective as the op amp can act like an RF detector separating a lower frequency envelope from a carrier.(4) Further reduction of that noise is achieved with an RF shield and a ground plane layer in printed circuit boards.

REFERENCES

(1) Tobey, G., Graeme, J., Huelsman, L., *Operational Amplifiers—Design and Applications*, McGraw-Hill, 1971.

(2) OPA101 product data sheet, PDS-434A, Burr-Brown Corp., 1980.

(3) Morrison, R., *Grounding and Shielding Techniques in Instrumentation*, second edition, John Wiley & Sons, 1977.

(4) Sutu Y., and Whalen, J., *Statistics for Demodulation RFI in Operational Amplifiers*, IEEE International Symposium on Electromagnetic Compatibility, August 23, 1983.

Teflon™ E.I. du Pont de Nemours & Co.

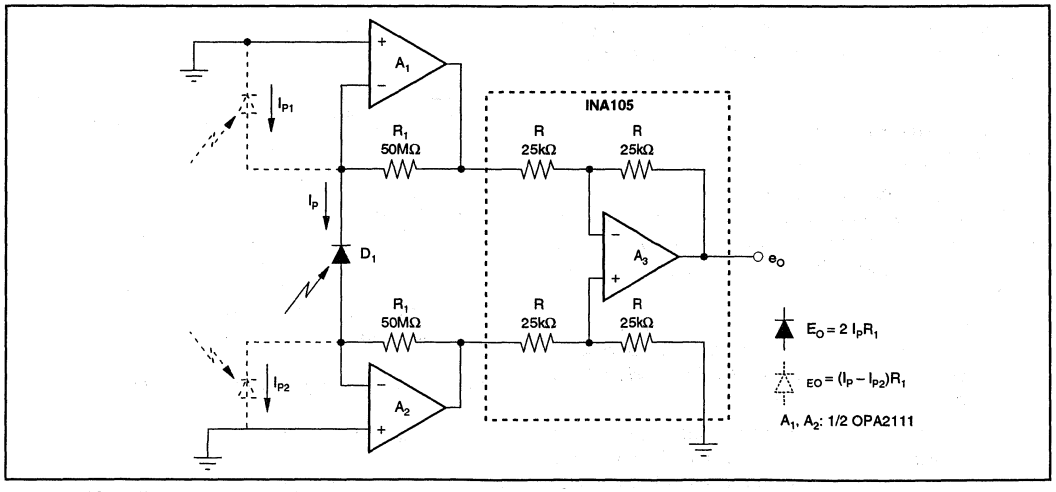


FIGURE 10. Differential Inputs with Wider Band CMR and Gain Result with Virtual Grounds Across Amplifier Common-Mode Input Capacitances.

BURR-BROWN®
APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

DESIGNING PHOTODIODE AMPLIFIER CIRCUITS WITH OPA128

The OPA128 ultra-low bias current operational amplifier achieves its 75fA maximum bias current without compromise. Using standard design techniques, serious performance trade-offs were required which sacrificed overall amplifier performance in order to reach femtoamp (fA = 10^{-15} A) bias currents.

UNIQUE DESIGN MINIMIZES PERFORMANCE TRADE-OFFS

Small-geometry FETs have low bias current, of course, but FET size reduction reduces transconductance and increases noise dramatically, placing a serious restriction on performance when low bias current is achieved simply by making input FETs extremely small. Unfortunately, larger geometries suffer from high gate-to-substrate isolation diode leakage (which is the major contribution to BIFET® amplifier input bias current).

Replacing the reverse-biased gate-to-substrate isolation diode structure of BIFETs with dielectric isolation removes this large leakage current component which, together with a noise-free cascode circuit, special FET geometry, and advanced wafer processing, allows far higher ***Difet*** ® performance compared to BIFETs.

HOW TO IMPROVE PHOTODIODE AMPLIFIER PERFORMANCE

An important electro-optical application of FET op amps is for photodiode amplifiers. The unequaled performance of the OPA128 is well-suited for very high sensitivity detector designs. A few design tips for photodiode amplifiers may be helpful:

- *Photodiode capacitance should be as low as possible.* See Figure 1: C_J affects not only bandwidth but noise as well. This is because C_J and the op amp's feedback resistor form a noise-gain zero (feedback pole).
- *Photodiode active area should be as small as possible so that C_J is small and R_J is high.* This will allow a higher signal-to-noise ratio. If a large area is needed, consider using optical "gain" (lens, mirror, etc.) rather than a large area diode. Optical "gain" is essentially noise-free.
- *Use as large a feedback resistor as possible (consistent with bandwidth requirements) to minimize noise.* This seems paradoxical, but remember, resistor thermal noise increases as:

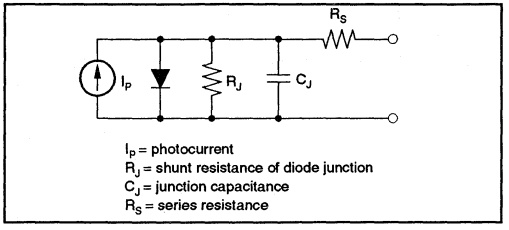


FIGURE 1. Photodiode Equivalent Circuit.

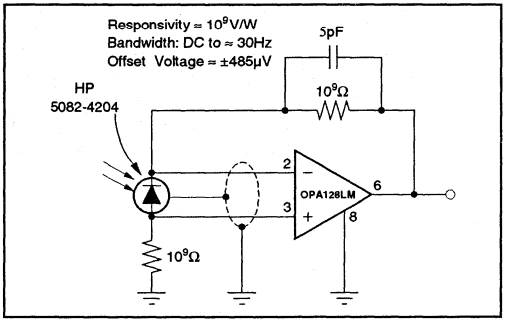


FIGURE 2. High-Sensitivity Photodiode Amplifier.

$e_{OUT} = \sqrt{4k\ TBR}$

k: Boltzman's constant = 1.38 x 10^{-23} J/K
T: temperature (°K)
B: noise bandwidth (Hz)
R: feedback resistor (Ω)
e_{OUT}: noise voltage (Vrms)

while transimpedance gain (signal) increases as:

$$e_{OUT} = i\ (signal)\ R$$

Signal-to-noise improves by $\sqrt{R}$.

- *A low bias current op amp is needed to achieve highest sensitivity.* Bias current causes voltage offset errors with large-feedback resistors. Wide bandwidth circuits with smaller feedback resistors are less subject to bias current errors, but even in these circuits, bias current must be

considered if wide temperature range operation is expected. The OPA128LM specs only ±2pA max at +70°C. Bias current also causes shot noise.

$$i_S = \sqrt{2qi}$$

q: 1.602×10^{-19} coulombs
i: bias (or signal) current (A)
i_S: noise current (A rms)

In most circuits, the dominant noise source will be the thermal (Johnson) noise of the feedback resistor.

• *Diode shunt resistance (R_J) should be as high as possible.* If $R_J \gg R_F$, then the circuit DC gain (noise gain) is 1V/V. Low resistance diodes will cause noise, voltage offset, and drift to be amplified by $1+ R_F/R_J$.

Since diode shunt resistance decreases at a higher temperature, it can cause unexpected errors. In Figure 3 a diffused-junction GaAsP photodiode is used to maintain R_J = 3000MΩ at +60°C. Due to its higher bandgap, GaAsP has a flatter R_J versus temperature slope than silicon.

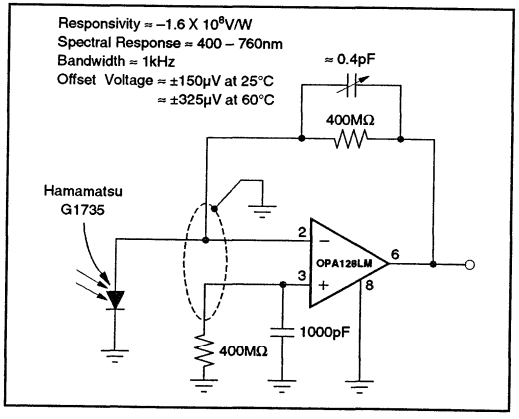


FIGURE 3. Wide-Temperature Range Photodiode Amplifier.

• *For highest sensitivity use the photodiode in a "photovoltaic mode".* With zero-bias operation, dark current offset errors are not generated by this (photodiode leakage) current. Zero bias is a slower but higher sensitivity mode of operation. Most photodiodes work quite effectively with zero bias, even those originally designed for reverse-biased operation.

• *Fastest response and greatest bandwidth are obtained in the "photoconductive mode".* Reverse bias reduces C_J substantially and also reduces or eliminates the slow rise time diffusion "tail" which is troublesome at longer wavelengths. Disadvantages of biased operation are: dark current, 1/F noise component is introduced, and the occasional need for an extra bias supply.

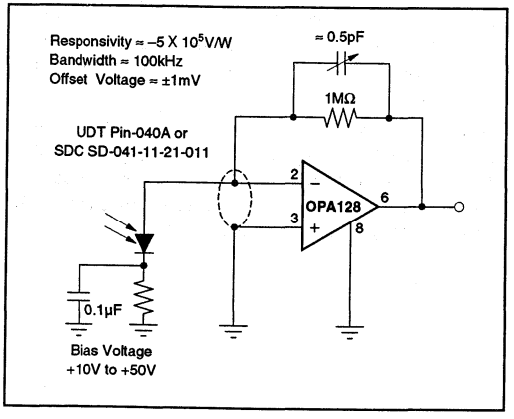


FIGURE 4. Wider-Bandwidth Photodiode Amplifier.

• *A very high resistance feedback resistor is MUCH better than a low resistance in a T network.* See Figure 5. Although transimpedance gain (e_{OUT}/i_{SIGNAL}) is equivalent, the T network will sacrifice performance. The low feedback resistance will generate higher current noise (i_N) and the voltage divider formed by R_1/R_2 multiply input offset voltage, drift, and amplifier voltage noise by the ratio of $1+ R_1/R_2$. In most electrometer amplifiers, these input specifications are not very good to start with. Multiplying an already high offset and drift (sometimes as high as 3mV and 50µV/°C) by use of a T network becomes impractical. By using a far better amplifier, such as the OPA128, moderate T network ratios can be accommodated and the resulting multiplied errors will be far smaller. Although a single very-high resistance will give better performance, the T network can overcome such problems as gain adjustment and difficulty in finding a large value resistor.

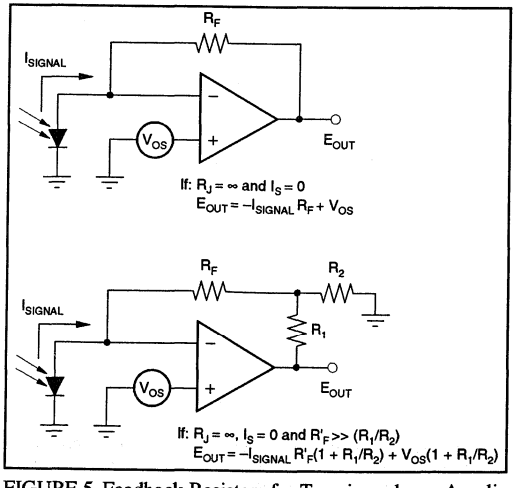


FIGURE 5. Feedback Resistors for Transimpedance Amplifiers.

- *Shield the photodetector circuit in a metal housing.* It is a very high impedance, high sensitivity circuit and it requires good shielding and effective power supply bypassing. This is **not** optional.
- *A small capacitor across R_F is frequently required to suppress oscillation or gain peaking.* Although it can affect bandwidth, a small amount of capacitance will usually be required to ensure loop stability. This capacitor can be made larger for bandwidth limitation if desired.

KEY OPA128 SPECIFICATIONS

Bias current	75fA max
Offset voltage	500μV max
Drift	5μV/°C max
Noise	15nV/√Hz at 10kHz

BIFFET® National Semiconductor Corp.; ***Difet***® Burr-Brown Corp.

BURR-BROWN®
APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

TAME PHOTODIODES WITH OP AMP BOOTSTRAP

by Jerald Graeme, (602) 746-7412

Applying a basic op amp current amplifier to photodiodes presents three severe problems: high nonlinearity, oscillations, and a latch condition. All three result from the presence of load-signal voltage feedback to the photodiode. A simple bootstrapping arrangement can remove them all.

In the basic circuit, Figure 1, two resistors, R_1 and R_2, control the positive and negative feedback, respectively. Consequently, they also control the current amplifier's gain. All the signal current, i_P, from the photodiode flows through R_1 (negligible current flows into the op amp's input), thereby defining the input-to-output voltage drop of the op amp. Because of the op amp's very high open-loop gain and the feedback arrangement, the circuit replicates that voltage across R_2 to keep the differential voltage between the op amp inputs close to zero. As a result, feedback current i_O flows into the load Z_L through R_2. Thus, the current gain i_O/i_P, or A_i, equals R_1/R_2.

Because the photodiode's responsivity changes as its voltage changes with light input, voltage variation across Z_L, which is also across the photodiode, causes nonlinearity. Even worse, the photodiode's capacitance, C_D, rolls off the negative feedback from R_1 at high frequencies. Consequently, the positive feedback from R_2 can dominate, and oscillations, can result. In fact, C_D inadvertently converts the circuit to a conventional op amp square-wave generator. If large enough to stop oscillations, a dominant roll-off bypass capacitor C_B added across the load would devastate the circuit's bandwidth.

Moreover, under the condition of input overloads, which can occur during turn-on, a high impedance load could create a latch state in conjunction with the diode. If the load impedance supports a great enough voltage, positive feedback takes continuous control at the amplifier's noninverting input. At the inverting input, the photodiode clamps the voltage and prevents negative feedback recovery.

Bootstrapping, though, removes each of the problems caused by load voltage on the photodiode (see Figure 2). In the new circuit, the load voltage drives the end of the photodiode that's grounded in the basic circuit. Also, a feedback-tee circuit option becomes possible. With only the very small op amp differential input error signal across the photodiode, its response is essentially linear. Moreover, the canceled-out positive feedback signal on C_D avoids the square-wave generator action.

Through its effect on feedback, bootstrapping preserves bandwidth in two ways. The negative-feedback network riding on top of the positive-feedback signal always ensures a net negative feedback. The circuit requires little, if any, load bypassing. As a result, this arrangement reduces the bandwidth-limiting bypassing effect of the load and its capacitance comparable to that of traditional current-to-voltage conversion circuits. Also, because positive feedback can no longer dominate, the circuit eliminates input clamping by the photodiode and the latch state.

The bootstrapping circuit also benefits from the use of a feedback-tee network. In the bootstrapping circuit, the tee, like the photodiode, also rides atop the load to similarly avoid the positive-feedback effects. Tee networks offer a degree of frequency-response control. In the tee, capacitor C_1 blocks the low-frequency shunting effects of R_3 to produce a high-pass response without an amplified offset voltage. (Request PDS-653.)

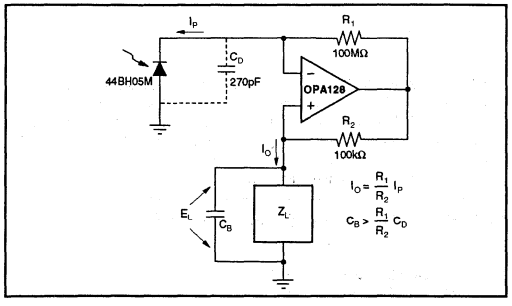


FIGURE 1. Basic Photodiode Circuit.

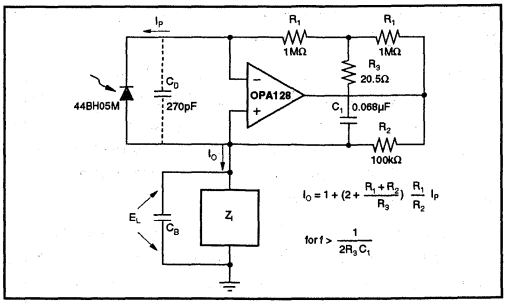


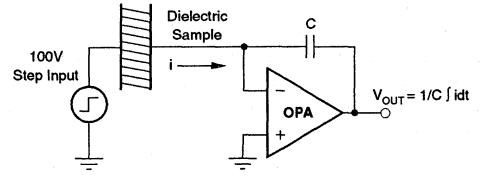
FIGURE 2. Bootstrapped Photodiode Circuit.

BURR-BROWN® APPLICATION BULLETIN

Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

DIODE-CONNECTED FET PROTECTS OP AMPS

Providing input-overload protection for sensitive measurement circuits proves difficult when you must not degrade the circuits' performance in the process. It's an especially tricky problem when you're measuring a material's dielectric properties. In such an application (see Figure 1), an ultra-low input bias current op amp serves as a current integrator to measure a dielectric's response to a 100V step.



STANDARD DIELECTRIC-EVALUATION SCHEMES can prove disastrous to the op amp they employ. If the dielectric under test shorts, the resulting high voltage at the op amp's input destroys the device unless the device's very-low-bias (low voltage) input stage is somehow protected. The solution is difficult: Whatever you do, it must not degrade the op amp's performance.

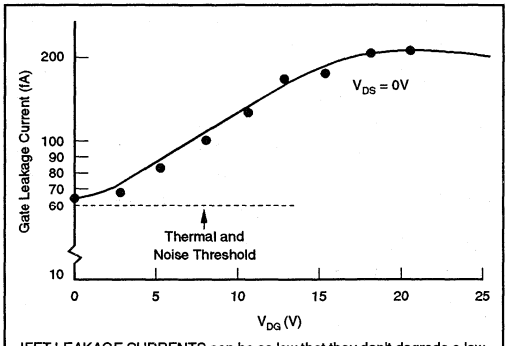
FIGURE 1. Dielectric Evaluation Circuit.

Unfortunately, the op amp is destroyed if the dielectric sample shorts.

For one such measurement setup, low-bias current op amps like the OPA111, OPA121, OPA128, OPA124 or OPA129 can serve because their bias current is in the pA or even fA range and therefore contributes negligible measurement error. What type of protective device doesn't degrade this op amp's parameters? PN-junction devices usually have leakage currents in the nanoamp range even at very-low bias voltages—a degradation of several orders of magnitude. FETs are generally much better in this respect, and Siliconix's 2N4117A JFET proves the best.

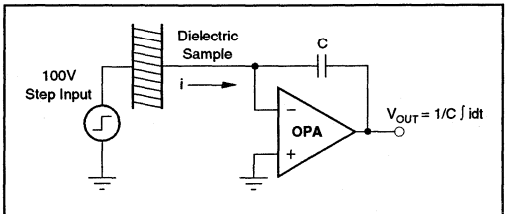
Figure 2 shows an experimentally derived curve of leakage current vs voltage for this device. Note that for voltages comparable to those between an op amp's inputs, the 2N4117A's leakage is compatible with the op amp's bias. (The residual 60fA level at 0V arises from thermal effects and measurement-system noise.)

The overload-protected design resulting from these FET measurements is shown in Figure 3. The diode-connected JFET serves as a shunt across the op amp's input—a scheme that limits the differential input to 0.6V if the dielectric shorts. Resistor R_i limits the maximum short-circuit current to the 50mA level specified in the FET's data sheet. R_i's effect on measurement accuracy is negligible because the dielectric's impedance is very much greater than the resistor's 2kΩ value.



JFET LEAKAGE CURRENTS can be so low that they don't degrade a low-input bias op amp's parameters. Measurements show that Siliconix's 2N4117A can serve as a voltage limiter when it's diode-connected. The actual leakage is probably somewhat lower than measured, but thermal effects and noise place a limiting threshold on the measurement.

FIGURE 2. Curve of Leakage Current vs Voltage.



OVERVOLTAGE PROTECTION results when you incorporate a diode-connected JFET in the measuring circuit. If the dielectric shorts during testing, the FET clamps at 0.6V saving the sensitive op amp from destruction. R_i's resistance—although high enough to protect the FET against overcurrent failure—is still so small relative to the dielectric's impedance that it doesn't impair measurement accuracy.

FIGURE 3. Overvoltage Protection Circuit.

Reprinted from EDN, October 5, 1980;

BURR-BROWN®
APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

SINGLE-SUPPLY OPERATION OF OPERATIONAL AMPLIFIERS

One of the most common applications questions on operational amplifiers concerns operation from a single supply voltage. "Can the model OPAxyz be operated from a single supply?" The answer is almost always yes. Operation of op amps from single supply voltages is useful when negative supply voltages are not available. Furthermore, certain applications using high voltage and high current op amps can derive important benefits from single supply operation.

Consider the basic op amp connection shown in Figure 1a. It is powered from a dual supply (also called a balanced or split supply). Note that there is no ground connection to the op amp. In fact, it could be said that the op amp doesn't know where ground potential is. Ground potential is somewhere between the positive and negative power supply voltages, but the op amp has no electrical connection to tell it exactly where.

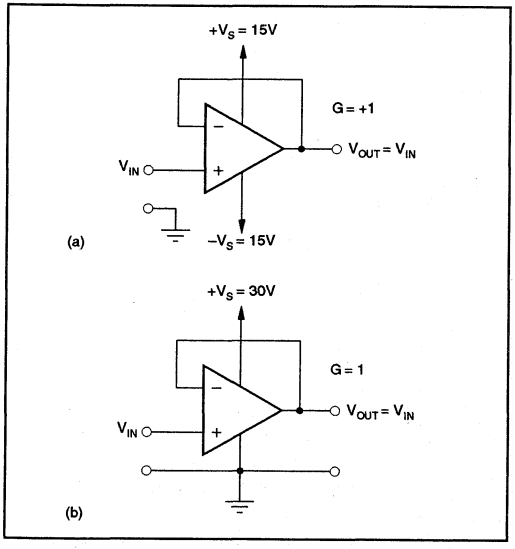


FIGURE 1. A simple unity-gain buffer connection of an op amp illustrates the similarity of split-supply operation (a) to single-supply operation in (b).

The circuit shown is connected as a voltage follower, so the output voltage is equal to the input voltage. Of course, there are limits to the ability of the output to follow the input. As the input voltage swings positively, the output at some point near the positive power supply will be unable to follow the input. Similarly the negative output swing will be limited to somewhere close to $-V_S$. A typical op amp might allow output to swing within 2V of the power supply, making it possible to output –13V to +13V with ±15V supplies.

Figure 1b shows the same unity-gain follower operated from a single 30V power supply. The op amp still has a total of 30V across the power supply terminals, but in this case it comes from a single positive supply. Operation is otherwise unchanged. The output is capable of following the input as long as the input comes no closer than 2V from either supply terminal of the op amp. The usable range of the circuit shown would be from +2V to +28V.

Any op amp would be capable of this type of single-supply operation (with somewhat different swing limits). Why then are some op amps specifically touted for single supply applications?

Sometimes, the limit on output swing near ground (the "negative" power supply to the op amp) poses a significant limitation. Figure 1b shows an application where the input signal is referenced to ground. In this case, input signals of less than 2V will not be accurately handled by the op amp. A "single-supply op amp" would handle this particular application more successfully. There are, however, many ways to use a standard op amp in single-supply applications which may lead to better overall performance. The key to these applications is in understanding the limitations of op amps when handling voltages near their power supplies.

There are two possible causes for the inability of a standard op amp to function near ground in Figure 1b. They are (1) limited common-mode range and (2) output voltage swing capability.

These performance characteristics are easily visualized with the graphical representation shown in Figure 2. The range over which a given op amp properly functions is shown in relationship to the power supply voltage. The common-mode range, for instance, is sometimes shown plotted with respect to another parameter such as temperature. A ±15V supply is assumed in the preparation of this plot, but it is easy to imagine the negative supply as being ground.

In Figure 2a, notice that the op amp has a common-mode range of –13V to +13.5V. For voltages on the input terminals of the op amp of more negative than –13V or more positive than +13.5V, the differential input stage ceases to properly function.

Similarly, the output stages of the op amp will have limits on output swing close to the supply voltage. This will be load-dependent and perhaps temperature-dependent also. Figure 2b shows output swing ability of an op amp plotted with respect to load current. It shows an output swing capability of –13.8V to +12.8V for a 10kΩ load (approximately ±1mA) at 25°C.

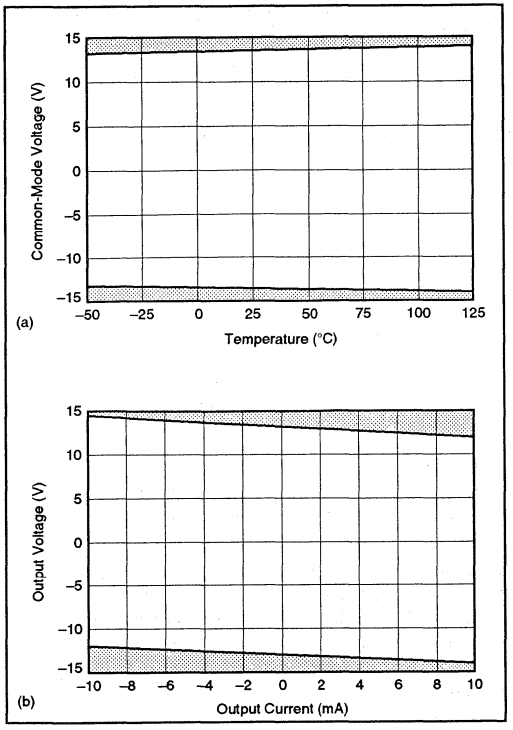


FIGURE 2. The Common-mode Range of an Op Amp is Usually Dependent on Temperature. This behavior is shown plotted in (a). Output voltage swing will be affected by output current. (b). Often the op amp load is connected to ground, so load current is always positive. Furthermore, as the output voltage approaches zero, load current approaches zero, increasing the available output swing. A split power supply voltage (normally ±15V) is assumed in preparation of these plots.

So the circuit of Figure 1b is limited to +13V output by output swing capability and –13V by negative common-mode range. A single-supply op amp is specifically designed to have a common-mode range which extends all the way to the negative supply (ground). Also, its output stage is usually designed to swing close to ground.

It would be convenient if all op amps were designed to have this capability, but significant compromises must be made to achieve these goals. Increased common-mode range, for instance, often comes at the sacrifice of performance characteristics such as offset voltage, offset drift, and noise. General purpose applications may tolerate op amp performance with these compromises, but high accuracy or other special purpose applications may require a different approach.

Fortunately, there are many ways to use high performance and special purpose op amps in single-supply applications. As demonstrated in Figure 1b, an op amp with typical common mode and output characteristics functions well on a single supply as long as the input and output voltages are constrained to the necessary limits. Circuit configurations must be used which operate within these limits.

Figure 3 shows a circuit, for instance, which references the input and output to a "floating ground" created with a zener diode. The zener diode is biased with a current set by R_Z. Since V_{IN} and V_{OUT} are both referenced to the same floating ground, the zener voltage accuracy or stability is not critical. V_{IN} and V_{OUT} can now be bipolar signals (with respect to floating ground). With +V = 30V and V_Z = 15V, operation is similar to standard split supply operation. The load current in this circuit, however, flows to the floating ground where it will add to the zener diode current (negative load currents subtract from zener current). The zener diode must be selected to handle this additional current. If the zener current is allowed to approach zero, the floating ground voltage will fall rapidly as the zener turns off. R_1 must be selected so that the zener diode current remains positive under all op amp load conditions.

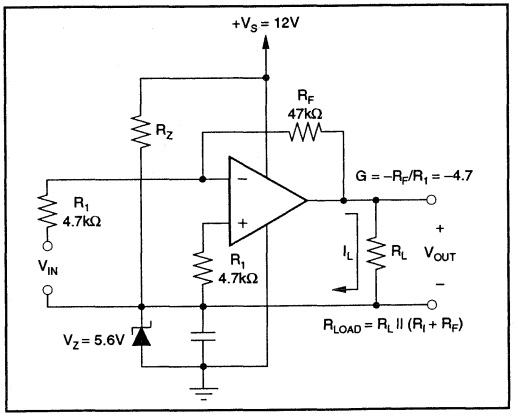


FIGURE 3. Bipolar Signals Can be Handled When Input and Output are Referenced to a Floating Ground. Changing load current causes a variation in zener current which must be evaluated.

Figure 4 shows operation in a noninverting gain configuration. In this circuit, the feedback components present an additional load to the op amp equal to the sum of the two resistors. This current must also be considered when planning for the variation in current flowing in the zener diode. Again, the zener current should not be allowed to approach zero or exceed a safe value.

Notice that in this example, a single +12V supply is shown. Often, single-supply applications use supply voltages which are considerably less than the 30V total (±15V) at which the

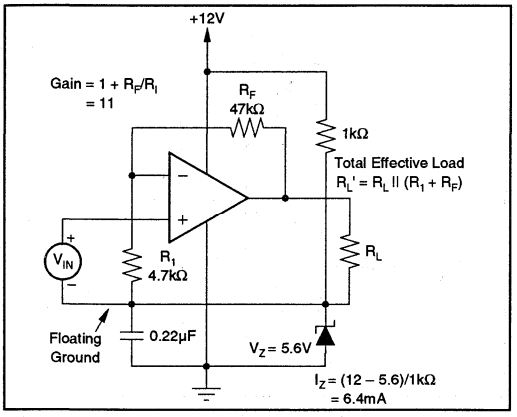


FIGURE 4. As with Conventional Split-Supply Operation, a Noninverting Gain Configuration Can Be Acheived. The feed back components create an additional load for the op amp which flows in the zener diode. Basic performance characteristics of the circuit are the same as for split supply operation.

performance of most op amps is specified. While modern op amps generally perform well at less than their characterized voltage, this needs to be verified. Some op amps, although they are specified to operate at lower voltage, suffer degraded power supply and common-mode rejection as their minimum operating voltage is approached.

Extremes of common-mode voltage on some amplifiers may produce unexpected behavior. Certain types of FET input op amps, for instance, exhibit much greater input bias current when the common-mode voltage relative to either of the power supplies exceeds 15V to 20V. This could occur with single-supply operation of 30V and common-mode voltage unbalanced nearer one supply or the other. The actual amplifier performance should be verified with the expected worst-case common-mode voltage conditions.

Resistor voltage dividers are sometimes used to establish floating ground (Figure 5). The impedance of the ground is determined by the parallel combination of the divider resistors. Unless these resistors are made very low in value (consuming significant power supply current), this will lead to higher "ground" impedance. But with careful attention to the effects of varying load current in the reference point, this approach may prove useful. In fact, it may not be important in some applications that a truly "solid" ground be established since input and output are referenced to the same node. Good bypassing, however, will help avoid transient disturbances of V_G, or oscillation problems by providing a lower high frequency impedance without low value divider resistors.

Appropriate voltage points often exist in related circuitry which can be useful in establishing a floating ground. In Figure 6, a +5V source used to power logic circuitry is used as a floating ground. Beware that most regulators used to supply these voltages are designed to source current to a load only. If sufficient op amp load current flows into the 5V line, its voltage will rise. Again, load currents should be evaluated to assure that the floating ground voltage remains well defined. Normally other system components would sufficiently load the regulator to allow for plenty of op amp load current.

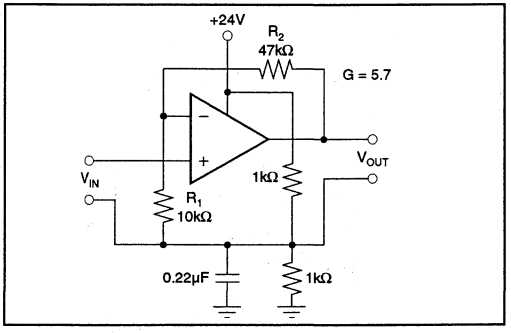


FIGURE 5. Even Though the Impedance of the Voltage Divider is in Series with R_1 to Ground, the Gain of this Noninverting Circuit is Determined Solely by R_1 and R_2. Since the input and output are referenced to the same floating ground, its impedance does not affect the voltage gain of the circuit.

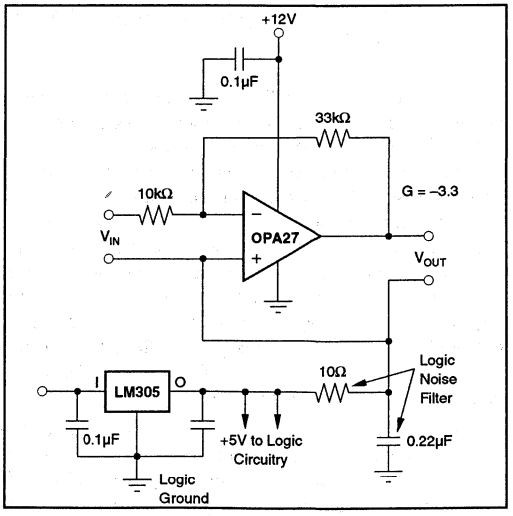


FIGURE 6. Many Systems Have a +5V Logic Supply or Other Appropriate Voltage Source which Can Be Used as a Floating Reference Potential for Analog Circuitry. Be sure logic noise does not enter the analog system by providing an adequate decoupling network or additional bypassing.

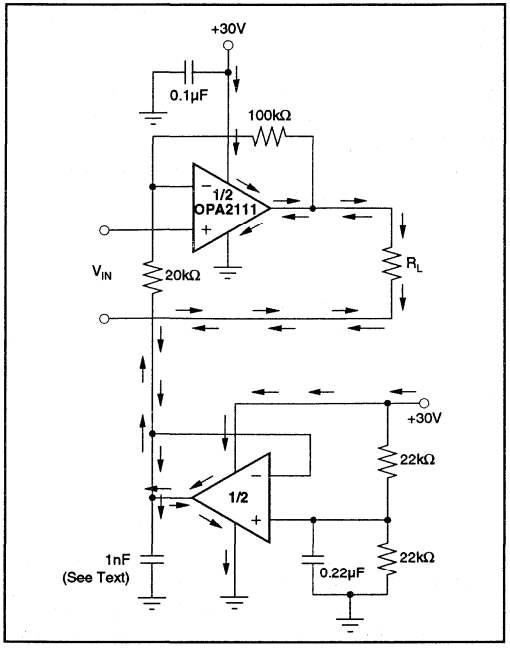


FIGURE 7. A Very-Low Floating Ground Impedance is Provided by Using One Section of the OPA2111 Op Amp Connected as a Unity-Gain Buffer. Input to the buffer is a voltage divider which can be heavily bypassed. The arrows indicate the direction of positive and negative load current flow.

Particularly demanding applications may require that a buffer op amp be used to establish a very low impedance floating ground. Input to the buffer (Figure 7) could come from any of the previously discussed techniques. The buffer can both source and sink load current up to the output current limits of the op amp used as the buffer. The closed-loop output impedance of the op amp provides a very solid reference ground. Frequency response and open-loop output impedance characteristics of the buffer op amp will determine the high frequency floating ground impedance. Bypassing the output of the buffer amp may help lower the high frequency impedance, but don't exceed a safe capacitive load of the buffer amp or oscillations may result.

Figure 8 shows a technique often used with high voltage and high current op amps. Here, an unbalanced power supply is used to produce the desired output voltage swing. In applications such as a programmable power source, the output voltage is required to go all the way to the ground. A small negative supply is used to provide the necessary common-mode voltage and output stage requirements to allow full output swing to ground. A much larger positive voltage supply can now be used to maximize the available output voltage.

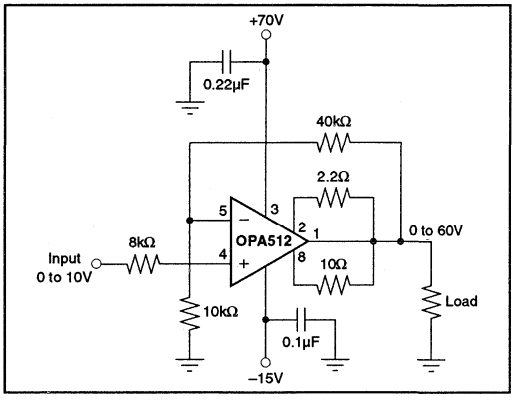


FIGURE 8. Unbalanced Power Supplies are Often Used with Power Op Amps to Achieve Higher Unipolar Output Voltage Yet Provide Output Swing Down to 0V. The negative supply voltage in this OPA512 circuit is made large enough to provide the common-mode voltage and output swing requirements of the application.

A higher current limit (lower value current limit resistor is set for positive output current in this circuit since the primary purpose is to source current to a load connected to ground. Be sure to consider the safe operating area constraints carefully in this type of operation. Unequal supplies mean that larger voltages will be present across the conducting output transistor, thus requiring greater safe operating area. See *Understanding Power Amplifier Specifications*, Application Bulletin AB-123, for information on evaluation of safe operating area.

Other signal processing circuits which are normally powered from a split supply can be operated from a single supply as well. These include such devices as instrumentation amplifiers, current transmitters, analog multipliers, log amps, etc. The principles in assuring proper operation are the same as for op amps.

The INA105 difference amplifier provides an instructive example. This device is comprised internally (Figure 9) of a precision op amp and four precision matched resistors. In a majority of applications pin 1 is connected to ground. This is the output voltage reference pin. If pin 1 is referenced to a floating ground using one of the previously described techniques, operation is similar to split-supply operation. Unlike the op amp applications previously described, however, the differential input terminals (pins 2 and 3) will be capable of accommodating common-mode voltages equal to and even greater than the supply voltages. Voltages applied to the input resistors are divided down, maintaining common-mode voltages to the op amp within operating limits. In this case, the voltage at pin 1 in conjunction with the required output swing determines the technique required for single-supply operation.

True instrumentation amplifiers (Figure 10) usually have an op amp at their input. Therefore, common-mode range of the input op amp again becomes a concern. Input voltages must be confined to within the specified common-mode range of the device. The output section of the instrument amp is like the difference amplifier and output voltages swing requirements will dictate the techniques required.

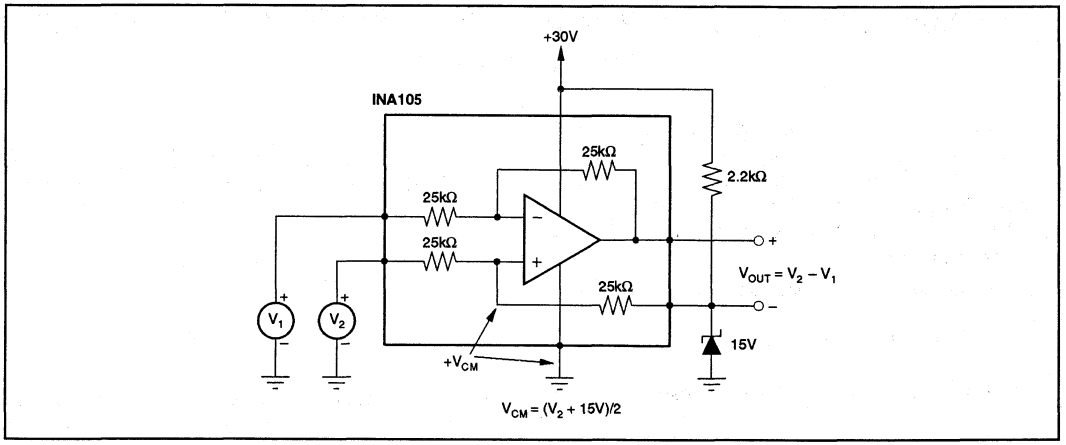


FIGURE 9. The Input Voltage to this Simple Difference Amplifier is Divided Down by the Input Resistors Before Being Applied to the Op Amp. Thus it is able to handle voltages which are equal to or greater than the power supply voltage.

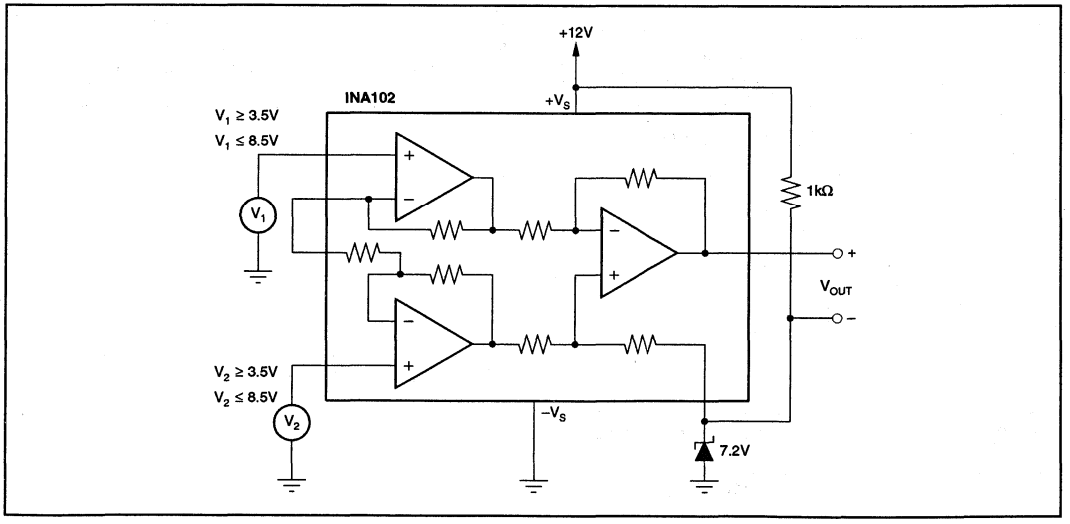


FIGURE 10. Inputs to the Instrumentation Amplifier Are Applied Directly to the Active Circuitry of the Input Op Amps and Therefore are Subject to the Common-Mode Range Limitations of these Op Amps.

BURR-BROWN® APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

COMPENSATE TRANSIMPEDANCE AMPLIFIERS INTUITIVELY

By Tony Wang and Barry Ehrman

Transimpedance amplifiers are used to convert low-level photodiode currents to usable voltage signals. All too often the amplifiers have to be empirically compensated to operate properly. The problem can be easily understood if one looks at all the elements involved. Figure 1 shows the typical photodiode application.

The ideal transimpedance transfer function is, by inspection:

$$V_{OUT} = -I_S \bullet Z_F = -I_S \bullet \frac{R_F}{1 + j\,2\pi\,f\,R_F C_F}$$

This equation suggests that the frequency response is strictly due to the feedback network. This does not explain why transimpedance amplifiers are prone to oscillate. Figure 2 provides more insight into the stability problem. The photodiode is replaced with an ideal current source in parallel with its equivalent resistance, R_D, and capacitance, C_D. The op amp input capacitance cannot be considered insignificant and should be included as part of C_D.

The noise gain (i.e., the noninverting closed-loop gain) of this configuration determines the stability of the circuit. The reason for this is that any noise signal, no matter how small, can trigger an unstable circuit into oscillation. From inspection, the transfer function can be determined to be:

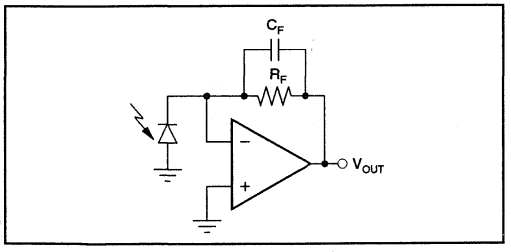


FIGURE 1. Typical Photodiode Transimpedance Amplifier.

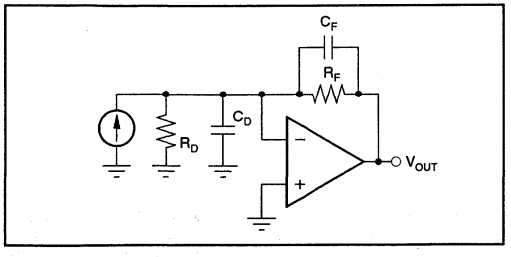


FIGURE 2. Photodiode Modelled with Ideal Elements.

$$A_{CL}(f) = \frac{R_F + R_D}{R_D} \bullet \frac{1 + j\,2\pi\,f\left[\frac{R_F R_D}{R_F + R_D}\right](C_F + C_D)}{1 + j\,2\pi\,f\,R_F C_F}$$

$$= \frac{R_F + R_D}{R_D} \bullet \frac{1 + j\,\frac{f}{f_Z}}{1 + j\,\frac{f}{f_P}}$$

The dc gain is set solely by the resistors. The pole frequency, f_P, is set by the feedback network, just as in the transimpedance function. The zero frequency, f_Z, is determined by (a) the sum of the feedback and the diode capacitances and (b) the parallel combination of the feedback and the diode resistances.

Typically, the feedback resistor is much smaller than the photodiode's equivalent resistance. This makes the dc resistive gain unity. The value of the parallel combination is essentially equal to the feedback resistor alone. Therefor, f_Z will always be lower than f_P, as shown in Figure 3.

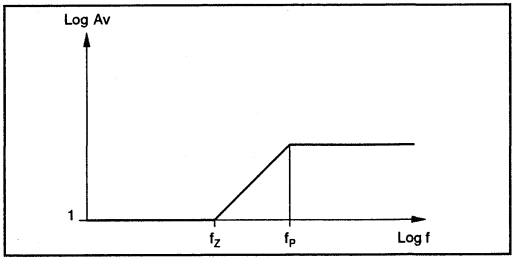


FIGURE 3. Bode Plot of Noise Gain.

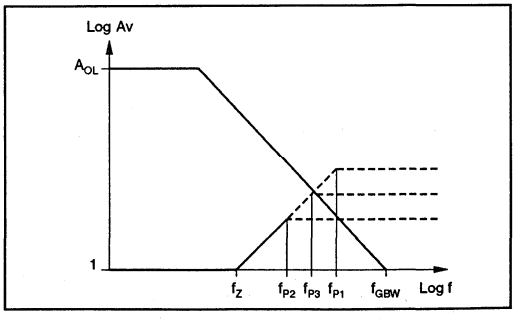


FIGURE 4. Various Feedback Responses Intersecting Op Amp Open-loop Gain.

Figure 4 depicts three different scenarios for the intersection of the closed-loop response curve with the open-loop gain curve. Stability degradation will occur when f_P falls outside the open-loop gain curve. For f_{P1} the circuit will oscillate. If f_P lies inside the open-loop gain curve, the transimpedance circuit will be unconditionally stable. This is the case for f_{P2} but stability is traded off for transimpedance bandwidth. The optimum solution paces f_P on the open-loop gain curve as shown for f_{P3}.

Since f_P is determined by the feedback network, judicious selection of C_F is all that is necessary. This process can be greatly simplified by noting that the high frequency asymptote for the noise gain is determined by capacitance values alone:

$$A_{CL}(f >> f_P) = \frac{C_F + C_D}{C_F}$$

This value should be equal to the op amp's open-loop gain at f_P. The open-loop gain is found by dividing the op amp's gain-bandwidth product (GBW) by f_P. Setting these two expressions equal yields:

$$\frac{GBW}{f_P} = \frac{C_F + C_D}{C_F}$$

Simple substitution yields a quadratic equation whose only real, positive solution is:

$$C_F = \frac{1}{4\pi R_F GBW}\sqrt{(1 + \quad 1 + 8\pi R_F C_D GBW)}$$

This simple equation selects the appropriate feedback capacitor for guaranteed stability once the op amp's minimum gain-bandwidth and the photodiode's maximum capacitance are determined.

Further insight can be gained with some simplifying assumptions and a little algebra:

$$f_P \approx \sqrt{\frac{GBW}{2\pi R_F C_D}}$$

This result indicates that, for a given op amp and photodiode, transimpedance bandwidth is inversely related to the square root of the feedback resistor. Thus, if bandwidth is a critical requirement, the best approach may be to opt for a moderate transimpedance gain stage followed by a broadband voltage gain stage.

BURR-BROWN® APPLICATION BULLETIN

Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

FEEDBACK PLOTS DEFINE OP AMP AC PERFORMANCE

By Jerald G. Graeme (602) 746-7412

(Originally published in EDN magazine as "Feedback Plots Offer Insight into Operational Amplifiers" and "Bode Plots Enhance Feedback Analysis of Operational Amplifiers" on 1/19/89 and 2/2/89, respectively.)

Feedback plots simplify the analysis of an op amp's closed-loop AC performance by showing bandwidth and stability conditions as a function of the op amp's gain and phase response. These plots also provide insight into noise performance and the special feedback requirements of circuits such as integrating converters, photodiode amplifiers, composite amplifiers and active feedback circuits.

Engineers routinely use Bode plots[1] to determine the bandwidth and frequency stability of voltage-gain op amp circuits. A Bode plot provides a visual representation of an op amp's transfer response and its potential stability. Moreover, such plots define the circuit's pole and zero locations at the intercepts of the response-curve extensions.

The Bode plot of Figure 1, for example, shows the interaction of the magnitude response of the open-loop gain (|A|) and the reciprocal of the feedback factor (1/β). The fraction of the output that feeds back to the input is β. The voltage-divider action of Figure 1's feedback network determines the value of β; for moderate resistance values, $\beta = R_1/(R_1 + R_2)$. For this noninverting example, the feedback equation, $A_{CL} = A/(1 + A\beta)$, defines the closed-loop voltage gain. Aβ is the loop gain, and where it is high:

$$A_{CL} \approx 1/\beta = (R_1 + R_2)/R_1$$

Aβ represents the amplifier gain available to maintain the ideal closed-loop response. At the point where the loop gain no longer matches the feedback demand, the closed-loop curve deviates from the ideal. The Bode plot graphically defines this limit by plotting the 1/β curve with the gain-magnitude response curve of the op amp. Because the 1/β line represents the feedback demand, closed-loop requirements will be satisfied as long as this line is below the amplifier-gain curve. Where this condition is no longer true, the actual response drops, following the amplifier's open-loop response downward. The rate of descent for the roll-off is –20dB/decade (for most op amps) and is characteristic of a single-pole response. In Figure 1, the heavier line on the gain-magnitude plot depicts the resulting closed-loop curve.

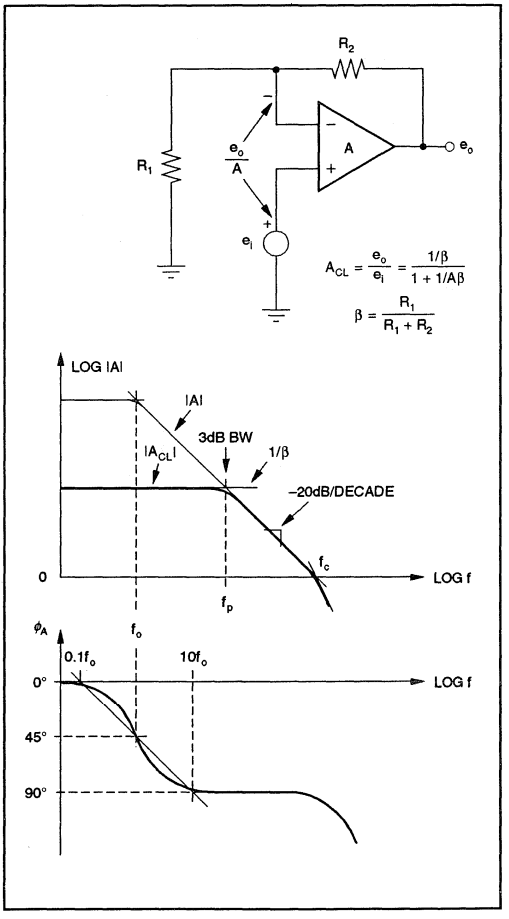


FIGURE 1. This feedback analysis provides a summary of loop conditions in the 1/β curve and defines the underlying poles, zeros, and phase shift.

INTERCEPT DEFINES BANDWIDTH

For a basic voltage-gain amplifier, the location of the f_p pole determines the closed-loop bandwidth. In this case, a single-pole roll-off determines the point at which the gain magnitude goes below 3dB (equivalent to 0.707 of its low-frequency level). To find this point relative to the Bode plots, rewrite the closed-loop gain as

$$A_{CL} = (1/\beta)/(1/A\beta + 1)$$

The bandwidth-defining gain error is a result of the 1/Aβ term in the denominator. Because β is constant for the circuit in Figure 1, the amplifier gain (A) determines the frequency dependence of the loop gain. For a typical op amp, the gain-

bandwidth product is constant after the first break frequency occurs and $A = jf_c/f = j|A|$ where f_c is the amplifier's unity-gain crossover frequency. For this common condition,

$$A_{CL} = (1/\beta)/(1 + 1/(j|A|\beta)$$

The bandwidth is defined in terms of the absolute value (magnitude) of A_{CL}:

$$|A_{CL}| = (1/\beta)/\sqrt{(1 + 1/(|A|^2\,\beta^2))}$$

which, at the –3dB point, becomes

$$|A_{CL}| = 0.707(1/\beta) = (1/\beta)/\sqrt{2}$$

Comparing the last two expressions, you can see that the –3dB bandwidth occurs when $|A| = 1/\beta$. This equality is true when the gain supply drops to the exact level of the feedback demand. When you plot these two functions on the same graph, they reach equality at the intersection of the two curves. This intercept pinpoints the closed-loop pole location and defines the circuit bandwidth for the voltage-gain amplifier.

STABILITY PREDICTED FROM THE INTERCEPT

This critical intercept point also exhibits other characteristics that can help you define conditions for frequency stability. By relating the phase shift to the slopes of the gain-magnitude and $1/\beta$ curves, you can determine the loop phase shift at this intercept. Again, the importance of the intercept is apparent from the closed-loop-gain expression, $A_{CL} = A/(1 + A\beta)$. If $A\beta$ becomes –1, the closed-loop gain will be infinite and will support an output signal even in the absence of an input signal, which is a condition for oscillation. The magnitude of $A\beta$ is unity only at the intercept point because it is at this point that $A = 1/\beta$; a negative polarity for $A\beta$ only requires 180° phase shift.

Virtually every practical analog circuit is a minimum-phase system. For such systems, which have only left-half-plane poles and zeros, you can directly read the phase shift from the gain-magnitude response[2]. Although many op amps do have a right-plane zero caused by Miller phase compensation, the effects of this zero are suppressed below the unity-gain crossover. For the case of a minimum-phase system, a pole creates a –20dB/decade response roll-off and a –90° phase shift; a zero produces the same effects but with opposite polarities. Additional poles and zeros simply add to the response slope and phase shift in increments of the same magnitude.

Relying on the feedback phase shift's correlation with the response slope, you can determine its value at the critical intercept from the gain-magnitude and $1/\beta$ curves. For the example of Figure 1, the gain-magnitude curve has a slope of –20dB/decade and the $1/\beta$ curve has a zero slope for a net 90° feedback phase shift at the intercept. This situation leaves a phase margin of 90° out of the 180° that would cause oscillation. Because the intercept is well removed from the open-loop-response break frequencies, the analysis of this example is easier to understand. The intercept occurs after the amplifier's first pole develops the full 90° phase shift, but well before the second pole has any effect.

APPROXIMATING PHASE MARGIN

In cases where the intercept is less than one decade from a response break, the Bode approximation of the phase shift shows a linear slope that has a maximum error of 5.7°[1]. For Figure 1, the phase-shift approximation starts at 0° one decade before the break frequency f_o. From there, it increases linearly on the log scale to 45° at the break frequency and then to 90° one decade above it.

Using this approximation, you can combine the stability criteria for loop-gain magnitude and feedback phase shift to obtain the rate-of-closure indicator. Rather than computing phase shifts from slopes, you can use this indicator to deal with the slopes directly. Rate-of-closure is simply the difference in slopes of the gain-magnitude curve and the $1/\beta$ curve when they intercept. This difference reflects the combined phase shift around the feedback loop. For Figure 1, the rate-of-closure is 20dB/decade, which corresponds to a stable 90° phase shift.

In other cases, the slope of the $1/\beta$ curve is not zero, giving a 40dB/decade rate-of-closure that indicates an oscillatory 180° of phase shift. Rate-of-closure alone is an exact stability indicator where the intercept is at least one decade away from all other break frequencies. In still other cases, the Bode phase approximation modifies the rate-of-closure result.

FEEDBACK FACTOR IS A VOLTAGE DIVIDER RATIO

To use feedback relationships to perform circuit analysis, you should consider the feedback network separately. This separation parallels the nature of the op amp's open-loop gain, which is a characteristic of the amplifier in the absence of the feedback network. You only need to retain the loading effects between the amplifier and the feedback network to determine their individual responses[2]. Then, by putting the two responses on the same plot, you can see how they will work together.

Figure 2 shows a generalized feedback condition defined by Z_1 and Z_2. The equations of Figure 2a directly determine the circuit response for high loop gain and moderate impedances. Nonetheless, the input impedance of the amplifier alters the simplified results of these equations by shunting the feedback network. The inclusion of this loading effect on the feedback network completes the $1/\beta$ analysis in the circuit of Figure 2b. Here, the op amp input resistance (R_i), differential input capacitance (C_{id}), and common-mode input capacitance (C_{icm}) all shunt impedance Z_1. Except for conditions where the feedback impedances have low values, you need to include these amplifier characteristics in your analysis.

Where there is impedance in series with the amplifier's noninverting input, you must add this too-along with the shunting effect of the input's C_{icm} capacitance. You can then find the feedback factor from the divider action, e_i/e_o. For the $1/\beta$ curve, this result is inverted and, in the logarithmic format of computer simulations, becomes simply

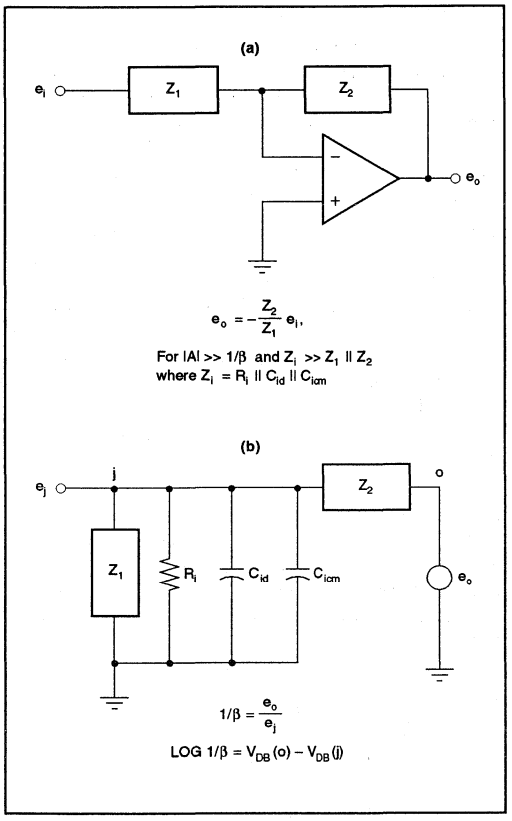


FIGURE 2. To determine the 1/β curve for the generalized circuit of (a), you can draw a voltage-divider circuit that represents the feedback network and the shunting effects of the amplifier input (b).

$V_{DB}(o) - V_{DB}(j)$. By adding this curve to the plot of the amplifier's gain-magnitude response, you can display the characteristics of the critical intercept for subsequent feedback interpretation.

NOISE GAIN AND 1/ß

The 1/β curve also communicates performance information across the entire response range of the op amp. For example, it displays loop gain, which provides an indication of gain accuracy vs frequency and the ultimate bandwidth limit. Furthermore, the 1/β curve demonstrates that the circuit's signal bandwidth can be different from its noise bandwidth. Note that the previous feedback-network analysis returns Z_1 to ground as it would in a noninverting op amp configuration, even though the op amp shown is in the inverting mode.

Underlying the difference between noise and signal bandwidth is the concept of noise gain, which is the source of some of the more common op amp application problems.

For any given feedback network, the inverting and noninverting configurations develop signal gains that differ in magnitude as well as in sign; nevertheless, the feedback conditions remain the same. In both cases, your feedback analysis is concerned with the gain-error voltage developed between the op amp inputs. This error signal always receives the gain of the noninverting connection, as you would see if you performed superposition analysis. Superposition of the signal between the amplifier inputs grounds the signal source, producing the noninverting configuration.

The same condition holds true for the input voltage noise of an op amp, resulting in the noise-gain characteristic for the 1/β curve. In practice, the noise gain and the 1/β curve are the same—until they intercept with the gain-magnitude curve. After that, the noise gain rolls off with the amplifier open-loop response but the 1/β curve continues on its path. For the noninverting voltage amplifier, the noise gain and the closed-loop gain, A_{CL}, are the same.

NOISE BANDWIDTH

In inverting configurations, this correspondence does not hold true, giving rise to frequent surprises during attempts at noise filtering. The simplest case of the inverting amplifier, where it is common practice to bypass the feedback resistor, serves to illustrate the inverting relationship (Figure 3). Bypassing the feedback resistor is intended to limit noise bandwidth, and it does indeed remove noise presented as an input signal. However, the circuit will continue to pass amplifier noise across the entire op amp bandwidth. C_f shunts the signal supplied through R_1 for the desired lowpass roll-off of the op amp's e_o/e_i response. To the op amp noise voltage, e_n, C_f merely presents the unity feedback of a voltage-follower. Noise gain drops to unity but continues out to the open-loop roll-off of the op amp. This leveling off of 1/β also shows why the op amp must be unity-gain stable, even though the circuit gain has been rolled off well below the amplifier response. With 1/β following the unity gain axis, the critical intercept occurs at f_c.

While the continued noise gain is at a lower level, it covers much of the amplifier bandwidth, which can result in a dramatic increase in output noise. For example, if you're using the 2MHz Burr-Brown OPA111 shown and choose C_f to obtain a 2kHz roll-off, only 0.1% of the amplifier bandwidth will be enclosed in the intended system response. Although the logarithmic scale of the frequency axis may be visually deceptive, the remaining 99.9% of the bandwidth is still available to the amplifier's voltage noise. For an initial gain of 10, the output noise that this amplifier produces is more than doubled by the bandwidth effect. Many active-filter configurations are subject to the same limitation.

The only way to avoid excessive noise bandwidth is to restrict the frequency range of the op amp. By doing so, the control of the noise response switches from the 1/β curve to the amplifier roll-off. Where the op amp has provision for external phase compensation, this control is a simple matter and permits you to remove bandwidth from signal and noise

alike. However, because most op amps lack an external-phase-compensation facility, passive filtering within the feedback loop offers a broader solution[3]. Such filtering introduces a capacitive shunt to ground following the amplifier but within the feedback loop.

You can also demonstrate the extended noise bandwidth of an integrating converter using a feedback plot but, more importantly, the curves illustrate the dynamic-range limit for integrator-based instrumentation. In Figure 4, the integrator 1/β curve also levels off at the unity-gain line for continued noise gain out to where the op amp rolls off. Be aware that this action has far less noise significance for the integrator because of its increasing gain at lower frequencies. Integrators designed for operation to 1kHz or even higher are generally unaffected by the added noise bandwidth.

Nevertheless, the feedback plot for the integrator demonstrates a unique bandwidth limitation involving two critical intercepts. Not only does the 1/β curve intercept the gain-magnitude curve at the high-frequency extreme, but it does so at the low-frequency end as well. Each intercept indicates a lack of amplifier gain for support of the feedback and a departure from the ideal response. At the high end, the 1/β curve and noise-gain level off, leaving A_{CL} to continue as long as the loop gain lasts. Next, 1/β intercepts the gain-magnitude curve at f_c where the noise gain rolls off.

This intercept is a high-frequency 3dB point for the integrator response, which then usually rolls up rather than down. Upward response in this region is due to signal feedthrough caused by the feedback elements in the absence of loop control. At the lower frequencies, the increasing gain demand encounters the DC gain limit of the op amp. This intercept marks the second 3dB point for the integrator response, which sets the range for accurate performance. Both intercepts have a 20dB/decade rate-of-closure, indicating stable operation.

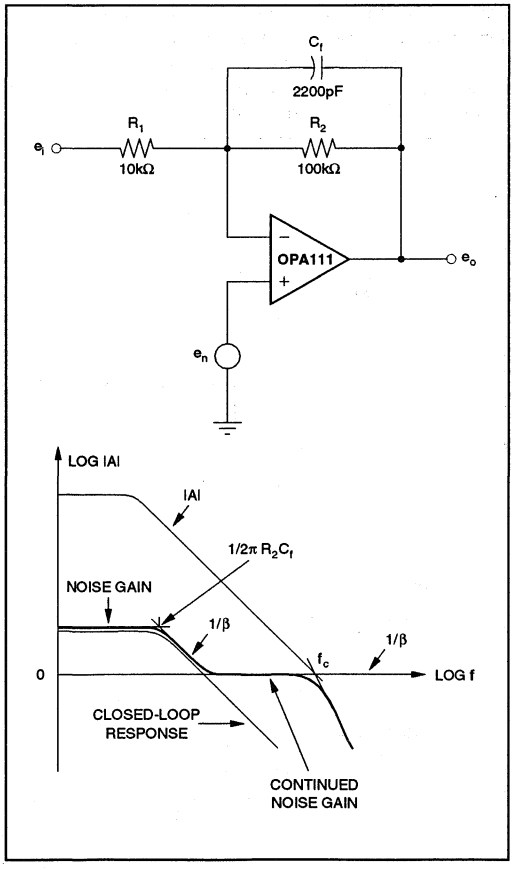


FIGURE 3. Highlighting the difference between closed-loop gain and noise gain, this inverting op amp configuration demonstrates the greater bandwidth that is often available to amplifier noise.

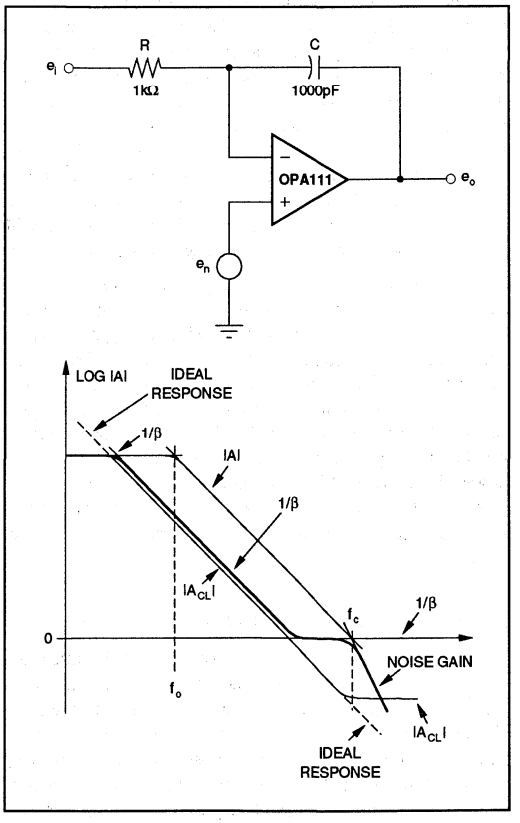


FIGURE 4. Defining the dynamic range for integrating data converters, the integrator 1/β curve displays upper and lower intercepts with the gain-magnitude response.

TWO BANDWIDTH LIMITS FOR INTEGRATORS

Between the two integrator-response limits is the usable dynamic range for dual-slope A/D and V/F converters. The gain error limits this dynamic range; the plots are a graphic representation of this error. The gain error is inversely related either to a circuit's loop gain or the difference between the amplifier's open-loop gain and the feedback demand of 1/β. On the response plots, the loop gain is the vertical distance between the two curves. For the Figure 4 integrator, this separation decreases following 1/βs encounter with the unity-gain axis. From there, the separation finally reduces to zero at f_c. The gain error then becomes the distance between the dashed continuation of the ideal integrator response and the actual A_{CL} response. Graphically, this distance is the source of the large-signal limitation for integrating converters where higher signals correspond to the upper frequencies.

At the other end of the converter range, lower-level signals demand low-frequency integrator operation that encounters a similar limitation. Below the frequency of the op amp's first pole, f_o, the separation between the 1/β and gain-magnitude curves again drops, signaling reduced loop gain. Moving further down in frequency, the 1/β curve finally crosses the op amp's DC-gain level, and the actual response flattens again. For integrating-type converters, this action defines a range of performance that is accurate to within 3dB from f_c down to the lower intercept. To extend the dynamic range, you move the lower intercept downward either with a lower integrator-time-constant or with boosted DC gain.

A higher accuracy dynamic range results from the unique loop-gain conditions of the integrator. The loop gain is constant for the integrator from f_o to its unity-gain crossing. The gain error in this range is constant as marked by the uniform separation of the gain-magnitude and 1/β curves. You can compensate for such an error by making a fixed adjustment to the feedback network, leaving gain-accuracy bounded by the stability of the network. This limit permits you to adjust the more restricted dynamic range to 0.01% levels. For the OPA111 op amp and a 100kHz integrator crossover frequency, this more precise dynamic range has a span of 100,000:1.

INPUT CAPACITANCE ALTERS 1/ß

The previous discussion of the inverter and the integrator considered the feedback network independent of the amplifier input shunting. Although engineers frequently use this simplification, they often encounter unexpected results. Because of the feedback factor, most first-time users of op amps with large feedback-resistance values are surprised by the response curve. Transient-response ringing or even oscillation sometimes occurs; the common cure is a capacitive bypass of the feedback resistor. The 1/β curve can display the problem and provide some guidance in the selection of the bypass capacitor.

Underlying the problem is the op amp input capacitance's effect on the feedback factor. By including this capacitance with the voltage divider formed by the feedback resistors, you can achieve the results of the 1/β curve in Figure 5. This curve rises at high frequencies, increasing the rate-of-closure and flagging the need for closer stability analysis. The phase margin drops as 1/β rises and, at the limit, goes to zero if the 1/β rise spans one decade of frequency. Generally, the span is much smaller than that and the Bode phase approximation evaluates the actual conditions. The key to minimizing the effect on the feedback factor is the low input capacitance that the small input FETs of the OPA128 device provide. The net 3pF of input capacitance leaves the response undisturbed until the parallel combination of the two resistors reaches 50kΩ.

The capacitive bypassing of R_2 increases the high-frequency feedback, which counteracts the shunting of C_{ia} by leveling off the 1/β curve. The selection of this capacitor is better illustrated by Figure 6's photodiode amplifier. You can reduce the non-obvious bandwidth of this application to an equation. The circuit contends with diode capacitances at the input up to 20,000pF. As a result, the break in the 1/β curve is generally far removed from the intercept, making the rate-of-closure analysis accurate without requiring any adjustment of the phase-shift approximation.

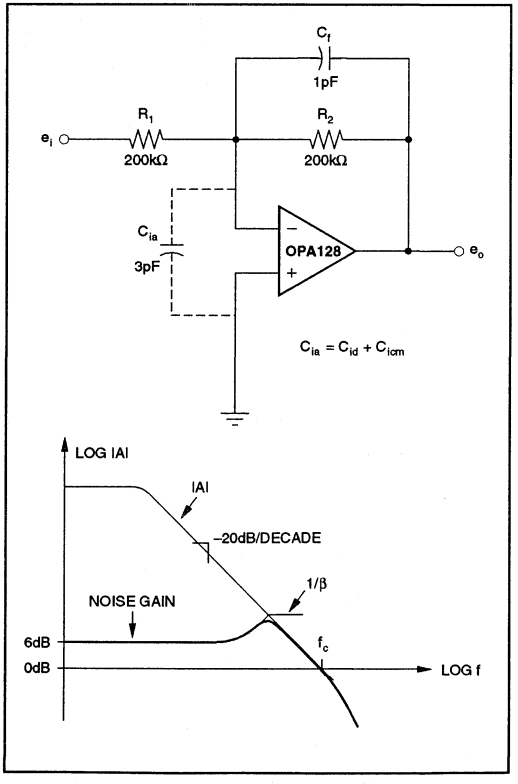


FIGURE 5. Higher feedback resistances will react with the op amp's input capacitance to produce a peaking effect, which the 1/β curve anticipates.

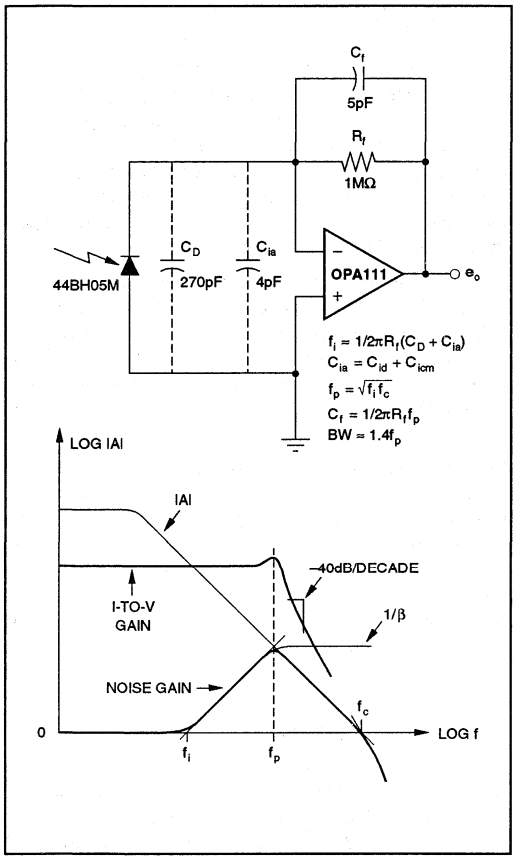


FIGURE 6. A photodiode amplifier's voltage function serves to obscure its bandwidth and stability, but you can rely on feedback-loop conditions to define its performance.

Unfortunately, the bandwidth for the circuit of Figure 6 is obscured by its function. Because its function is a current-to-voltage conversion, rather than simple voltage gain, you cannot draw the signal-gain curve on the gain-magnitude response to estimate bandwidth. When you inspect the circuit to find its bandwidth limitation, you'll see that the only inherent break frequency is that of the feedback resistance and the capacitance of the input circuit. By plotting the 1/β curve, however, you can see that the loop gain remains to support the ideal feedback condition far beyond the f_i break frequency.

Initially, the 1/β curve is flat at unity because of the direct output-to-input connection of R_f. When the feedback is later shunted by C_D and C_{ia}, 1/β rises at a 20dB/decade rate. The transition between these regions occurs at

$$f_i \approx 1/2\pi R_f(C_D + C_{ia})$$

where $C_{ia} = C_{id} + C_{icm}$.

The intercept with the gain-magnitude curve marks the end of the response rise for the noise gain. This curve has a –20dB/decade slope so, if left uncompensated, the rate-of-closure at the intercept will be 40dB/decade. Thus, the plot indicates two poles at that intercept frequency, f_p. This intercept is the point at which there is no longer sufficient amplifier gain for the feedback-factor demand, and it indicates response roll-off independent of the op amp function. Any amplifier function would then roll off with a slope equal to the rate-of-closure.

COMPENSATION BREAKS AT THE INTERCEPT

Because the rate-of-closure is 40dB/decade, you should examine phase shift at the intercept to determine the phase compensation necessary for stability. When the various break frequencies are well removed from the intercept, the rate-of-closure accurately reflects 180° of phase shift for the uncompensated loop. To avoid oscillation and to achieve good damping characteristics, you must reduce this phase shift by at least 45° through roll-off of the 1/β curve.

According to the Bode phase approximation, this phase shift is the amount of phase introduced at a break frequency. Choosing C_f to break with R_f at the intercept frequency, f_p, yields 45° of phase margin. Accompanying this phase condition is a 3dB peak in the signal response, which for a 2-pole response pushes the –3dB bandwidth out to $1.4f_p$. For the OPA111 and the feedback elements shown, the 3dB response extends to 48kHz. (You can extend this analysis to lower capacitance levels, and the common solution mentioned above will still suffice-even for the high-feedback-resistance case of Figure 5.)

As long as C_f breaks with R_f at the frequency of the intercept, the 1/β rise contributes no more than 45° of phase shift. In the range where the op amp phase shift is 90°, this rise leaves a stable 45° phase margin. Nevertheless, as the op amp approaches its crossover frequency, f_c, its contribution to phase shift moves toward 135°. The rule of thumb for selecting C_f remains valid, however, because any intercept near f_c must be a result of a 1/β rise of short duration. The added phase shift of the amplifier, accompanied by a necessary decrease in feedback phase shift at the intercept, results in a net zero effect. By simple sketching of the phase approximations for the 1/β and gain-magnitude curves, you can show this transition.

GEOMETRY DEFINES INTERCEPT

To select the compensation capacitance, it is desirable to reduce the graphical analysis to an equation. Luckily, the response plots provide an elegantly simple solution. Straight-line extensions of the 1/β and gain-magnitude curves form a triangle with the horizontal axis. These extensions have equal but opposite slopes, which form an isosceles triangle. The peak of the triangle, located over the center of its base, lies at the average of the base end points. Mathematically, this average point is equal to

$$\text{Log } f_p = (\text{Log } f_i + \text{Log } f_c)/2$$

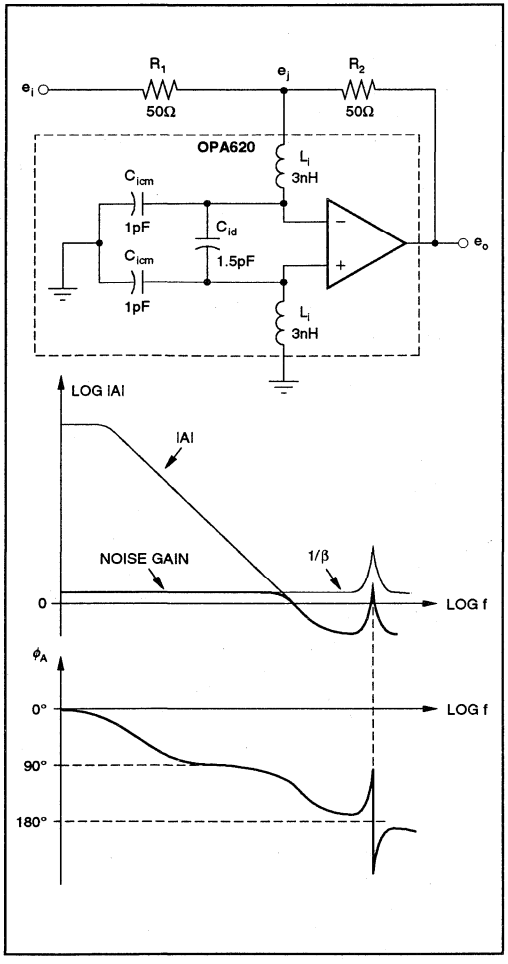


FIGURE 7. Although amplifier gain and phase plots suggest instability, the 1/β curve shows stable conditions for a circuit with input-lead inductance.

Given the expressed logarithmic nature of the frequency axis, you can reduce this relationship to the simple geometric mean of the two characteristic frequencies:

$$f_p = \sqrt{f_i\, f_c}$$

where $f_i = 1/2\pi R_f(C_D + C_{id} + C_{icm})$, and f_c equals the unity-gain bandwidth of the op amp.

GAIN AND PHASE CAN BE MISLEADING

For a third input-circuit effect, the 1/β curve demonstrates stable conditions where typical gain and phase plots would point to oscillation. In addition to input capacitance, op amps have input inductance; this combination produces a high-frequency resonance. The inductance is small but inescapable, being associated with internal input wires and being compounded by external wiring.

For very high-frequency amplifiers, like the OPA620 wideband amplifier of Figure 7, sufficient amplifier gain exists at the resonant frequency to give the appearance of zero gain margin. A comparison of the output signal (e_o) with that at the summing junction (e_j) produces the plot's gain and phase responses. Following unity crossover, the gain curve rises again above the unity axis; this rise generally guarantees oscillation for lower gain levels. Adding to stability concerns is the phase plot, which swings wildly through 180° during the gain peak.

By adding the 1/β curve to the plot, you can see that this curve does not intersect the gain peak but merely rides over it. Without an intercept there is no oscillation, regardless of the phase shift, because the loop gain is insufficient. Loop-gain demand rises in synchronization with the gain peak because the resonant circuit also alters the feedback network.

In many cases, the gain peaking results from conditions in the amplifier output rather than from the input circuit. In such a case, no corresponding modification of feedback occurs, and an intercept and oscillation result. However, for Figure 7, the gain margin remains high, as you can see by the separation between the 1/β curve and the gain response when the phase reaches 180°. This separation remains large throughout the region of higher phase shift, indicating good relative stability.

COMPOSITE AMPLIFIERS

Whereas the normal op amp feedback loop involves only one amplifier, designers often need to extend the feedback loop to work with composite circuits that use two or more op amps for increased gain. By adhering to conventional feedback principles, you can implement phase compensation for the extended loop and rely on a Bode plot to provide a visual representation of the increased gain and the opportunity for extended bandwidth.

For instance, with two op amps in the same loop as in Figure 8, you can achieve increased gain without incurring any added offset and noise error. The input-error effects of the second amplifier are divided by the open-loop gain of the first amplifier. The net open-loop gain of this composite circuit becomes the product of the individual op amp gains and greatly reduces the overall gain error and nonlinearity.

In Figure 8, the two op amps are those of the dual OPA2111, which imposes only a modest cost increase over a single device. You could, of course, select individual op amps to provide specific performance characteristics. In the latter case, you might select the input amplifier for good DC and noise performance and the output amplifier for its load-driving and slewing performance. For example, the output amplifier could handle the load current and the resulting power dissipation, thus producing no thermal feedback to the input of the composite circuit. Moreover, it could also fulfill the high-slew-rate demands of the application. The input amplifier in this case would only swing through small signals.

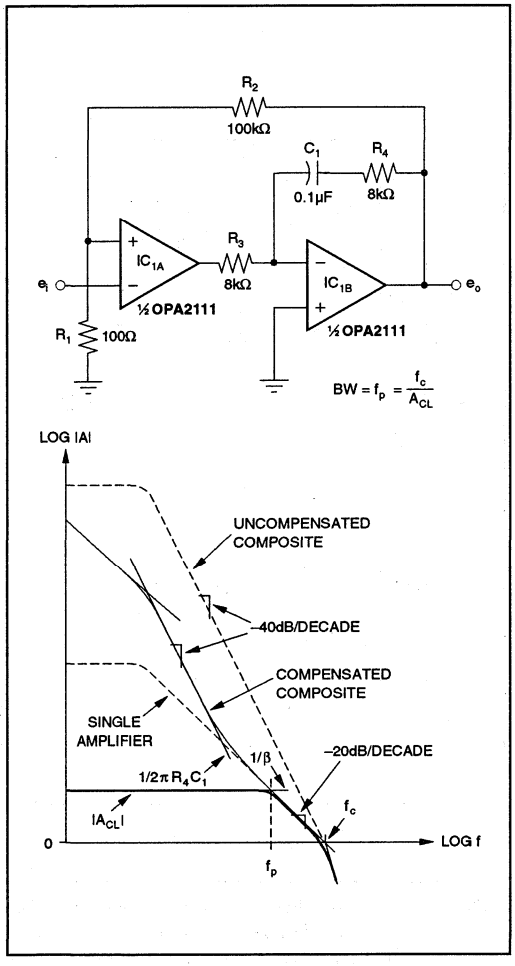


FIGURE 8. To utilize the boosted gain of the composite amplifier, traditional phase-compensation techniques tailor the gain-magnitude slope to obtain a stable region with a 1/β intercept.

An integrator and a common op amp test loop can demonstrate the benefits of using a composite amplifier. By extending the composite open-loop gain to higher levels, you can expand the dynamic range for integrating analog functions. The low-frequency intercept moves back by a factor equal to the added amplifier gain. This change is so extreme that other error effects will surface well before the gain error from the intercepts. For two op amps in the same loop each having 100dB open-loop gain, the composite gain is 200dB. At this gain level, an input error of 1nV will develop the full 10V output swing. Long before the circuit reaches that limit, noise becomes a prime AC constraint and typically restrains lower-level accuracy over a dynamic range of about 3,000,000:1. Nevertheless, this restraint is a 30:1 improvement over a single op amp and moves the focus of measurement accuracy to other factors.

In the op amp test-loop application[4], the addition of the second amplifier removes signal swing from the output of the tested device. The extra gain transfers that voltage swing to an isolated output and removes any gain error from the signal detected at the tested amplifier's inputs. This gain-error removal permits the discernment of other input-error signals for the measurement of parameters such as power-supply and common-mode rejection. If these parameters were to approach the level of the amplifier's open-loop gain, gain-error signals at the input would cloud the effects of the measured parameter.

PHASE COMPENSATION FOR THE COMPOSITE AMPLIFIER

With a composite op amp structure, you must include the roll-off characteristics of both amplifiers in your AC analysis and have some means of providing phase compensation for the loop. Two op amps in a common loop invite oscillation; the individual amplifier poles combine for a composite 2-pole roll-off. As shown in Figure 8, the logarithmic scale makes the initial composite-response curve the linear sum of the two individual responses. The upper, dashed response curve, which has a –40dB/decade slope, shows this result.

Two methods are available for compensating the composite loop. One modifies the gain-magnitude response and the other alters the 1/β curve. The more usual of the two approaches is to reduce the slope of the gain-magnitude curve in the vicinity of the intercept, as Figure 8 does. After forcing the compensated response to roll off earlier, the gain-magnitude curve returns with a more gentle slope to the boundary of the uncompensated response. This action serves the general-purpose requirements of voltage-gain applications and produces a stable range that you can place almost anywhere in the total composite-gain range.

Figure 8 achieves this compensation by creating a modified integrator response for IC_{1B}. Because this integrator is an inverting circuit, the inputs of IC_{1A} are reversed to retain only one phase inversion in the loop. Capacitor C_1 blocks the local DC feedback, and the overall gain is still the product of the two open-loop gains. The integrator response that R_3 and C_1 established for IC_{1B} rolls off this composite gain. Next, the first open-loop pole of IC_{1A} returns the compensated response slope to –40dB/decade. At a higher frequency, a response zero provides the region of reduced slope thanks to the inclusion of R_4. Above the break frequency of R_4 and C_1, R_4 transforms the response of IC_{1B} from an integrator to an inverting amplifier with a gain of $-R_4/R_3$.

Where this gain is unity, the compensated response drops to and follows the open-loop response of IC_{1A} as shown. For gain levels other than unity, you have different options, which you can explore by using other response plots and defining the particular stable conditions you have in mind.

Having control of this gain becomes particularly useful as the 1/β intercept approaches the uncompensated unity-gain crossover point. In this region, the second poles of the two op amps increase the phase shift. In such cases, you have to make the magnitude of the internal R_4/R_3 gain less than unity to force the compensated response to cross over earlier. Generally, when you have two op amps of the same type, making $R_4 = R_3/3$ will yield a unity-gain stable composite amplifier.

The net phase correction that you can achieve with this technique depends on the frequency-response range for which you maintain the –20dB/decade slope. This span begins with the R_4C_1 break frequency and ends with the intercept of the composite open-loop response. After this intercept, the lack of open-loop gain returns the response to that of the uncompensated composite amplifier. To ensure a phase margin of 45° or more, you can use the guidance that the Bode phase approximation provides; the plot shows that this reduced slope region must last for three decades of frequency and must intercept the 1/β curve after running for at least a decade.

COMPOSITE AMPLIFIERS EXTEND BANDWIDTH

Although most engineers are familiar with this type of phase compensation, it is too restrictive of bandwidth at higher gains. For applications requiring higher gains, you can greatly extend the bandwidth and reduce the settling time by 40:1 by using a different phase-compensation technique. The general-purpose $R_4 = R_3$ case of Figure 8 sets a constant closed-loop gain-bandwidth product. Looking at the curves, you can see that the closed-loop bandwidth is the same as that for IC_{1A} itself when $BW = f_p = f_c/A_{CL}$. Even so, the large separation between the compensated and uncompensated responses shows a significant sacrifice in bandwidth—expressly for the accommodation of phase compensation. Uncompensated, the gain-magnitude response has a gain-bandwidth product that increases with closed-loop gain and that provides a potential bandwidth of $f_p = f_c/\sqrt{A_{CL}}$. Comparing the last two expressions shows that the potential for bandwidth improvement equals $\sqrt{A_{CL}}$, which is significant at higher gains.

COMPENSATE THE 1/β CURVE

You can take advantage of quite a bit of this bandwidth-improvement opportunity by compensating the 1/β curve instead of the gain-magnitude response curve. By referring back to the rate-of-closure stability criteria discussed previously, you would see that both curves contribute to the rate-of-closure parameter even though the gain-magnitude curve is generally the focus of phase-compensation efforts. To satisfy the rate-of-closure criteria, all that is necessary is to control the difference between the slopes, regardless of the slopes of the individual curves. So, instead of reducing the gain-magnitude slope, increase the 1/β slope (Figure 9). A simple capacitive bypass of feedback resistor R_2 accomplishes this slope increase for a final 20dB/decade rate-of-closure.

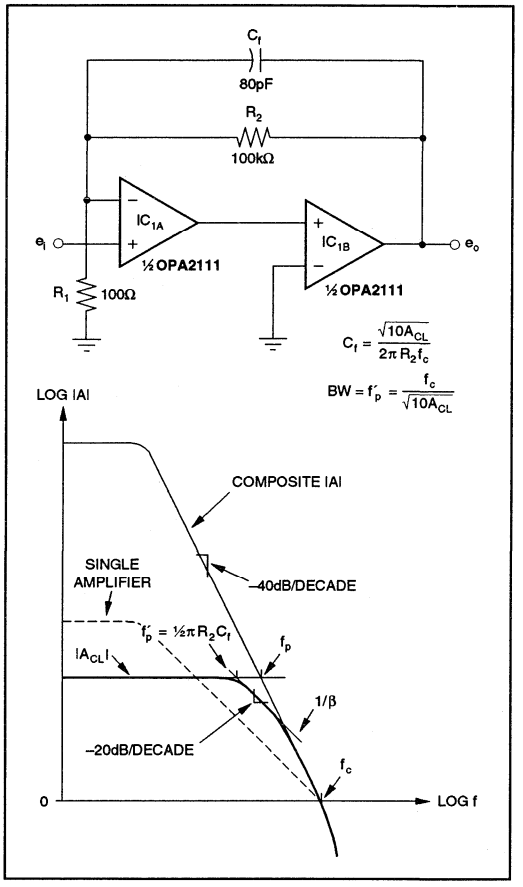


FIGURE 9. For greater bandwidth in high-gain circuits, you can provide phase compensation for the 1/β response to retain a smooth open-loop response for fast settling.

An integrator configuration, on the other hand, with its special characteristics, inherently produces the –20dB/decade slope for 1/β and achieves optimum bandwidth and dynamic range.

Two factors distinguish this feedback-factor compensation technique for higher gains. Greater bandwidth is open for reclaiming, and the associated 1/β curves are well above the unity-gain axis. From higher levels, the 1/β roll-off is developed well before its intercept with the gain-magnitude curve. Starting this roll-off a decade ahead of the final intercept produces a 45° phase adjustment for a like amount of phase margin. The slopes of the two curves show that, in order to accomplish this phase adjustment, C_f must break with R_2 one-half decade below the initial intercept frequency, f_p. Then, the 2:1 difference in slopes will place the new intercept one-half decade above f_p for the required full decade of the 1/β roll-off.

CHOOSING C_F FOR THE COMPOSITE AMPLIFIER

Again, the design equations for the required value of C_f and the resulting bandwidth are obvious from the logarithmic nature of the frequency axis. Setting f_p' at one-half decade below f_p implies that

$$\text{Log } f_p' = (\text{Log } f_p + \text{Log } f_p/10)/2$$

for which $f_p' = f_p/\sqrt{10}$. From before, you'll remember that $f_p = f_c/\sqrt{A_{CL}}$ describes the uncompensated curve's bandwidth. The compensated bandwidth is

$$BW = f_p' = f_c/\sqrt{(10A_{CL})}$$

Here, f_c is the unity-gain crossover frequency of the composite gain-magnitude response. As becomes obvious when you examine this expression, the improved bandwidth falls short of the total potential by $\sqrt{10}$. However, it is better than the Figure 8 result by $\sqrt{(A_{CL}/10)}$, or a factor of 10, for a gain of 1000. Setting C_f to break with R_2 at f_p' defines the value of this capacitor as

$$C_f = \sqrt{(10A_{CL})/2\pi R_2 f_c}$$

For the op amps of the dual OPA2111 shown, the gain-of-1000 bandwidth becomes 20kHz as compared with the 2kHz you'd realize if you used just one of the op amps.

COMPOSITE COMPENSATION EFFECTS

Settling time also improves when you choose the composite amplifier's 1/β curve for phase compensation. The improvement is a result of both the increased bandwidth and the retained constant gain-magnitude slope. For a single amplifier of the OPA2111 type, for a gain of 1000, the settling time would be 700µs to 0.01%. Because the Figure 9 amplifier has 10 times the bandwidth of a single amplifier, the settling time drops by the same factor to 70µs. This improvement would not be possible without the smooth and continuous slope of the compensated-amplifier response. A response having an intermediate pole and zero, such as Figure 8 does, has low-frequency response terms that are slow to settle following a transient. Known as an integrating frequency doublet, this pole/zero combination is notorious for its poor settling time[5]. By providing phase compensation for the 1/β curve, you ensure that the smooth gain-magnitude curve is left undisturbed, therefore achieving the optimum settling time.

At lower gains, the benefit of the 1/β compensation technique diminishes as does its control of phase. Because lower gains have 1/β curves closer to the unity-gain axis, they have less room for 1/β roll-off. To produce an intercept with the gain-magnitude curve after a decade of 1/β roll-off requires a minimum closed-loop gain of 10. Op amp phase shifts impose further limits by growing from 90° to 135° as they approach the unity-gain crossover frequency. In the practical case, this phase-compensation method needs gains of 30 or more for good stability.

This type of phase compensation does have an unusual aspect: Too great a compensating capacitance will have a surprising effect. Whereas increasing such capacitance normally yields more damping and a more stable response, making C_f too large will cause instability. As C_f increases, the resulting intercept moves toward f_c and encounters the added phase shift of the secondary-amplifier poles. Even greater values of C_f will drop the 1/β curve to its limit at the unity-gain axis. From there, it proceeds along the axis to the magnitude-curve intercept that guarantees oscillation. Only a range of compensation-capacitor values provides stability with this second approach; the 1/β curves display this range for sensitivity-analysis purposes. Because of the capacitor's window of stable values, a random selection of C_f followed by a stability test is likely to miss the bandwidth opportunity of this technique.

PHASE ONLY MATTERS AT THE INTERCEPT

Another concept fundamental to op amp feedback in composite-amplifier circuits becomes apparent when you examine phase shift and stability. Composite amplifiers such as the one in Figure 10 produce a –40dB/decade slope over wide ranges both before and after the 1/β intercept. Because this slope corresponds to a 180° phase shift, frequent concern over stability conditions arises at points other than that of the critical intercept. Beyond the 1/β intercept, the loop gain is less than 1 and therefore it is easy to see that the circuit cannot sustain oscillation. Yet, prior to the intercept, the gain of the feedback loop is very high and would seem capable of causing the circuit to oscillate.

In reality, the high loop gain is a protection against, rather than a promoter of, oscillation. Sustained oscillation depends on the op amp's gain-error signal. In Figure 10, the gain error, e_o/A, appears between the op amp inputs and receives amplification from the closed-loop gain, A_{CL}. Here, A_{CL} is that of the noninverting configuration, the noise gain that reacts with any input-referred error signal. To sustain oscillation, the amplified error signal must independently deliver the output signal. This action requires that $(-e_o/A)A_{CL} = e_o$. Note that e_o appears on both sides of this equation; it should therefore be obvious that any solution must conform to very specific constraints. This equation expresses both polarity and magnitude constraints; the composite amplifier's 180° phase shift satisfies the sign change.

For the magnitude constraint, two possible solutions exist. The first is $e_o = 0$, which is the stable state for the composite amplifier in the questioned region. There, the loop gain makes the signal e_o/A too small to independently support an output signal. In the plots of Figure 10, e_o/A starts at a very low level due to the high loop gain at low frequencies. As you move up in frequency, the gain-error signal rises while the amplifier-response slope signals its polarity inversion through the 180° phase shift. This inversion increases the output signal but cannot sustain it until the gain-error signal reaches a sufficient level. This critical level is a prerequisite for oscillation.

This level applies to the second solution for the magnitude constraint. At this level, A/A_{CL} has unity magnitude and maintains the balance for the previous feedback equation's magnitude requirement. Unity loop gain occurs at the 1/β

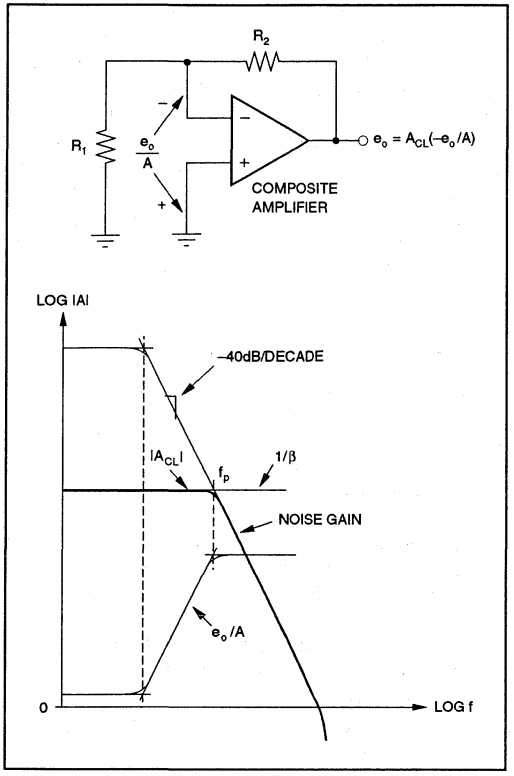


FIGURE 10. A phase shift of 180° causes oscillation only where the gain-error, e_o/A, is capable of independently supporting the output signal.

intercept where the open-loop and noise-gain curves meet. Without phase-compensation intervention, this intercept satisfies both the phase and magnitude requirements for oscillation. Beyond this point, e_o and A fall off together, leaving the e_o/A signal constant and unable to support oscillation with the reduced gain. At the point where the magnitude of the gain error and the feedback phase shift must both reach specific levels to support oscillation, the intercept becomes critical. Before or after the intercept, the loop phase shift can be at any level and the gain-error magnitude will not be sufficient to cause instability.

Unfortunately, despite the composite amplifier's very specific requirements for oscillation, the greatly varied applications of op amps make this critical condition all to easy to encounter. To contend with this problem, you can rely on the 1/β curve to present a visual prediction of the problem and provide insight into a solution.

ACTIVE FEEDBACK VARIES 1/ß

Some applications demand that you include a second active element in the feedback loop to produce a varying feedback factor. In these applications, both the magnitude and the

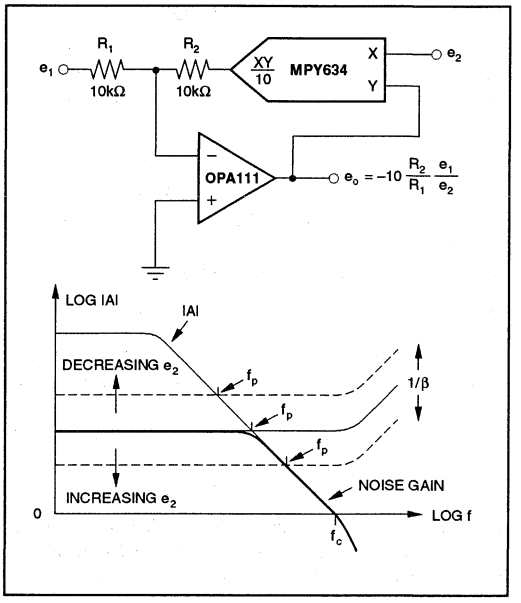


FIGURE 11. For this common analog divider, a variable feedback magnitude allows a range of conditions that define bandwidth and stability.

frequency characteristics of 1/β become variables. Fortunately, the gain- and feedback-response curves offer a means of quickly evaluating the range of conditions resulting from the changing feedback.

The most common way to provide magnitude variation in the feedback factor is to use a low-cost analog divider realization. Placing a multiplier in the feedback loop of an op amp (Figure 11) makes feedback a function of a second signal and therefore produces divider operation. With signal dependent feedback, the bandwidth and stability conditions also become variables.

Figure 11 shows the divider connection[6] and demonstrates the effect of voltage-controlled feedback on 1/β. The amplifier's feedback inverts the function of the multiplier by placing the feedback signal under the control of the e_2 signal. Then, the multiplier's transfer function of XY/10 delivers $e_o(e_2/10)$ to R_2. This action scales the feedback signal by comparing e_2 to 10V reference level to obtain

$$\beta = (e_2/10)\ R_1/(R_1 + R_2)$$

With the feedback factor under control of this signal, the 1/β curve moves across the full range of the gain-magnitude response. As e_2 nears zero, the 1/β curve approaches infinity, leaving the op amp essentially in an open-loop configuration. At the other extreme, a full-scale 10V value for e_2 delivers a feedback signal to R_2 that equals e_o almost as if the multiplier were not present. Then, the net response is that of a simple inverting amplifier with a feedback factor of $R_1/(R_1 + R_2)$ and an inverting gain of $-R_2/R_1$.

INTERCEPT VARIES WITH 1/ß

Between the extremes, the variation of e_2 moves the 1/β curve from as low as the unity-gain axis to above the upper reaches of the amplifier's gain-magnitude curve. This variation moves the critical intercept and requires attention to the rate-of-closure over the entire span of the gain-magnitude response. If no significant multiplier phase shift exists, the feedback will always resemble that of an inverting amplifier for a zero 1/β slope, and you can ensure stability by just using a unity-gain-stable op amp. You can then read the range of bandwidth for the divider operation directly from the moving 1/β intercept. For a given e_2 range, the intercept moves linearly with the signal, defining the corresponding bandwidth range.

The multiplier also introduces phase shift that alters the net phase shift around the feedback loop. Poles in the response of the multiplier circuit are zeros in the inverse 1/β function, causing the curve to rise at high frequencies. This rise moves toward the critical intercept when the multiplier control voltage, e_2, increases. This rise has an impact on the rate-of-closure, and the op amp must introduce a dominant pole to maintain stability. For the components shown, the OPA111 dominates the circuit roll-off because of its 2MHz unity-gain crossover frequency. This frequency is well below the 10MHz bandwidth of the MPY634 multiplier, placing the op amp in control. Other options that use a separate feedback path to restrict the op amp bandwidth are also available[3].

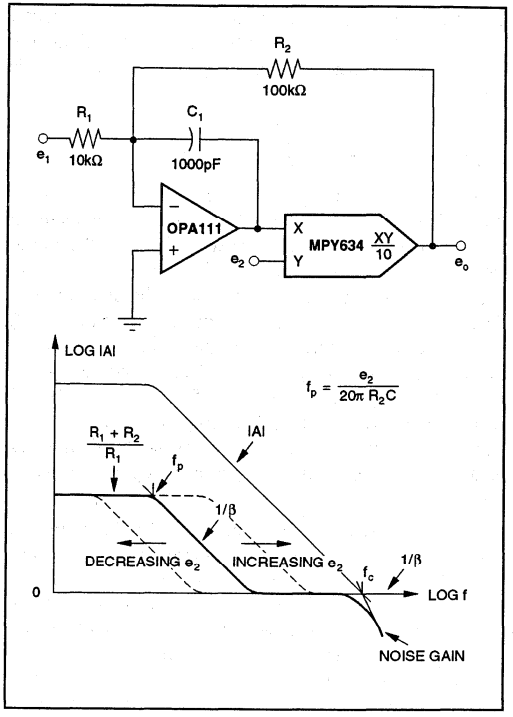


FIGURE 12. In this filter circuit, variations in the frequency characteristic of 1/β make possible a changing 1/β slope at the intercept.

VARIABLE 1/ß FREQUENCY RESPONSES

Other ways of providing variable feedback are also available. For example, you can have the signal control the frequency-rather than the magnitude-characteristics of the feedback. The result is a variable slope at the intercept, as is the case with the voltage-controlled lowpass filter in Figure 12. The basic elements of the lowpass filter are the op amp, the resistors, and the capacitor. If you replace the multiplier with a short circuit, these elements form a fixed-frequency roll-off. Essentially, this shorted condition is established when e_2 = 10V and when the gain through the multiplier is unity. Capacitor C_1 then breaks with R_2 to define the filter roll-off just as if the resistor and capacitor were directly in parallel.

For levels of e_2 below full scale, the multiplier serves as a voltage-controlled attenuator to effectively alter the filter time constant. Attenuating the feedback voltage to R_2 lowers the signal current to the summing node, which has the same effect as increasing the resistor's value. Increased effective resistance corresponds to a decrease in the resistor's break frequency with C_1. This break defines the variable filter roll-off when $f_p = e_2/20\pi R_2 C_1$

The maneuvering of the 1/β curve through this operation deserves closer inspection. The circuit exhibits a signal-dependent transition between the two different loops, which alternately control the feedback. At low frequencies, C_1 is effectively an open circuit, and the controlling feedback path is through the op amp and the multiplier. This composite structure has resistive feedback that defines a signal gain of $-R_2/R_1$ and a noise gain of $(R_1 + R_2)/R_1$. The latter relationship equals 1/β at low frequencies and the curve of interest starts at this level with a zero slope. At the high-frequency end, the composite structure is overridden when C_1 acts as a short circuit, which results in a unity feedback factor around the op amp. This short circuit absorbs all feedback current from R_2 without any corresponding change in the amplifier output voltage. The feedback loop of the composite structure is then disabled, switching feedback control to just the op amp. With C_1 then providing a unity feedback factor to the op amp, the 1/β curve follows the unity-gain axis at high frequencies.

Once the 1/β levels are fixed at the extremes, the multiplier determines the nature of the transition between the two. In the transition region, feedback currents from R_2 and C_1 compete for control of the summing node of the op amp input. The contest for dominance is analogous to the frequency-dependent control of impedance with a parallel RC circuit. In both cases, the 3dB point, where each element carries the same magnitude of current, defines the transition of control. The Figure 12 filter achieves equal element currents when the impedance of C_1 and the effective impedance of R_2 are equal. This equality defines the voltage-

controlled roll-off frequency of the filter as previously expressed. At this frequency, 1/β also rolls off and drops at –20dB/decade to the high-frequency limit of the unity-gain axis.

RATE-OF-CLOSURE VARIES WITH 1/ß

The stability conditions of the Figure 12 circuit depend on the particular feedback loop or the combination of elements that are in control at the intercept point. For the lower-frequency filter cutoff frequencies illustrated, the op amp's bypass capacitor takes control before the intercept and defines the relevant feedback conditions. Because the 1/β curve follows the unity axis at the upper end, you can guarantee stability by ensuring that the op amp be unity-gain stable. For higher-frequency cutoff frequencies, the 1/β transition moves toward the gain-magnitude curve of the op amp. Circuit response cannot move beyond this limit, so the op amp roll-off becomes the upper boundary of filter operation.

When the cutoff frequency approaches this boundary, the intercept rate-of-closure varies, prompting stability analysis. First, the zero of the 1/β curve approaches the intercept, where it increases the slope of the curve. Because this action reduces the rate-of-closure, stability is improved and a more detailed analysis is unnecessary. A continued increase in the cutoff frequency moves the 1/β curve further to the right where its pole interacts at the intercept. This break frequency returns the rate-of-closure to 20dB/decade, thus retaining stability. Beyond this point, the intercept occurs at the flat lower end of the 1/β curve, and no further change in the rate-of-closure takes place.

Utilizing these various feedback conditions and a unity-gain-stable op amp, you can design a composite circuit that fulfills its primary stability requirement over the entire operating range. In addition, however, you may sometimes require a multiplier having a bandwidth much greater than that of the op amp, as the two previous examples demonstrate. Without a wide-bandwidth multiplier, 1/β would begin to rise near the higher-frequency intercepts and increase the rate-of-closure. The OPA111 avoids this complication when using the MPY634 multiplier by maintaining a dominant op amp pole.

Other applications may involve feedback peaking and op amps that are not unity-gain stable-log amps and active filters, for example. For these and other variations requiring feedback analysis, the test remains the same. Look for the critical condition where the rate-of-closure is 40dB/decade. Where conditions approach this level, conduct further analysis and compare phase-compensation alternatives for optimization.

REFERENCES

1. Tobey, G. E., Graeme, J. G., and Huelsman, L. P., *Operational Amplifiers: Design and Applications,* McGraw-Hill, 1971.

2. Bower, J. L., and Schultheis, P. M., *Introduction to the Design of Servomechanisms,* Wiley, 1961.

3. Stitt, R. M., and Burt, R. E., "Möglichkeiten zur Rauschunter-druckung," *Elektronik,* December 1987, pg 112.

4. Lewis, E. D., "Compensation of Linear IC Test Loops," *Electronics Test,* May, 1979, pg 83.

5. Dostal, E. J., *Operational Amplifiers,* Elsevier Scientific Publishing, Amsterdam, Holland, 1981.

6. Wong, Y. J., and Ott, W. E., *Function Circuits: Design and Applications,* McGraw-Hill, New York, NY, 1976.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

BURR-BROWN® APPLICATION BULLETIN

Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

FEEDBACK CIRCUIT CLAMPS PRECISELY

by Jerald Graeme, (602) 746-7412

A limiter circuit consisting of an input buffer (A_1), an output-scaling amplifier (A_2), two zener diodes (Z_1 and Z_2), and several other components can supply sharp, precise, bipolar clamp levels with continuous variable control, from 0 to ±11V. See Figure 1. A feedback loop enclosing the amplifiers and zeners generates the high clamping accuracy.

Within the limit range of the clamp ($\pm V_L$), the zener diodes are off, and A_2 feeds back its output to the inverting input of A_1 through R_4. At the same time A_1 drives A_2 through the voltage divider R_V. The feedback forces the inverting input of op amp A_1 to equal E_I at the noninverting input terminal.

The circuit forces the inverting input of A_2 also to follow E_I. There's no signal voltage drop across R_4, because no current can flow from it into A_2's inverting input. Consequently, the noninverting input of A_2, which defines the potentiometer output at feedback equilibrium, must also track E_I. A resistor voltage divider can replace the control potentiometer R_V in fixed-level limiting applications.

Amplifier A_2 then delivers an output:

$$E_O = (1 + R_3/R_2)\, E_I$$

when

$$-V_L < E_O < V_L$$

and

$$V_L = x\,[(1 + R_3/R_2)]\,(V_Z + V_F)$$

where x is the setting fraction of R_V, and V_Z and V_F are the zener and forward voltages, respectively. The overall circuit response, then, is simply that of a voltage amplifier when the output signal is within the limit boundaries.

Amplifier A_1 generates small deviations from an ideal response because A_2's circuit gain $(1 + R_3/R_2)$ amplifies any offset voltage and noise from A_1. Similarly, this loop gain mitigates the clamping error by sharpening its clamping response. The zener drive increases during the transition to the clamping state.

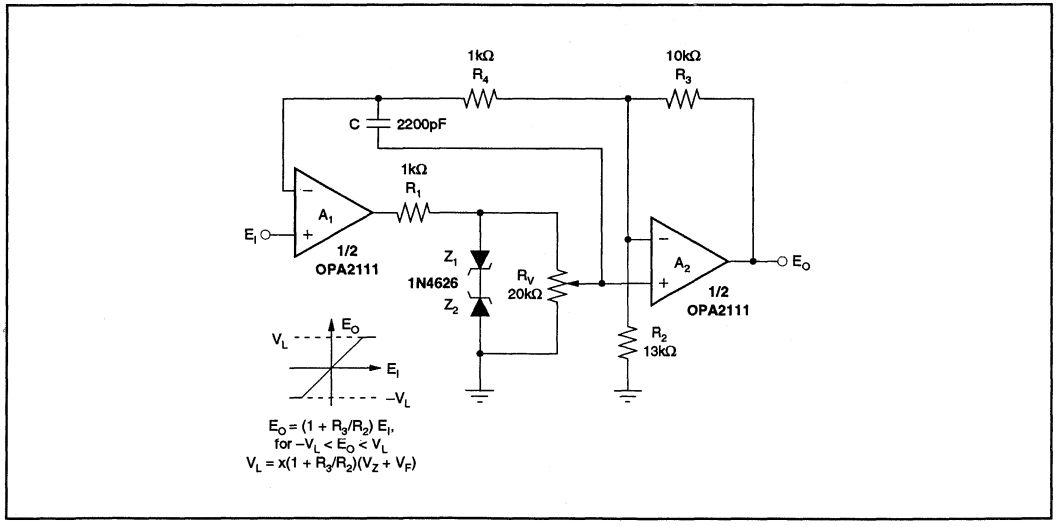


FIGURE 1. Amplifier A_1 Buffers and Amplifier A_2 Scales Input Signals Under Feedback Control. Zener diodes and a potentiometer or voltage divider in the feedback loop supply a continuously variable bipolar-clamping limit.

In the clamping mode, when the voltage across the two zeners reaches $\pm(V_Z + V_F)$, the circuit goes from acting as a voltage amplifier to acting as a voltage reference; the voltage across R_V is fixed and the potentiometer output is $\pm x(V_Z + V_F)$. Further increase in the magnitude of the signal at E_I can't change this potentiometer value until it drops below the limit point V_L.

Thus, clamping is no longer limited to the fixed levels of available zener voltages. Even clamping levels as low as 5mV become practical when offset-trimmable OPA111 op amps replace the OPA2111. However, available zener voltages and the closed-loop gain of A_2 set the maximum clamping level.

Use of 10 –V zeners and a gain of one for A_2 can cover the voltage range of most analog-signal processing. Unfortunately, the voltage temperature coefficients of 10 –V zeners would produce thermal drift in the clamping level. With 5.6 –V zeners, however, the temperature coefficients of the zener and forward voltages tend to cancel. For such zener diodes $V_Z + V_F = 6.2V$, and the net drift is near zero. Then, with A_2 set to a gain of 1.77, the maximum limit voltage V_L is 11V.

The 5% tolerances of the zener voltages determine the basic accuracy of the clamp levels. The gain-setting resistors R_2 and R_3 impose additional tolerance error. However, adjusting the gain with these resistors can compensate for any zener-voltage error and resistor tolerances. With matched zeners, the adjustment can readily reduce the clamp-level errors to less than 1%. Without matching, the 5% error of simple zener clamping prevails, but the circuit still clamps sharply.

For frequency stability, resistor R_4 and capacitor C supply a frequency roll-off in A_1. At high frequencies, the capacitor shorts the output of A_1 to its inverting input. Then A_1 and A_2 operate with independent feedback loops, and the overall circuit requires stability in the individual amplifiers.

BURR-BROWN® APPLICATION BULLETIN

Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

OP AMP PERFORMANCE ANALYSIS

By Jerald Graeme (602) 746-7412

Given the numerous specifications describing op amp performance, the above title suggests an ambitious goal for one bulletin. Yet, this bulletin reflects the analysis power gained through knowledge of an op amp circuit's feedback factor. Feedback dictates the performance of an op amp both in function and in quality. The major specifications of the amplifier describe an open-loop device awaiting feedback direction of the end circuit's function. Just how well the amplifier performs the function reflects through the feedback interaction with the open-loop error specifications. Fortunately, most open-loop errors simply reflect to the circuit output amplified by the reciprocal of the circuit's feedback factor.

Amplifier bandwidth limits this simple relationship but the feedback factor defines this limit as well. Above a certain frequency, the amplifier lacks sufficient gain to continue amplification of signal and errors alike. Graphical analysis defines this frequency limit through plots representing available amplifier gain and the feedback demand for that gain. This same analysis indicates frequency stability characteristics for op amp circuits. Just the slopes of the plots indicate the phase shift in the feedback loop. Thus, the feedback factor of an op amp circuit is a powerful performance indicator.

The determination of a circuit's feedback factor depends upon feedback modelling. The basic feedback model of an op amp applies directly to the noninverting circuit configuration. Using this configuration, this treatment demonstrates the performance, feedback and stability concepts common to all op amp configurations. A simple guideline extends feedback factor determination to most other op amp circuits. Just knowing a circuit's feedback factor extends the concepts and conclusions of this bulletin to these other op amp configurations.

FEEDBACK FACTOR DEFINES PERFORMANCE

More than any other parameter, the feedback factor of an op amp application defines the circuit performance.[1] Feedback factor sets the gain received by the input-referred errors of the amplifier. These open-loop errors include offset voltage, noise and the error signals generated by limitations in open-loop gain, common-mode rejection and power-supply rejection. In addition, a circuit's feedback factor determines bandwidth and frequency stability.

For the noninverting op amp configuration, a convenient relationship between closed-loop gain and feedback factor simplifies performance analysis. There, the gain of the application circuit itself sets the amplification of input-referred errors and determines the circuit bandwidth. Shown in Figure 1 as a voltage amplifier, this noninverting circuit produces the familiar, ideal closed-loop gain of $A_{CLi} = (R_1 + R_2)/R_1$. This gain amplifies both the input signal e_i and the differential input error e_{id} of the op amp. Simply multiplying e_{id} by A_{CLi} defines the resulting output error. Later examination adds frequency dependence to this simple relationship.

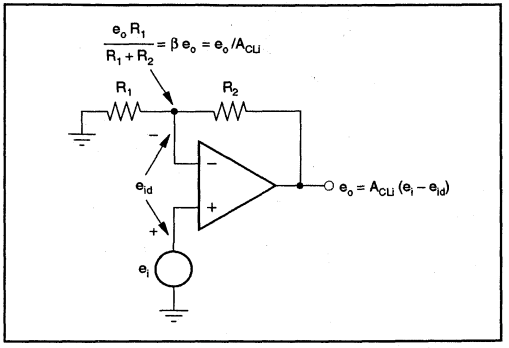


FIGURE 1. Noninverting op amp connections amplify input signal e_i and error signal e_{id} by a gain of $A_{CLi} = 1/\beta$.

The fundamental mechanism relating input and output errors lies in the feedback factor. Feedback factor is the fraction of the amplifier output signal fed back to the amplifier input. In the figure, a feedback voltage divider defines this fraction through the output to input transfer response

$$\beta e_o = \frac{e_o R_1}{R_1 + R_2}$$

This defines β as simply the voltage divider ratio, $R_1/(R_1 + R_2)$. Comparison of this result with A_{CLi} shows that $A_{CLi} = 1/\beta$ for the noninverting case.

Other op amp circuit configurations produce different A_{CLi} but β remains the same. As a general guideline, the feedback factor of an op amp circuit equals the voltage divider ratio of the feedback network. This fact extends the results developed below with the noninverting circuit to almost all other op amp circuits. Just determining this voltage divider ratio for a circuit defines the β term common to a broad range of performance results. In rare cases, complex feedback defies this simple guideline, requiring detailed feedback modelling.[1]

General error analysis depends on β rather than A_{CLi} as emphasized with the model of Figure 2. This model represents the noninverting op amp connection by an amplifier with input error signal e_{id} and with feedback transmission factor β. This feedback factor determines the signal βe_o fed back to the amplifier input from the output signal e_o. Writing a loop equation for the model shows that

$$e_o = (1/\beta)(e_i - e_{id})$$

In this result, a gain of 1/β amplifies both e_i and e_i. Thus, the Figure 1 circuit and Figure 2 model agree for purposes of input-to-output transmission of amplifier signals.

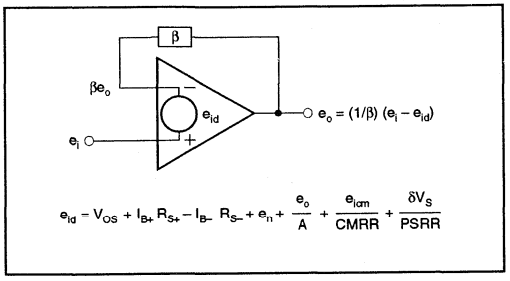


FIGURE 2. The input error amplified by 1/β, e_{id}, includes the effects of the major performance characteristics of an op amp.

INPUT-REFERRED ERRORS SUMMARIZE PERFORMANCE

The simple 1/β relationship between input and output errors predicts the output errors resulting from almost all amplifier performance characteristics. Each of these characteristics produces an input-referred error source for the op amp as combined in

$$e_{id} = V_{OS} + I_{B+} R_S + I_{B-} R_{S-} + e_n + e_o/A + e_{icm}/CMRR + \delta V_S/PSRR$$

Error terms included here cover the effects of the op amp input offset voltage, input bias currents, input noise voltage, open-loop gain, common-mode rejection and power-supply rejection. Here, the second and third terms of the e_{id} equation include the source resistances presented to the two amplifier inputs. The last three error terms include circuit signals which are the output voltage, the common-mode voltage and the power supply voltage change.

The input-referred representations of the individual error terms generally follow from the definitions of the associated performance characteristics. Definitions directly classify V_{OS}, I_{B+}, I_{B-} and e_n as input error sources. Open-loop gain is simply a ratio of output voltage to differential input voltage. Dividing the output voltage by the gain defines the associated input signal as e_o/A. The amplifier's finite open-loop gain requires this input error signal to support the output signal. Similarly, power-supply rejection ratio equals the ratio of a power supply change to the resulting change in differential input voltage. Thus, PSRR = $\delta V_S/\delta e_{id}$ and the associated input-referred error is $\delta e_{id} = \delta V_S/PSRR$.

For CMRR, the relationship between definition and input error requires closer examination. Common-mode rejection ratio is defined as the ratio of the differential gain to the common-mode gain, A_D/A_{CM}. For an op amp, the differential gain is simply the open-loop gain A. Then, CMRR = A/A_{CM} and rewriting this shows the common-mode gain to be A_{CM} = A/CMRR. However, by definition $A_{CM} = e_{ocm}/e_{icm}$ where e_{ocm} is the output signal resulting from e_{icm}. Combining the two A_{CM} equations results in $e_{ocm} = Ae_{icm}/CMRR$. To support this component of output voltage, the op amp develops another gain error signal in e_{id}. As before, the resulting e_{id} component equals the associated output voltage divided by the open-loop gain. Dividing the preceding e_{ocm} expression by open-loop gain A defines the input-referred CMRR error as $e_{icm}/CMRR$.

Closer examination also clarifies the source resistances, R_{S+} and R_{S-}, of the e_{id} equation. In the simplest case, a source resistance is just the output resistance of a signal source that drives a circuit input. For op amp circuits, scaling and feedback resistances alter the net resistances presented to the amplifier's inputs. The difference amplifier connection well illustrates this as shown in Figure 3. There, scaling resistors R_3 and R_4 alter the resistance presented to the amplifier's noninverting input and feedback resistors R_1 and R_2 alter that presented to the inverting input.

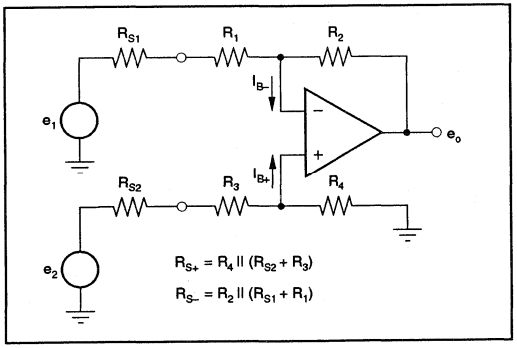


FIGURE 3. Scaling and feedback resistors alter the source resistances presented to the input bias currents of an op amp.

Signal sources e_1 and e_2 drive the difference amplifier's inputs through conventional source resistances R_{S1} and R_{S2}. However, the scaling and feedback resistances alter the net resistances presented to the op amp's input currents I_{B+} and I_{B-}. Current I_{B+} divides between two paths to ground through R_4 and the $R_3 + R_{S2}$ combination. Here, the $R_3 + R_{S2}$ path returns to ground through the low resistance of the e_2 source. Thus, for the e_{id} equation, $R_{S+} = R_4 \| (R_3 + R_{S2})$. Analogously, I_{B-} divides between the path through R_2 and that through $R_1 + R_{S1}$. In this case, R_2 departs from the analogy by returning

to the op amp output instead of to ground. However, the low output impedance of the op amp produces an equivalent result for this resistance evaluation. Thus, $R_{S-} = R_2 \parallel (R_1 + R_{S1})$.

Together, the error terms of the Figure 2 model provide a fairly complete representation of op amp performance limits. However, the e_{id} expression does not specifically list errors due to distortion, bandwidth and slew rate limiting. Actually, e_{id} includes the amplifier's distortion error in the gain and CMRR error signals.[2] A circuit's bandwidth limit restricts the effects of the e_{id} error sources at higher frequencies. Slew rate limiting simply imposes a secondary bandwidth limit for large signal operation. Feedback factor analysis treats the bandwidth limiting of error effects later.

Up to the circuit's bandwidth limit, each input-referred error term of the Figure 2 model reflects to the amplifier output through a gain equal to $1/\beta$. Multiplication of the error terms by $1/\beta$ produces some familiar results. Output error due to the finite open-loop gain becomes $e_o/A\beta$. This shows that error due to open-loop gain reduces the output e_o by a fraction of that output. This fraction equals the reciprocal of the loop gain $A\beta$. The decline of A with frequency makes this error rise and this shapes the closed-loop frequency response of the circuit. Similar multiplication of the input noise error defines the output noise as e_n/β, leading to the term "noise gain" for $1/\beta$. This description of $1/\beta$ only holds under the bandwidth limits to be described. For both the loop gain and noise errors, greater visibility results through the frequency response analysis described below. Similarly, the frequency dependencies of CMRR and PSRR reflect to the circuit output with circuit-specific bandwidths.

FEEDBACK MODELLING DEFINES CLOSED-LOOP RESPONSE

The above discussion presents the $1/\beta$ relationship between input-referred op amp error sources and the resulting output errors. However, the frequency dependance of amplifier gain modifies this simple, initial relationship. Amplifier response roll off defines a bandwidth limit for both signal and error sources. This reduces the output error effect of all error sources except for the DC errors V_{OS}, I_{B+} R_{S+} and I_B R_{S-}. Amplifier gain, noise, CMRR and PSRR produce AC errors and their output effects depend on the circuit's frequency response. More complete feedback modelling defines this frequency response through the noninverting amplifier example. However, the frequency response results developed here extend to any op amp configuration through a standardized response denominator.

Figure 4 shows the generalized noninverting connection with the feedback network as the generalized Z_1 and Z_2 rather than the resistors shown before. Redrawing the amplifier configuration as shown highlights the voltage divider action of the feedback network. The network's divider action again displays the fraction of the amplifier output fed back to the amplifier input. In preparation for the next modelling step, the figure reduces the amplifier input error signal, e_{id}, to just the open-loop gain error e_o/A. Feedback modelling focuses on gain and related frequency characteristics. Still, this one error signal suffices to define frequency response for use with the previous multi-error analysis.

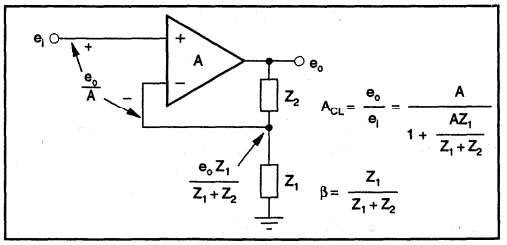


FIGURE 4. Redrawing the op amp circuit and reducing e_{id} to the gain error signal, e_o/A, prepares the circuit for feedback modelling.

Loop analysis defines the noninverting circuit's transfer response as

$$A_{CL} = \frac{e_o}{e_i} = \frac{A}{1 + \frac{AZ_1}{Z_1 + Z_2}}$$

Gain A in this expression contains the frequency dependence that shapes the circuit's frequency response. Note that the denominator of this response contains the feedback factor $Z_1/(Z_1 + Z_2)$. This makes the denominator $1 + A\beta$ and this relates the circuit to the model presented next.

To more completely model the noninverting circuit, Figure 5 replaces the op amp of Figure 4 with a gain block and a summation element. Also, a feedback block replaces the feedback network from before. The gain block represents the amplifier open-loop gain and the summation models the differential action of the op amp inputs. Op amp open-loop gain amplifies the differential signal between the two amplifier inputs. Opposite polarities at the model's summation inputs reproduce the differential action in the summation. Here, the polarity assignments match the polarities of the corresponding op amp inputs. With these assignments, the summation extracts the differential signal through subtraction. The model then supplies the differential signal to the gain block and this block drives the feedback block β. For op amps, this classic feedback model, initially developed by Black[3], only represents the noninverting case. Modifications to the model adapt it to other configurations.[1] However, the noninverting case here suffices to define performance conditions common to all op amp configurations.

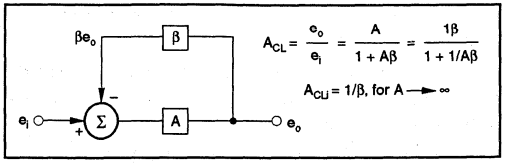


FIGURE 5. Black's classic feedback model reproduces the A_{CL} transfer response of the noninverting op amp configuration.

Comparison of circuit and model responses demonstrates the model validity. The model amplifies the difference between the summation inputs by gain A to produce the output signal. This results in $e_o = A(e_i - \beta e_o)$ and solving for e_o/e_i defines the modelled transfer response as

$$A_{CL} = \frac{e_o}{e_i} = \frac{A}{1 + A\beta}$$

Comparison of terms in the A_{CL} equations for the model, above, and the circuit, before, shows the feedback factor to be $\beta = Z_1/(Z_1 + Z_2)$, validating the model.

LOOP GAIN SUSTAINS RESPONSE

Further analysis of the A_{CL} result defines the op amp frequency response and stability conditions.[4] This added performance information depends upon the denominator of the A_{CL} response and not upon the noninverting case considered here. Conclusions based upon this denominator extend to all other op amp configurations. Rewriting the A_{CL} equation for the noninverting case yields

$$A_{CL} = \frac{1/\beta}{1 + 1/A\beta}$$

Then, the response numerator expresses the ideal closed-loop gain, $A_{CLi} = 1/\beta$, and the denominator expresses the frequency dependance in through A and β.

Other op amp configurations produce different numerators, but always with the same $1 + 1/A\beta$ denominator. This common denominator unifies bandwidth and stability characteristics for all op amp configurations. All op amp configurations produce a closed-loop response of

$$A_{CL} = \frac{A_{CLi}}{1 + 1/A\beta}$$

Writing a given configuration's response in this form immediately identifies the ideal response, A_{CLi}, as the numerator. It also directly links the configuration to the denominator-based bandwidth results and stability criteria that follow.

The frequency dependencies of A and β combine to set a configuration's frequency response. At low frequencies, the high level of open-loop gain A reduces the denominator above to $1 + 1/A\beta \approx 1$. Then, the circuit response simplifies to the ideal gain of A_{CLi}. At higher frequencies, the op amp open-loop gain drops, causing this denominator to increase. Then, A_{CL} declines from it's ideal value A_{CLi}. Similarly, a high-frequency drop in β would add to the A_{CL} decline. Initially, a constant β simplifies the analysis. Constant β results with the resistive feedback networks common to the majority of applications.

The open-loop gain decline with frequency produces the circuit's bandwidth limit as illustrated in Figure 6. There, the resistive feedback case illustrates the most common condition. Reactive rather than resistive feedback slightly modifies the bandwidth conclusions developed here and a later example describes this effect. However, reactive feedback does not alter the frequency stability conditions developed through this resistive feedback example. The plot of the figure displays the frequency responses of all three variables in the A_{CL} equation. Shown are the closed-loop gain, A_{CL}, the open-loop gain, A_{OL}, and $1/\beta$ as a function of frequency. The graphical interaction of these variables provides visual insight into bandwidth and frequency stability limits. The heavier curve represents the resulting closed-loop response A_{CL}.

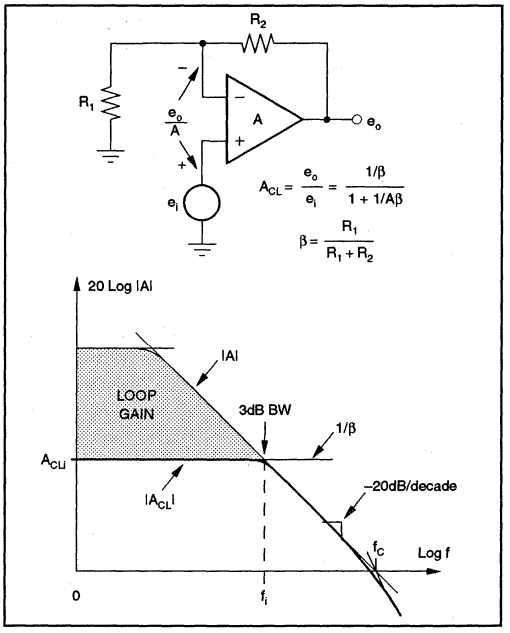


FIGURE 6. Graphical analysis with a circuit's A and $1/\beta$ curves defines the circuit's closed-loop bandwidth.

The loop gain of the circuit, $A\beta$ in the above denominator, represents the amplifier gain resource available to maintain the ideal closed-loop response. In Figure 6, the shaded area of the graph highlights this gain. At any given frequency, the corresponding loop gain equals the vertical distance between the A and $1/\beta$ curves. The logarithmic scale of the graph makes this distance $\log(A) - \log(1/\beta) = \log(A\beta)$. Loop gain $A\beta$ represents the amplifier's reserve capacity to supply the feedback demand for gain. Where loop gain drops below unity, the closed-loop curve drops from the ideal A_{CLi}.

The A and $1/\beta$ curves graphically display this loop gain limit. Here, the $1/\beta$ curve represents the feedback demand. Loop gain meets this demand as long as the $1/\beta$ curve remains below the open-loop gain curve. However, at higher frequencies, the open-loop gain curve falls below the $1/\beta$ level. There, feedback demand exceeds the available amplifier gain and A_{CL} rolls off, following the amplifier open-loop response. This response roll off follows a –20 dB/decade slope for the single-pole response characteristic of typical op amps.

1/β INTERCEPT MARKS BANDWIDTH LIMIT

The bandwidth limit of most op amp circuits occurs at the 1/β intercept with the open-loop gain curve. Some circuits reduce bandwidth further, through reactive feedback elements, but all op amp circuits encounter a bandwidth limit at the 1/β intercept. Figure 6 illustrates this intercept and the coincident roll off of the A_{CL} response. By definition, the 3dB bandwidth limit occurs where A_{CL} drops from its DC value to 0.707 times that value. Analysis shows that this condition results at the intersection of the A and 1/β curves. These curves are actually magnitude responses and, at their intersection, their magnitudes are the same or $|A| = |1/\beta|$. Rearranging this result shows that the intercept occurs where the loop gain is $|A\beta| = 1$ at the frequency f_i. A phase shift of –90° accompanies this unity gain magnitude because of the single-pole roll off of gain A. Then, $A\beta = -j1$, at the intercept, and the denominator of the A_{CL} equation becomes $1 + 1/A\beta = 1 + j1$.

The $\sqrt{2}$ magnitude of this denominator drops circuit gain from A_{CLi} to $0.707A_{CLi}$. Thus, for frequency independent feedback factors, the 3 dB bandwidth occurs at the intercept frequency f_i. With frequency dependent feedback factors, the closed-loop response still rolls off following the intercept but this point may not be the 3dB bandwidth limit. Then, peaking or additional roll off in the closed-loop response curve moves the actual 3dB point away from f_i.

For the more common op amp applications, constant feedback factors permit a simple equation for the 3dB bandwidth. Single-pole responses characterize the open-loop roll offs of most op amps and virtually all 1/β intercepts occur in this single-pole range. There, the single-pole makes the gain magnitude simply $|A| = f_C/f$ where f_C is the unity-gain crossover frequency of the amplifier. Then, at the intercept, $f = f_i$ and $A = 1/\beta = f_C/f_i$. Solving for f_i defines the 3dB bandwidth for most op amp applications as

$$BW = f_i = \beta f_C$$

This result holds for all op amp applications having frequency independent β and single-pole op amp roll off.

Technically, the above bandwidth limit portrays only the small-signal performance of an op amp. In large-signal applications, slew rate limiting often sets a lesser bandwidth limit, especially in lower gain applications. There, the slew rate limit, S_r, imposes a power bandwidth limit of $BW_P = S_r/2\pi E_{op}$ where E_{op} is the peak value of the output voltage swing. This limit represents the only major performance characteristic of an op amp not directly related to the feedback factor β.

However, an indirect relationship still links large-signal bandwidth and β. The value of β helps determine which bandwidth limit, BW or BW_P above, applies in a given application. Both bandwidth limits set performance boundaries and the lower of the two prevails in large-signal applications. Higher values of β imply lower closed-loop gains and increase the frequency boundary set by $BW = \beta f_C$. There, $BW_P = S_r/2\pi E_{op}$ generally produces the lower of the two boundaries, controlling the circuit bandwidth. Conversely, lower values of β reduce the $BW = \beta f_C$ boundary, making this the dominant limit. For a given application, compare the two limits to determine which applies.

BANDWIDTH ALSO RESTRICTS ERROR SIGNALS

The frequency dependence defined by the 1/β intercept also applies to the AC error sources of the previous Figure 2 analysis. That analysis showed that the input-referred errors of op amps transfer to the amplifier output through a gain of 1/β. However, 1/β does not include the high frequency limitations of the amplifier. Thus, the earlier analysis remains valid only for frequencies up to the 1/β intercept at f_i. Above this frequency, the amplifier lacks sufficient gain to amplify input error sources by a gain of 1/β. The bandwidth limit $BW = \beta f_C$ marks a response roll off that reduces amplification of signal and error alike. Beyond this BW limit, the gain available to error signals rolls off with the amplifier open-loop response. Here, the limited error signal magnitudes always invoke the small-signal, rather than slew-rate, bandwidth limit.

This error signal roll off produces the previously mentioned difference between 1/β and "noise gain". Beyond the intercept, the gain supplied to noise follows the amplifier response roll off even though the 1/β curve continues uninterrupted. For A_{CL}, the response roll off results from the denominator of this gain's equation. For error signal gain, adding this denominator to the original 1/β gain inserts the frequency dependance. This makes the closed-loop error gain

$$A_{CLe} = \frac{1/\beta}{1 + 1/A\beta}$$

Here, the added frequency dependance reduces the higher-frequency output errors calculated for the noise, CMRR and PSRR error sources.

For the noninverting case considered here, $A_{CLe} = A_{CL}$ but, for other cases, A_{CL} varies. Error gain A_{CLe}, however, remains the same. This gain always equals 1/β up to this curve's intercept with the amplifier open-loop response. Then, A_{CLe} rolls off with that response. Note that A_{CLe} above depends only upon the variables β and A. Any feedback model with β and A blocks configured like Figure 5 yields the same expression for A_{CLe}.

1/β INTERCEPT ALSO DEFINES STABILITY

The AC performance indications of the feedback factor also predict op amp frequency stability. The response plots that define bandwidth also communicate the phase shift of the feedback loop. Excess phase shift promotes response ringing or oscillation and the plot slopes indicate this phase shift directly. Mathematical analysis defines the stability indicators applied to the plots and an intuitive evaluation verifies these indicators.

Response plots like that of Figure 6 permit frequency stability evaluation directly from the curve slopes. Specifically, the slopes of the A and 1/β curves at the intercept indicate phase shift for a critical feedback condition. As mentioned, the intercept corresponds to a loop gain magnitude of $|A\beta| = 1$. If the loop phase shift reaches 180°, the loop gain at the intercept becomes $A\beta = -1$. Then, the denominator of A_{CL} equation reduces to $1 + 1/A\beta = 0$ making A_{CL} infinite. With infinite gain, a circuit supports an output signal in the absence of an input signal. In other words, the circuit oscillates and it does so at the intercept frequency f_i.

The relative slopes of the gain magnitude and 1/β curves reflect the phase shift of the feedback loop. The relationship between response slope and phase shift follows from the basic effects of response poles and zeros. A pole creates a –20dB/decade response slope and –90° of phase shift and a zero produces the same effects with opposite polarities. Additional poles and zeroes simply add response slope and phase shift in increments of the same magnitudes. The slope and phase correlation accurately predicts the loop phase shift when the critical intercept remains well separated from response break frequencies. Within a frequency decade of the intercept, any break frequency of the amplifier or feedback network requires the more detailed analysis described later. However, even in these cases, the response slopes provide insight into probable stability behavior.

Relying on the slope and phase correlation, the rate-of-closure guideline quickly approximates the phase shift of Aβ. Rate-of-closure is simply the difference between the slopes of the A and 1/β curves at the intercept. Both slopes communicate phase shift and the slope difference indicates the net phase shift of the loop. Figure 7 illustrates the slope and phase correspondence for two common feedback cases. There, two 1/β curves having different slopes intercept the gain magnitude curve |A|. The $1/\beta_1$ curve has the zero slope of resistive feedback networks and the rate-of-closure depends only upon the gain magnitude curve. This curve has the –20dB/decade slope common to most op amps. Together, the two curves develop a 20dB/decade slope difference, or rate-of-closure, for 90° of Aβ phase shift.

In the feedback loop, the phase inversion of the op amp adds another 180° for a net phase shift of 270°. This leaves a phase margin of $\Phi_m = 90°$ from the 360° needed to support oscillation. For op amp stability analysis, the 180° phase shift from the amplifier phase inversion is automatic. Thus, op amp phase analysis simplifies, replacing the normal 360° stability criteria with a criteria of 180° of feedback phase shift. This convention applies in the examples that follow.

The second 1/β curve of Figure 7 illustrates the feedback condition of the basic differentiator circuit. This circuit produces a feedback demand curve represented in the figure by $1/\beta_2$. That curve slopes upward at +20dB/decade and intercepts the |A| curve where the slope difference is 40dB/decade. Then, the rate-of-closure guideline indicates a feedback phase shift of 180°, leaving zero phase margin. This explains the inherent oscillation of the basic differentiator circuit.

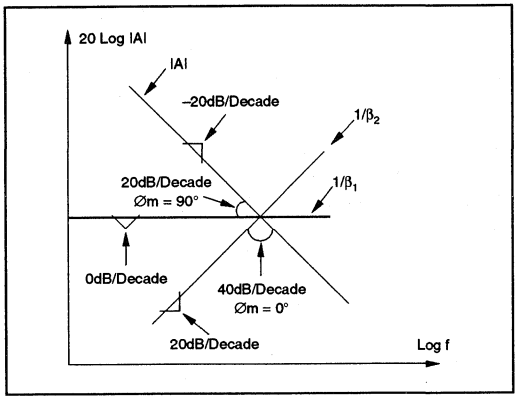


FIGURE 7. Plotted together, the 1/β and open-loop gain curves display a circuit's frequency stability conditions through the curves' rate-of-closure.

APPROXIMATION SIMPLIFIES PHASE ANALYSIS

As mentioned, the rate-of-closure criteria accurately predicts the Aβ phase shift when no response break frequencies occur within a decade of the intercept. Other cases require more detailed phase analysis but this too simplifies with the Bode phase approximation.[5] This approximation produces a maximum error of 5.7°. Shown in Figure 8, this approximation predicts the phase effect of a response singularity through a straight line approximation. The actual phase shift introduced by the illustrated pole at f_p progresses through the arctangent curve shown. The actual phase shift at any frequency can be calculated from $\Phi = \text{Arctan}(f/f_p)$.

However, the Bode approximation provides quicker, visual feedback when examining response plots. This approximation simplifies the phase shift curve to a straight line having a slope of –45°/decade. This line centers on the frequency f_p, where the phase shift is 45°. From there, the approximation line predicts 0° at $0.1f_p$ and the full 90° at $10f_p$. Just these three reference points provide a quick visual indication of the effect a given response break produces at a frequency of

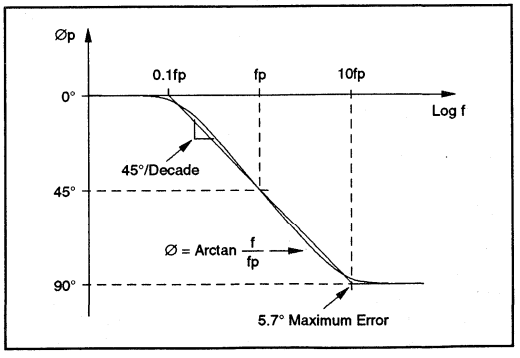


FIGURE 8. The Bode phase approximation refines phase analysis for cases where the rate-of-closure criteria looses accuracy.

interest. Outside the band of $0.1f_p$ to $10f_p$, a response break produces little influence. Near f_p, the response break introduces around 45° of phase shift.

In between these reference points, visual extrapolation approximates the phase shift. For example, consider a point midway between the f_p and $10f_p$ marks of the Log f scale. Note that this midpoint is a linear measure on the log scale. This requires no logarithmic conversion and visual perception of distance applies directly. At this midpoint, the phase approximation indicates a phase shift of approximately 45° + 0.5(45°) = 67.5°. Similarly, at a point two-tenths of the way between $0.1f_p$ and f_p the approximation indicates 0.2 (45°) = 9°. These analyses require no knowledge of the actual frequencies represented by the example points. In contrast, exact analysis with the arctangent relationship first requires conversion of the linear distance observed into the equivalent frequency of the log f scale. Then, the arctangent relationship must be calculated.

Figure 9 illustrates the application of the Bode phase approximation to the stability indication of the 1/β intercept. In the figure, the intercept occurs where the open-loop gain response has a slope of –20dB/decade. The rate-of-closure guideline suggests 90° of loop phase shift. However, a second amplifier pole at f_p develops a –40dB/decade slope in the open-loop gain response. As shown, the pole at f_p occurs less than a decade from the intercept. This limited separation compromises the simple rate-of-closure indication.

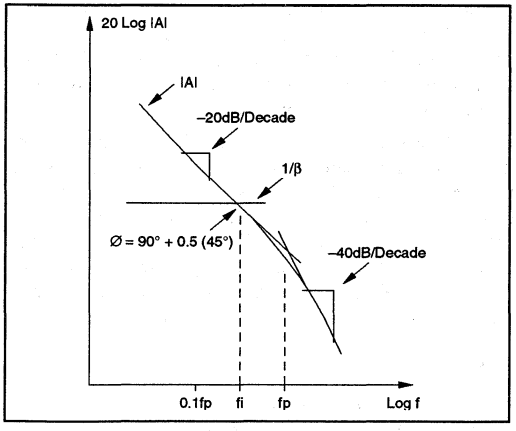


FIGURE 9. Application of the Bode approximation defines the phase effects of response breaks that occur less than a decade from the intercept at f_i.

Then, the Bode phase approximation estimates the phase effect of f_p at the intercept f_i. As shown, f_i occurs below f_p so the effect is less than 45°. Refinement of this initial estimate follows from the linear distance separating f_p and f_i on the plot. This linear distance represents a fraction of a frequency decade. The fraction equals this distance divided by the linear distance between f_p and $0.1f_p$. Visual reading of the example shown places f_i about midway between f_p and $0.1f_p$. This communicates a phase effect from f_p of 0.5(45°) = 22.5° at the intercept frequency f_i. Adding this to the 90° produced by the –20db/decade gain slope results in a net loop phase shift of 112.5°. This leaves 67.5° of phase margin from the 180° of feedback phase shift required for oscillation.

INTUITIVE ANALYSIS EXPLAINS OSCILLATION

With op amps, conventional insight into the cause of amplifier oscillation can be misleading. In the general amplifier case, high gain combined with high phase shift promotes oscillation. In the op amp case, these conditions often exist together without producing instability. The distinction lies in the simultaneous gain and phase conditions required for op amp oscillation. At lower frequencies, high loop gain prevents oscillation by attenuating the amplifier's input error signal. At higher frequencies, lack of loop gain restricts the output signal to similarly prevent oscillation. In between, the loop gain reaches a point where the high and low frequency limitations cross, satisfying the gain condition for oscillation. Still, the feedback phase shift at this crossover must reach 180° to produce oscillation.

To illustrate this gain and phase combination, Figure 10 demonstrates the basic requirements for op amp oscillation. This figure grounds the normal signal input of the circuit to remove the effect of any applied signal upon the output voltage. With the grounded input, only the gain error signal, $-e_o/A$, excites the input circuit. This signal must independently produce the output signal in order to sustain an oscillation. The circuit amplifies the gain error signal by the closed-loop gain A_{CL}, producing $e_o = A_{CL}(-e_o/A)$. In turn, this output signal reflects back through the amplifier, producing the attenuated input signal $-e_o/A$. If this circuit gain and attenuation cycle supports an output signal, it is self-sustaining oscillation.

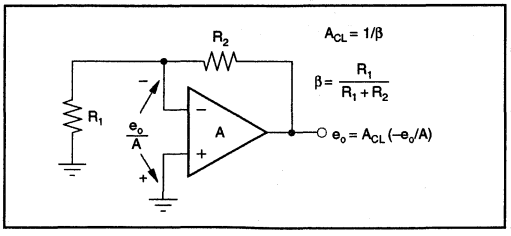


FIGURE 10. To sustain oscillation, error signal e_o/A and gain A_{CL} must support the output voltage in the absence of an applied input signal.

At lower frequencies, $A_{CL} = 1/\beta$, making the oscillation condition $e_o = -e_o/A\beta$. To sustain oscillation, the circuit must satisfy this equality and only two solutions do, $e_o = 0$ and $A\beta = -1$. The $e_o = 0$ solution indicates an oscillation of zero amplitude, representing the stable state. The $A\beta = -1$ solution represents the actual oscillation state, as noted in the previous mathematical analysis. This second solution places very specific magnitude and phase requirements upon the

loop gain Aβ. The condition Aβ = –1 requires that |Aβ| = 1 in combination with 180° of phase shift for the minus sign.

Consider the magnitude requirement first. If |Aβ| is too large, the circuit conditions would require $|e_o| > |e_o/A\beta|$. This condition can not be self sustaining. Here, the attenuated input error signal e_o/A, when amplified by a gain of 1/β, remains too small to support the required e_o. Only when the attenuating gain, A, equals the amplifying gain, 1/β, does the circuit meet the magnitude condition for oscillation. Expressing this in an equation, |A| = |1/β|, repeats the previous mathematically derived condition for oscillation. Only at the intercept of the A and 1/β curves do their magnitudes become equal. Only then does the circuit fill the magnitude condition for oscillation.

At this intercept, oscillation also requires 180° of feedback phase shift. If Aβ lacks 180° of phase shift, then the minus sign of the Aβ = –1 condition remains unsatisfied, preventing oscillation. Further, oscillation only results when this phase condition coincides with the magnitude condition above. An Aβ phase shift of 180° at frequencies other than the intercept frequency does not produce oscillation. At those other frequencies, the circuit fails to meet the magnitude condition for oscillation.

Composite amplifiers permit a graphical illustration of this combined oscillation requirement. These amplifiers inherently produce the 180° phase shift required for the minus sign. They consist of two op amps connected in series and each amplifier contributes a –20dB/decade slope to the composite open-loop gain. This produces a –40dB/decade gain slope as illustrated by Figure 11. This slope indicates 180° of phase shift over most of the amplifier's useful frequency range. Thus, composite amplifiers meet the phase condition for oscillation over a broad range.

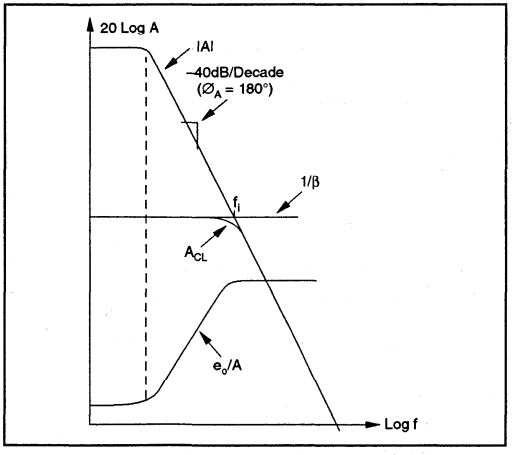


FIGURE 11. A composite amplifier response illustrates the fact that 180° of phase shift fails to support oscillation where e_o/A lacks sufficient magnitude.

Over the same frequency range, the composite amplifier provides high open-loop gain. This gain and phase combination might first suggest stability problems over the entire range. However, the high open-loop gain actually serves to stabilize the circuit through the circuit's loop gain. High values for A increase the loop gain Aβ to prevent the magnitude equality $|e_o| = |e_o/A\beta|$ required for oscillation. It does so by limiting the e_o/A error signal as illustrated in the figure. At lower frequencies, high levels of open-loop gain A reduce this input signal to a level insufficient to support oscillation.

The e_o/A curve rises as gain A declines but flattens when A_{CL} declines. The rise in e_o/A must reach a certain level to support the oscillation condition of $e_o = -A_{CL}(e_o/A)$. Also, to support this condition, the high-frequency roll off of A_{CL} must not excessively reduce this gain. Otherwise, the amplification of e_o/A by A_{CL} fails to develop sufficient e_o to sustain oscillation. Only one point in the plots satisfies this oscillation condition. As described before, where A = 1/β, e_o/A reaches the level required to support oscillation. This intercept also marks the peak value for $A_{CL}(e_o/A)$. Beyond there, A_{CL} rolls off with gain A, reducing e_o and leveling the e_o/A curve. With a level e_o/A curve, the A_{CL} roll off also rolls off the quantity $A_{CL}(e_o/A)$.

Before this intercept, e_o/A remains too small to support oscillation. After the intercept, the amplifier lacks the A_{CL} needed to sustain oscillation. Thus, before or after the intercept, 180° of feedback phase shift does not compromise stability. This phase shift produces oscillation only if present at the frequency of the intercept. There, gain magnitude conditions always permit oscillation given the required 180° phase condition. Phase compensation reduces this phase shift for the composite amplifier.

The 1/β intercept represents a critical mass point for frequency stability. There, the magnitude of the gain error and the feedback phase shift must both reach specific levels to support oscillation. Despite the very specific requirements for oscillation, the greatly varied applications of op amps make this critical mass condition all to easy to find. To contend with this, the 1/β curve presents visual prediction of the problem and provides insight into its solution.

REFERENCES

1. Graeme, J. G., *Feedback Models Reduce Op Amp Circuits to Voltage Dividers*, EDN, June 20, 1991, pg 139.

2. Graeme, J. G., *Op Amp Distortion Measurement Bypasses Test Equipment Limits*, EDN, February 17, 1992, pg 133.

3. Black, H., *Stabilized Feedback Amplifiers*, Bell System Technical Journal 13, 1/35.

4. Graeme, J. G., *Feedback Plots Offer Insight Into Operational Amplifiers*, EDN, January 19, 1989, pg 131.

5. Tobey, G. E., Graeme, J. G., Huelsman, L. P., *Operational Amplifiers; Design and Applications*, McGraw-Hill, 1971.

BURR-BROWN® APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

DOUBLE THE OUTPUT CURRENT TO A LOAD WITH THE DUAL OPA2604 AUDIO OP AMP

Headphones typically have an impedance of 40Ω to 300Ω. By using the dual OPA2604 and four resistors one can economically drive a 2.8V peak signal into the 40Ω headphones.

Figure 1 illustrates a circuit that can be used to drive loads that exceed the output current capabilities of an operational amplifier, but not enough to require the use of a power operational amplifier. The OPA2604 used in this application is a dual, FET-input operational amplifier that can typically sink or source 35mA on the output. By taking advantage of the fact that the OPA2604 is a dual, this circuit will sink or source 70mA. In addition, each operational amplifier has its own short circuit protection of ±40mA (typ), which makes the overall typical short circuit current of this application ±80mA.

One side of the dual OPA2604, A_2, is in the feedback loop of the other side of the dual, A_1. The current, I_1, which is supplied by A_1 is matched by the current I_2, the output current of A_2. The load will receive a total current of $I_1 + I_2$. The ratio between the output currents, I_1 and I_2, is equal to:

$$I_2 = I_1 \ (R_3/R_4)$$

Resistors R_3 and R_4 are set equal for equal output currents. Resistors R_1 and R_2 set the overall gain of the circuit. The transfer function is:

$$V_{OUT} = V_{IN} \ (1 + R_2/R_1)$$

The OPA2604 is a dual, FET-input operational amplifier designed for enhanced AC performance. Very low distortion, low noise and wide bandwidth provide superior performance in high quality audio applications. The OPA2604 is available is plastic 8-pin DIP and plastic 8-pin SOIC.

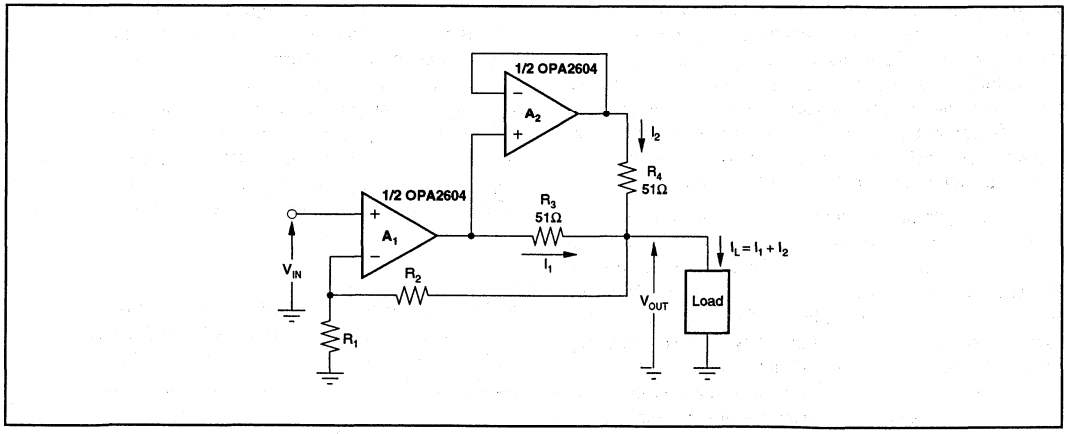


FIGURE 1. Using the Dual OPA2604 Op Amp to Double the Output Current to a Load.

BURR-BROWN® APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

A LOW NOISE, LOW DISTORTION DESIGN FOR ANTIALIASING AND ANTI-IMAGING FILTERS

Many customers have requested more information about the analog low-pass filters that appear in many of our PCM audio data sheets. They are used for antialiasing in front of ADCs or for smoothing on the output of DACs. The following bulletin is an excellent primer on the subject. —Ed.

In any digitizing system, antialiasing and anti-imaging filters are used to prevent the signal frequencies from "folding back" around the sample frequency and causing false (or alias) signals from appearing in the signal we are attempting to digitize. Very often, these filters must be very complex, high order analog filters in order to do their job effectively.

As sampling rates of converter systems have increased, however, oversampling may be used to reduce the filters' stopband attenuation requirements[1][2]. In digital audio systems, 4x oversampling may be used, and it can be shown[3] that for an antialiasing filter (which precedes the ADC), a simple sixth order filter may be used. For the output side, after the DAC, a simple third order filter may be used. Realizing these filters in a way that maintains extremely low noise and low distortion then becomes a challenge.

Compact disk player manufacturers began using a filter topology that was described many years ago—the Generalized Immittance Converter (GIC)[4]. This topology allows one to easily realize active filters beginning from a passive filter design. In addition, the GIC filter provides extremely low distortion and noise, at a reasonable cost. Compared with more familiar feedback filter techniques, such as Sallen & Key filter topologies, the GIC filter can be shown to have superior noise gain characteristics, making it particularly suitable for audio and DSP type applications[5].

We use this type of filter on our demonstration fixtures for the PCM1750 and PCM1700, dual 18-bit ADC and DAC, respectively. When sending out schematics of these demonstration fixtures, very often the first question is, "What are those filters anyway?" Well, they're GIC filters, and here's how you design them and how they perform. Stepping through this design process will allow you to modify these designs for a different cutoff frequency for your particular application. A more detailed treatment of the theory behind these filters may be found in Huelsman and Allen[6].

As stated above, for oversampling digital audio applications, third and sixth order filters are adequate. Thus, we may design our first GIC filter by designing a third order filter. The filter characteristic most desirable for sensitive DSP type applications is linear-phase. The linear-phase filter is sometimes called a Bessel (or Thomson) filter. The linear-phase filter has constant group delay. This means that the phase of the filter changes linearly with frequency, or that

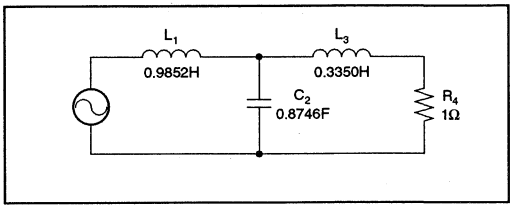


FIGURE 1. Passive Third Order, Linear-Phase, Low-Pass Filter Prototype.

the group delay is constant. These filters maintain phase information for sensitive DSP applications such as correlation, and preserve transient response. These characteristics are critical in audio applications as well, because they affect sound quality greatly.

Thus, we begin the design process by selecting a passive, third order linear-phase filter design that will be realized using this active approach. The passive design shown in Figure 1 is neither a Butterworth nor a Bessel response; it is something in between. The component values for this particular response, optimized for phase linearity and stopband attenuation, were found through exhaustive computer simulations and empirical analysis. Component values for standard Butterworth and Bessel responses may be found in standard filter tables, such as those available in Huelsman and Allen[7]. This circuit is then transformed to an active circuit by multiplying all circuit values by 1/s, which changes all inductors to resistors, all resistors to capacitors, and all capacitors to Frequency Dependent Negative Resistors (FDNRs). These FDNRs have the characteristic impedance of

$$\frac{1}{s^2C}$$

and may be realized using the GIC circuit. Thus, L_1 becomes R_1, C_2 becomes $1/s^2C_2$, L_3 becomes R_3, and the terminating resistor R_4 becomes C_4, as shown in Figure 2.

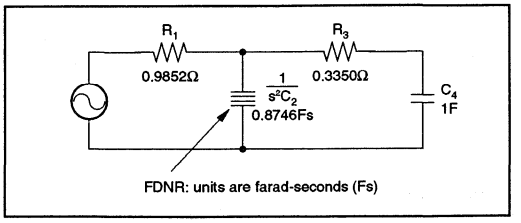


FIGURE 2. Filter of Figure 1 Transformed by Multiplying All Component Values by 1/s.

The FDNR is then realized by the GIC circuit shown in Figure 3. The value of the FDNR is determined by

$$D = (R_{12} \cdot R_{14} \cdot C_{13} \cdot C_{15})/R_{11}$$

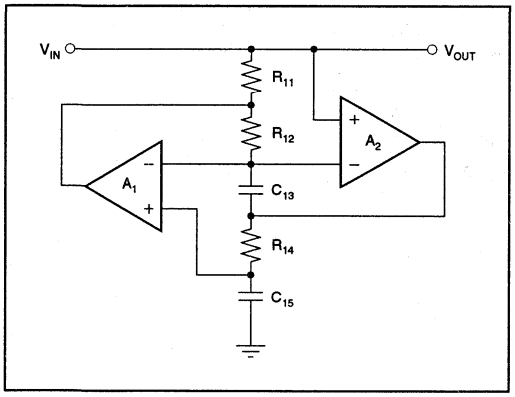


FIGURE 3. Frequency Dependent Negative Resistor (FDNR) Realized Using Generalized Immittance Converter (GIC).

Thus by setting $R_{11} = R_{12} = 1$ and $C_{13} = C_{15} = 1$, D is entirely determined by the value of R_{14}. For the FDNR of Figure 2, $R_{14} = 0.8746\Omega$.

The entire third order filter circuit is shown in Figure 4. This circuit now must be scaled in frequency to give the desired cutoff frequency, and then must be scaled in impedance to allow for the use of reasonable sized component values.

The filter circuits found in filter tables, such as that in Figure 1 and the active realization of this passive circuit (Figures 2 and 4), are designed for a cutoff frequency of $\omega = 1$ rad/s. To make the filter have the cutoff frequency we desire, we must scale it in frequency by the scaling factor

$$\Omega_N = 2\pi f_c$$

This scaling factor is applied to all frequency-determining components—capacitors in this case. The example filter will be designed for audio, so we might consider a cutoff frequency of 20kHz. However, linear-phase filters tend to roll-off very slowly, causing 1-2dB attenuation before the cutoff frequency; generally audio systems prefer to have their frequency response out to 20kHz to be within 0.1dB. The example filter then will have a cutoff frequency of 40kHz, commonly used in many of today's CD players. All capacitor values are divided by the frequency scaling factor, so $C_{13} = C_{15} = C_4 = 3.98\mu F$.

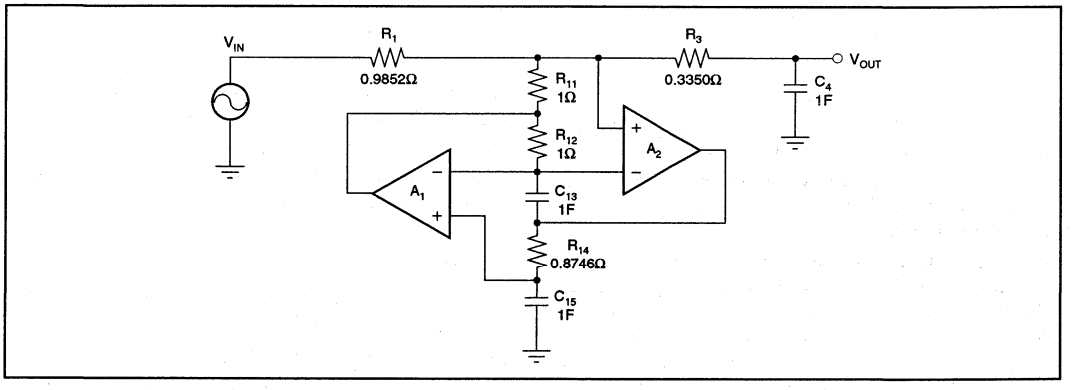


FIGURE 4. Third Order, Linear-Phase Realization of Circuit Shown in Figure 2.

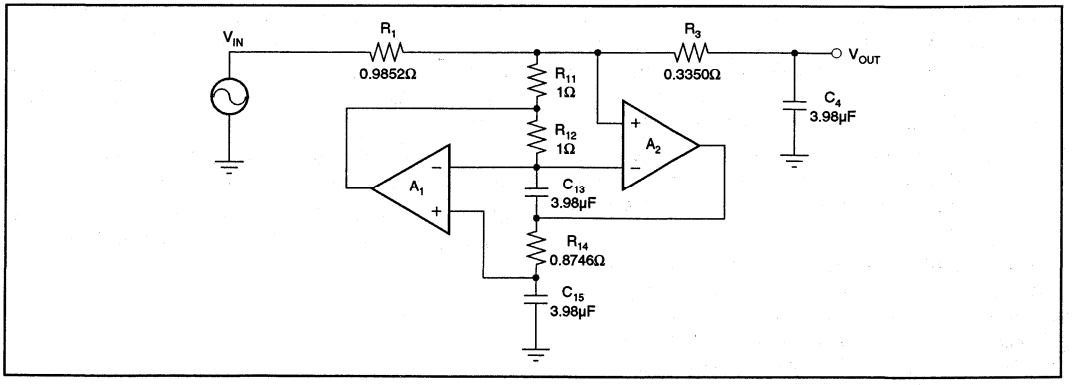


FIGURE 5. Circuit of Figure 4 Scaled to a 40kHz Cutoff Frequency.

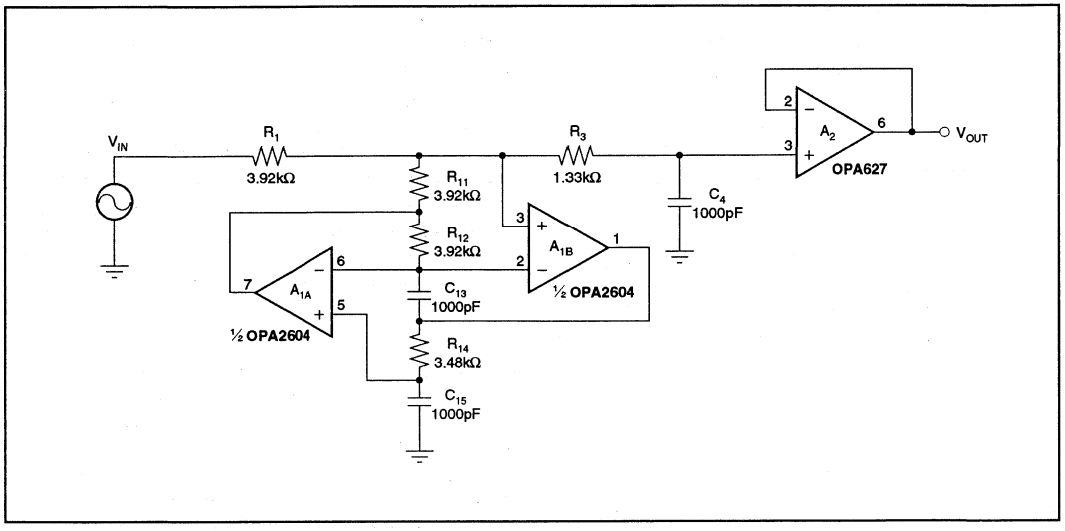


FIGURE 6. Circuit of Figure 5 Scaled in Impedance (note use of buffer amplifier to reduce output impedance of the filter).

The filter (Figure 5) could now be built, but the large capacitor values and low resistance values could pose practical problems. To alleviate this, the impedances of the circuit are scaled by an impedance scale factor:

$$Z_n = \frac{\text{Present C value}}{\text{Desired C value}}$$

By choosing the desired C value as 1000pF, $Z_n = 3.97 \times 10^3$. This impedance scaling factor then is multiplied by all resistor values to find the new resistor values, and divides all the capacitor values, taking them from the present values to the desired capacitance.

The final filter design is shown in Figure 6. Since the output impedance of this filter is relatively high, it's a good idea to buffer the output using an op amp voltage follower. Amplitude and phase response of this filter is shown in Figure 7a. Figure 7b is a closer look at the amplitude response in the passband—the frequency response is flat well within 0.1dB out to 20kHz.

Figure 7c is a plot of the frequency response of the filter (solid line) and the filter's deviation from linear phase (dotted line). Note the phase scale; the phase response is well within 0.1° of linear phase in the 1kHz-20kHz region, where the ear is most sensitive to phase distortion.

Figure 7d is a plot of the total harmonic distortion plus noise (THD + N) of this filter versus frequency. At about –108dB, this would be suitable for digital systems with true 18-bit converter performance!

To make a sixth order filter, you can repeat the design process above from a passive realization and directly implement a filter. This implementation is very sensitive to the gain-bandwidth product (GBW) match of all of the op amps used, however; for a 40kHz cutoff frequency, an op amp with extremely high GBW would be required. An example of a sixth order, 40kHz Butterworth filter realized in this fashion is shown in Figure 8, but its frequency response (Figure 9) is less than hoped for due to the GBW limitations described above.

A simpler solution is to cascade two of the third order sections designed above. This cascaded design (Figure 10) works equally well for most applications.

Figure 11 (a-d) shows the performance of this cascaded filter design. Note that the phase linearity and THD + N are still excellent using this approach.

REFERENCES

(1) R. Downs, "DSP Oversampling to Quiet Noise," *EE Times*, pg. 68, 8 August 1988.

(2) R. Downs, "High Speed A/D Converter Lets Users Reap Benefits of Oversampling," *Burr-Brown Update*, Vol. XIV, No. 2, pg. 3, May 1988.

(3) R. Downs, "Unique Topology Makes Simple, Low-Distortion Antialiasing Filters," to be published.

(4) S.K. Mitra, *Analysis and Synthesis of Linear Active Networks*, John Wiley & Sons, Inc., New York, pg. 494, 1969.

(5) R. Downs, "Unique Topology Makes Simple, Low-Distortion Antialiasing Filters," to be published.

(6) L.P. Huelsman, P.E. Allen, *Introduction to the Theory and Design of Active Filters*, McGraw-Hill, New York, 1980.

(7) Ibid.

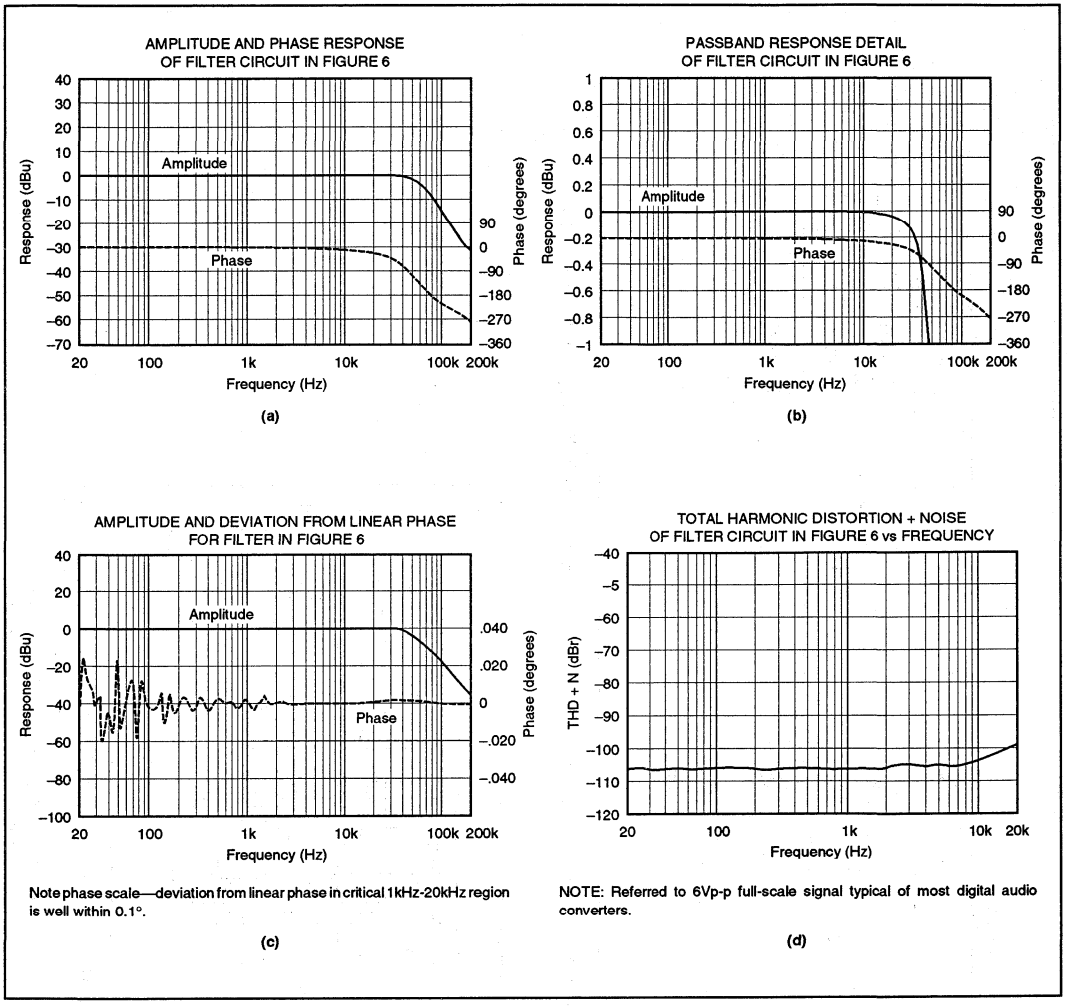


FIGURE 7. Performance Details of Figure 6 Circuit.

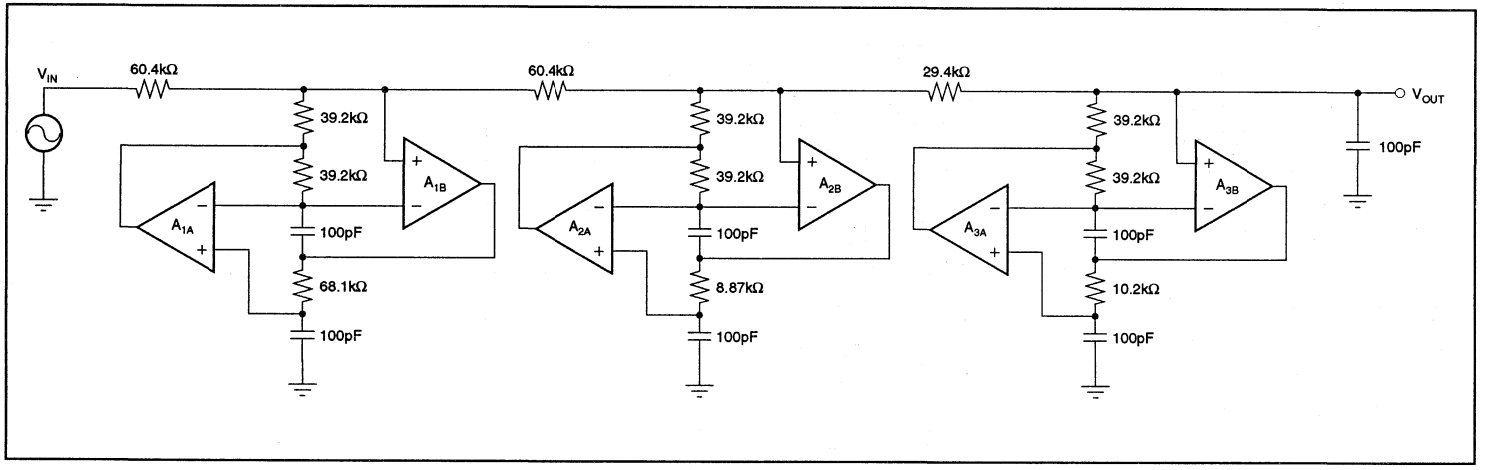


FIGURE 8. Sixth Order Butterworth Filter Realized by Method Outlined in Text (actual circuit would require output buffer amplifier to lower output impedance).

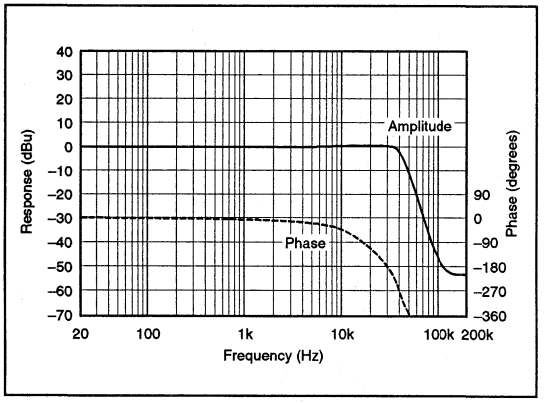


FIGURE 9. Amplitude (solid line) and Phase (dotted line) Response of Filter Circuit in Figure 8. (Note flattening of stopband response near 150kHz due to inadequate GBW of operational amplifiers used.)

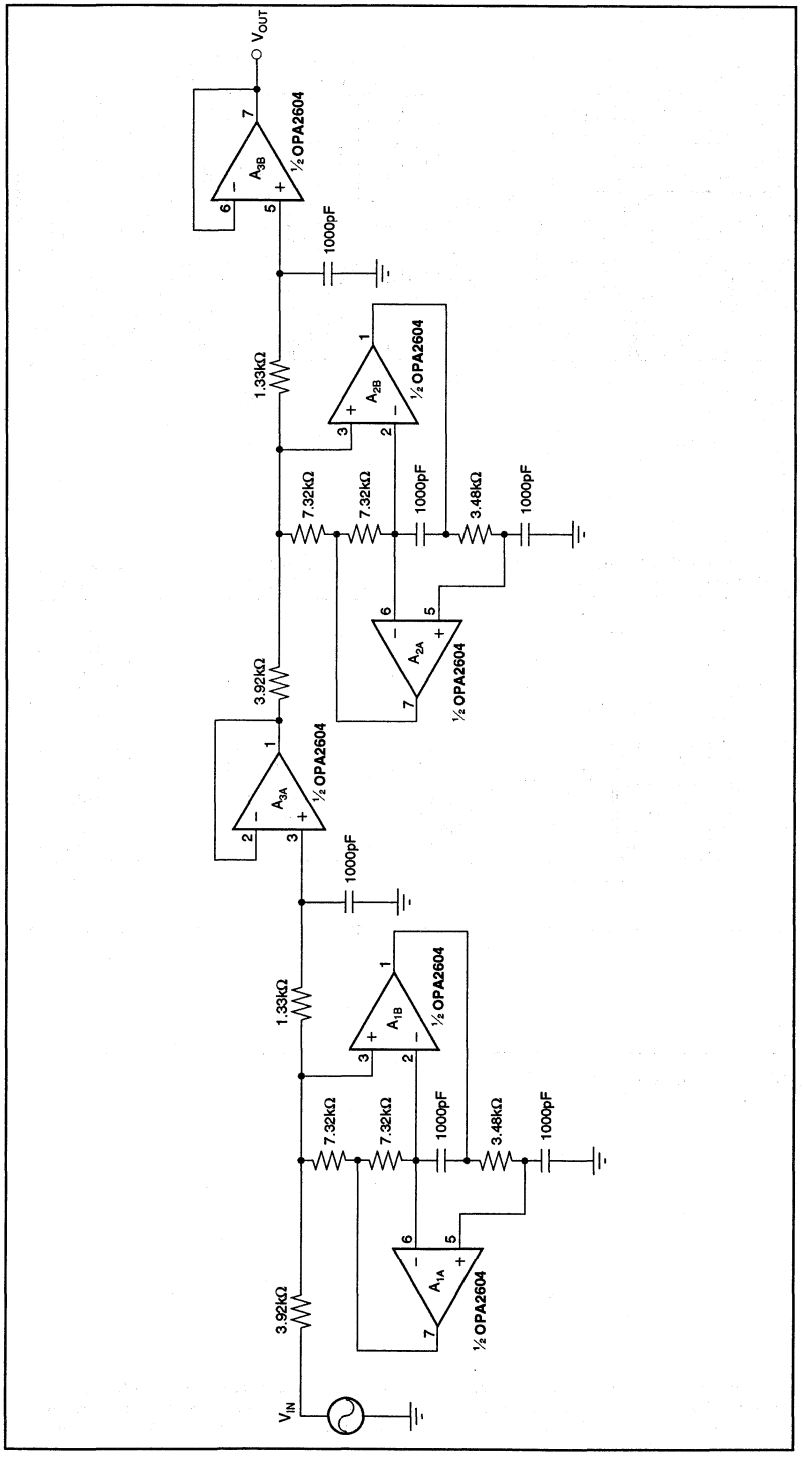


FIGURE 10. Sixth Order Linear-Phase Filter Made by Cascading Two Third Order Filters.

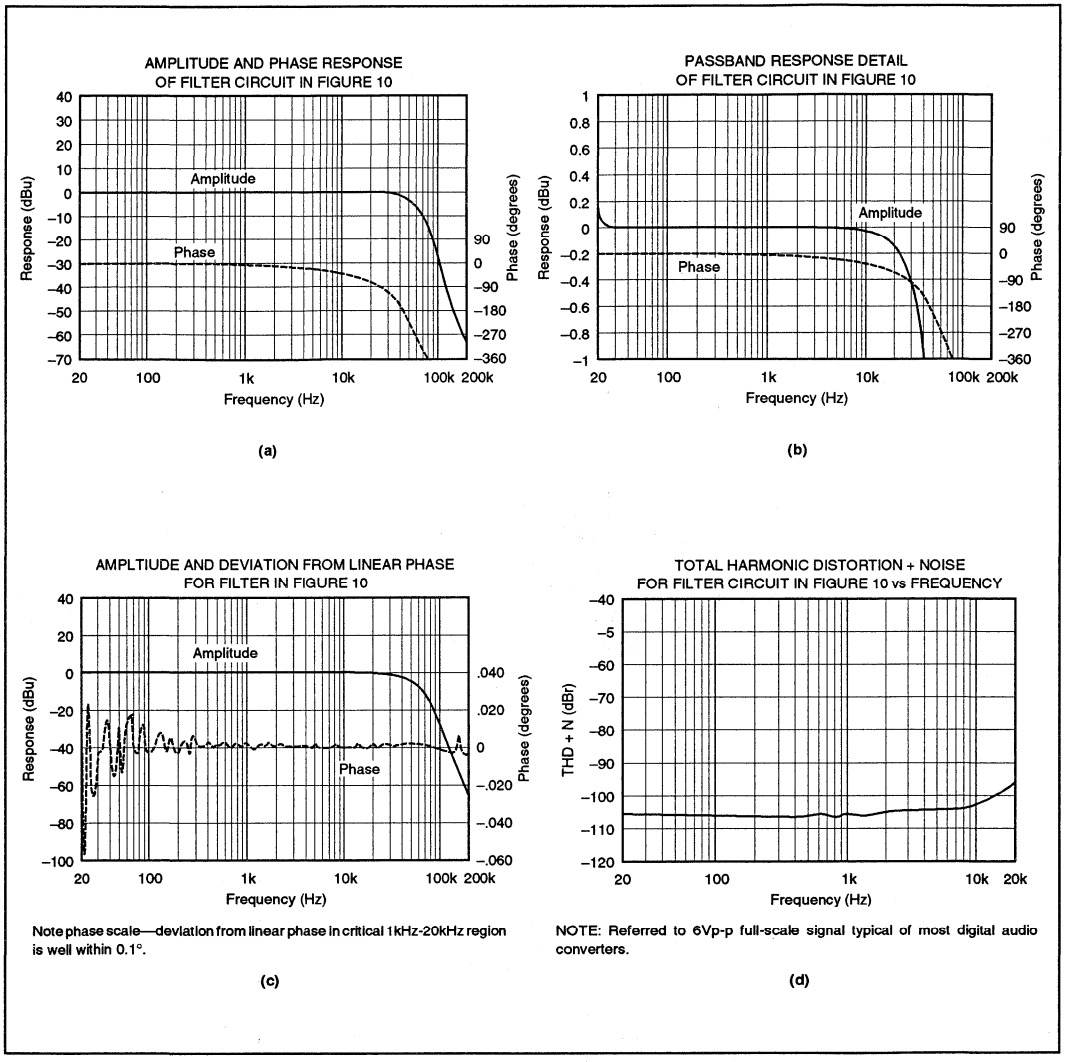


FIGURE 11. Performance Details of Figure 10 Circuit.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

BURR-BROWN® APPLICATION BULLETIN

Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

FAST SETTLING LOW-PASS FILTER

By Rod Burt and R. Mark Stitt (602) 746-7445

Noise reduction by filtering is the most commonly used method for improving signal-to-noise ratio. The increase in settling time, however, can be a serious disadvantage in some applications such as high-speed data acquisition systems. The nonlinear filter described here is a simple way to get a four-to-one improvement in settling time as compared to a conventional filter.

To understand the circuit, first consider the dynamics of a single-pole RC filter (Figure 1). Filtering reduces broadband or "white" noise by the square root of the bandwidth reduction as shown by the following calculation:

$$e_n^2 = \int_{f_1}^{f_2} e_B^2 \, df = e_B^2 \cdot f \Big|_{f_1}^{f_2}$$

$$e_n = e_B (f_2 - f_1)^{1/2}$$

Where:
e_n = total noise (Vrms)
e_B = broadband noise ($V/\sqrt{Hz}$)
f_1, f_2 = frequency range of interest (Hz)

In other words, if the frequency range ($f_2 - f_1$) is reduced by a factor of 100, the total noise would be reduced by a factor of 10.

Unfortunately, settling time depends on bandwidth. The penalty for the noise reduction is increased settling time. For a single-pole filter, the time needed for the signal to settle to any given accuracy can be calculated as follows:

For V_O/V_{IN} at time = t_S

$$\frac{V_O}{V_{IN}} = 1 - e^{-(ts/[R_1 \cdot C_1])}$$

$$-\left(\frac{V_O}{V_{IN}} - 1\right) \cdot 100 = \%$$

therefore

$$t_S = -\ln(\%/100) \cdot R_1 \cdot C_1$$

Where:
t_S = settling time (s)
% = percent accuracy at t_S
$R_1 \cdot C_1$ = RC time constant ($\Omega \cdot F$) or (s)

For example, if a settling to 0.01% is needed,

$$\ln(0.01/100) = -9.2$$

In other words, it takes 9.2 $R_1 \cdot C_1$ time constants for an input step to settle to within 0.01% of its final value.

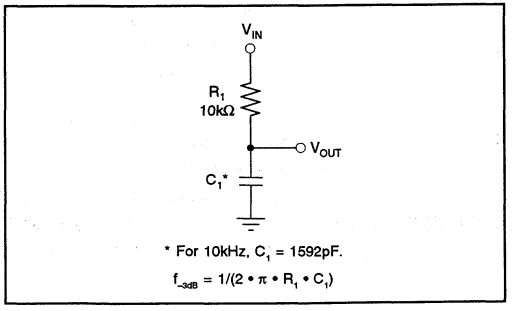


FIGURE 1. Conventional Single-Pole RC Filter.

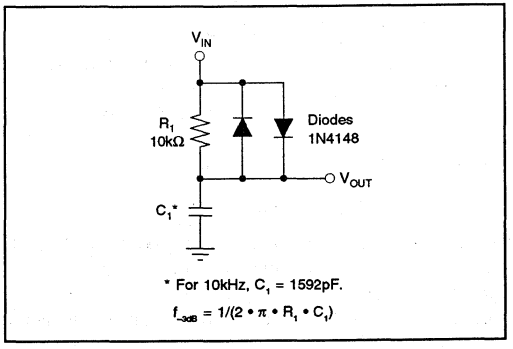


FIGURE 2. Diode-Clamped Nonlinear Filter (can improve 0.01% settling time for a conventional filter by 2/1 for a 20V step).

NONLINEAR FILTER

To understand how a nonlinear filter can improve settling time, consider the simple diode clamped nonlinear filter, shown in Figure 2. Settling time is improved because the filter capacitor, C_1, is charged faster through the low forward biased diode impedance (R_{ON}) during the initial portion of a large input step change. When the difference between the input and output voltage becomes less than the forward biased diode drop (about 0.6V), the diode turns off and C_1 reacts with R_1 alone. At this point, the circuit behaves like a normal single-pole RC filter.

Assuming diode R_{ON} is negligible, the improvement in settling time depends on the ratio of the input step voltage to the forward biased diode voltage. For a step of –10V to +10V (a 20V step), the improvement is ln(0.60/20) or 3.5 time constants. In other words, for a 20V step, the simple

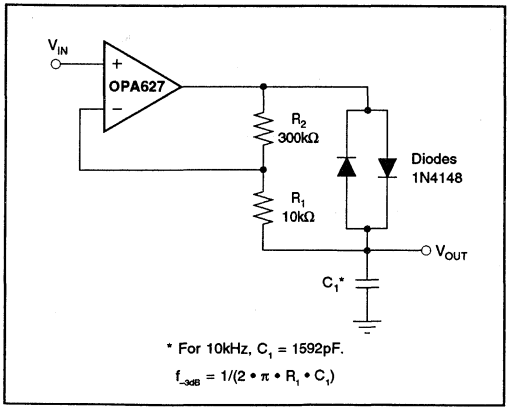


FIGURE 3. Improved Nonlinear Filter (can improve 0.01% settling time for a conventinal filter by 4/1 for a 20V step).

diode clamped nonlinear filter can improve 0.01% settling time from 9.2 time constants to

$$(9.2) - (3.5) = 5.7 \text{ time constants.}$$

For smaller differences between the input step change, and the forward biased diode voltage, the simple diode-clamped nonlinear filter affords less improvement. As the step change approaches the forward biased diode voltage, the simple nonlinear filter offers no improvement.

IMPROVED NONLINEAR FILTER

By reducing the threshold to below one diode drop, the settling time can be improved for smaller inputs. The improved nonlinear filter shown in Figure 3 lets you adjust the threshold to a small arbitrary value by adjusting the ratio of R_1 and R_2.

To see how the improved nonlinear filter works, notice that the op amp forces the voltage at its inverting input to be the same as at the noninverting input. For small differences between the output voltage and the input voltage, the difference is dropped across the 10kΩ resistor, R_1, and the filter behaves like a single-pole filter with an $R_1 \cdot C_1$ time constant. The voltage divider formed by R_1 and R_2 amplifies the voltage difference across R_1, as seen at the top of R_2, by $(1 + R_2/R_1)$. As the voltage across the R_1, R_2 divider becomes larger, one of the diodes (which one depends on signal polarity) begins to conduct, and the capacitor is rapidly charged through it. This occurs at a voltage difference between the input and output of about $0.6V/(1 + R_2/R_1)$ or about 20mV with the values shown. With the diode forward biased, the time constant of the filter becomes very small, limited only by op amp slew rate or current limit.

To determine the component values for the improved nonlinear filter, consider the noise-reduction requirements of the filter. For example, if you want to filter the noise of a 20V full-scale signal to 0.01% resolution, the peak noise must be filtered to less than 0.01% of 20V, i.e. 2mV peak.

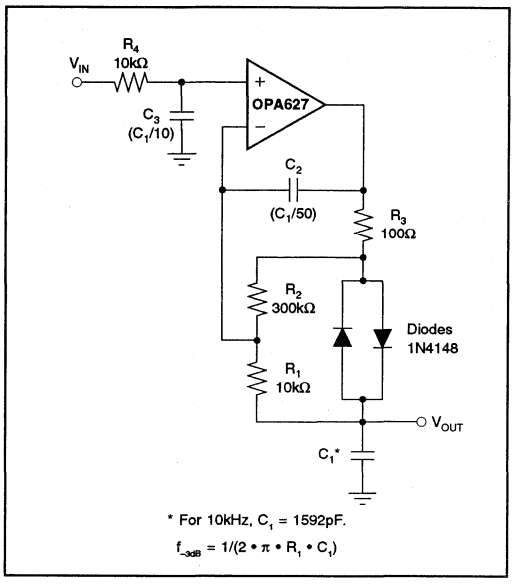


FIGURE 4. Improved Nonlinear Filter with R_4, C_3 Prefilter and R_3, C_2 Network to Assure Op Amp Stability in Driving C_1.

A clamp threshold of ten times this peak (20mV) is an arbitrary but ample threshold. The component values shown in Figure 3 set the filter's threshold to 20mV. For a 20V step as before, the improvement in settling time is ln(0.02/20) = 6.9 time constants. In other words, for a 20V step, the improved nonlinear filter can improve 0.01% settling time from 9.2 time constants to (9.2) – (6.9) = 2.3 time constants—a four-to-one improvement.

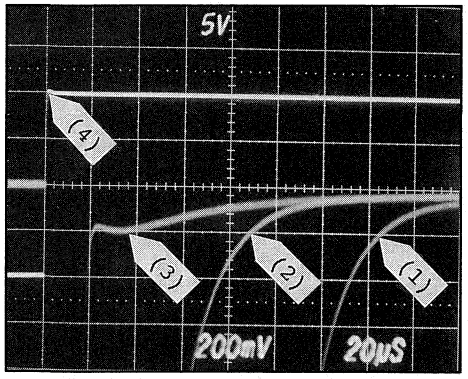
SOME SIGNALS REQUIRE PREFILTERING

In some instances, the input signal may have noise peaks above the 20mV threshold of the nonlinear filter. If the noise of the input signal to the nonlinear filter is greater than the 20mV threshold, the filter will mistake the noise for a step input and fail to filter it out. To prevent this situation an input prefilter can be added to the nonlinear filter as shown in Figure 4.

The prefilter's bandwidth is set by R_4 and C_3. To minimize the prefilter's effect on settling time, its bandwidth is set ten times higher than the bandwidth of the nonlinear filter. At this higher bandwidth, the prefilter's effect on settling time is negligible, and the noise at the prefilter's output is $\sqrt{10}$ times greater than 2mV (a little over 6mV peak). A noise level of 6mV provides a comfortable margin for a 20mV threshold.

ASSURE OP AMP STABILITY

Op amps tend to become unstable and oscillate when driving large capacitive loads. The C_2, R_3 network, shown in Figure 4, assures op amp stability when driving large values of C_1



Traces 1 to 3 show settling response for the various filters. Gain of the signals is 100V/V, so each division of the scope graticule represents 2mV (i.e. each division = 0.01%).

Trace 1 is a standard 10kHz single-pole RC filter.

Trace 2 is a diode-clamped 10kHz nonlinear filter.

Trace 3 is the improved 10kHz nonlinear filter shown in Figure 4.

Trace 4 is the ±10V input signal at 5V/division.

FIGURE 5. Settling-Time Response of Standard and Nonlinear Filters.

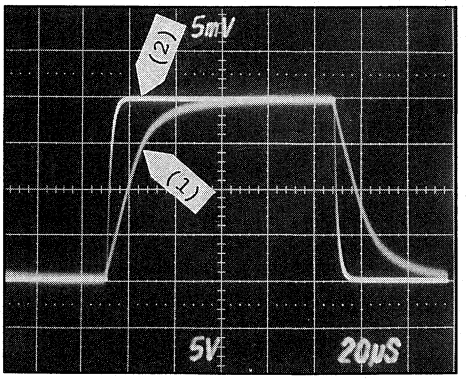
through the low impedance of the forward biased diode network. The C_2, R_3 network may not be needed if C_1 is small.

When choosing the op amp for the improved filter, make sure it has high output drive capability for charging C_1, and that its slew rate, settling time, and DC precision are adequate for the necessary filter response. The OPA627 shown has an excellent combination of DC precision, high slew rate, fast settling time and high output drive capability. The 16MHz bandwidth of the OPA627 gives excellent results for filters with –3dB bandwidths up to 100kHz. Also, notice that the op amp noise adds (at unity gain) to the signal noise. When a low noise op amp is used, this noise will be negligible in most instances.

The OPA627 contributes only a 6% increase in noise to the minimum theoretical noise of the 10kΩ resistor used in the filter. Remember that noise adds as the square root of the sum of the squares. To determine how much the 4.5nV/$\sqrt{\text{Hz}}$ noise of the OPA627 adds to the 12.8nV/$\sqrt{\text{Hz}}$ noise of the 10kΩ resistor, calculate the noise of the two components and compare that to the noise of the resistor alone:

$$\sqrt{(4.5)^2 + (12.8)^2}\,/12.8 = 1.06, \text{ a } 6\% \text{ increase}$$

Figure 5 is a triple exposure scope photo showing the filter output error settling time response for the three circuits to a –10V to +10V input step (20V). The bandwidth of each filter is set to 10kHz. The settling response is in a gain of 100 so that each box represents 2mV, or 0.01% of a 20V step. The filter has settled to 0.01% when the trace is within one box of the base grid.



Trace 1 shows 10kHz single-pole filter response for a ±10mV input step.

Trace 2 shows fast response for a ±10V input step.

FIGURE 6. Comparison of Large and Small Signal Step Response of the Improved Nonlinear Filter.

FILTER TYPE	THEORETICAL SETTLING TIME (time constants)	THEORETICAL SETTLING TIME (µs)[1]
Single-Pole RC	9.2	147
Diode-Clamped Nonlinear	5.7	91
Improved Nonlinear	2.3	37

NOTE: (1) Settling to 0.01% of final value for a 10kHz filter.

TABLE I. Theoretical Settling Times for Various Filters.

For a 10kHz filter, one RC time constant is 15.9µs. Ignoring input slew rate, and diode forward resistance (good approximations for the 10kHz filter when using an OPA627 op amp), the theoretical settling times are shown in Table I.

Notice that the actual measurements shown by the scope photos agree to the theoretical values within the resolution of the photographs.

Figure 6 is a double exposure scope photograph of the improved nonlinear filter operating at a high and low signal level. At the low level (a ±10mV input step), the response is that of a 10kHz single-pole RC filter as expected. At the high level (a ±10V input step), the greatly improved settling response is observed.

BURR-BROWN® APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

CLASSICAL OP AMP OR CURRENT-FEEDBACK OP AMP? THIS COMPOSITE OP AMP GIVES YOU THE BEST OF BOTH WORLDS

By Tim Kalthoff, Tony Wang, and R. Mark Stitt (602) 746-7445

Classical op amps such as the OPA627 have excellent performance in applications where the required gain bandwidth is low compared to the gain-bandwidth product of the op amp. However, increasing closed-loop gain decreases the error-reducing loop gain. Furthermore, starting at relatively low frequencies, the loop gain rolls-off at 20dB/decade of signal frequency increase. In combination these effects can produce significant errors, especially at higher frequencies where the loop gain can be very low.

Current-feedback op amps, such as the OPA603, have good dynamic performance at both low and high gains. This is because the feedback components set both closed-loop gain and open-loop gain, making loop gain and dynamic performance relatively independent of closed-loop gain. Unfortunately, the DC performance (V_{OS}, dV_{OS}/dT, CMR, etc) of current feedback amplifiers is poor compared to classical op amps.

A composite amplifier using a classical amplifier and the OPA603 current-feedback amplifier can combine the best qualities of both amplifiers.

Figures 1 and 2 show noninverting and inverting composite amplifiers. Table I shows suggested component values for selected gains and measured performance results.

DC performance of the composite amplifier is excellent. Since the OPA603 is in the feedback of the OPA627, the composite amplifier retains the excellent DC characteristics of the OPA627. In fact, since the OPA627 does not drive the load directly, its DC accuracy can be better than the OPA627 alone. Thermal feedback within an amplifier driving large loads will cause errors due to internal thermal gradients and package self-heating. The composite amplifier with an OPA603 can drive 150Ω loads to ±10V with no thermal feedback to the OPA627.

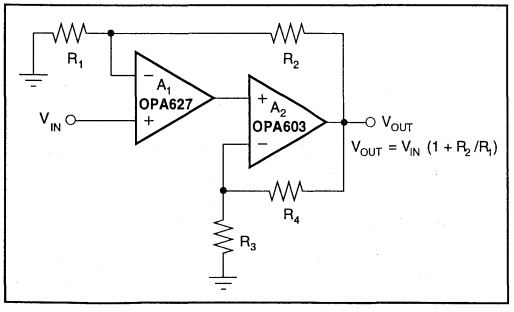


FIGURE 1. Composite Noninverting Amplifier with Precision of OPA627 and Speed of OPA603.

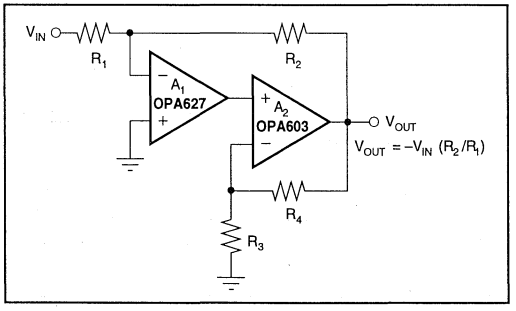


FIGURE 2. Composite Inverting Amplifier with Precision of OPA627 and Speed of OPA603.

OVERALL GAIN [V/V]	GBW [Hz]	A_1	OPA603 GAIN [V/V]	R_1[1] [Ω]	R_2 [Ω]	R_3[4] [Ω]	R_4 [Ω]	SLEW RATE [V/µs]	SETTLING (0.1%)[2] [ns]	SETTLING (0.01%)[2] [ns]
5	90M	OPA627	3	255	1020	499	1020	100	265	520
10	180M	OPA627	6	110	1000	200	1020	240	240	500
20	330M	OPA627	12	52.3	1000	93.1	1020	620	200	520
50	750M	OPA627	26	49.9	2430	40.2	1020	730	320	530
100	1.5G	OPA627	52	49.9	4990	20	1020	730	330	[3]
200	2.5G	OPA637	18	49.9	10k	60.4	1020	580	350	[3]
500	6.0G	OPA637	42	49.9	25k	24.3	1020	590	580	[3]
1000	10.0G	OPA637	85	49.9	50k	12.1	1020	510	640	[3]

NOTES: (1) R_1 shown is for noninverting composite amplifier. For inverting amplifier, R_1 = Gain/R_2. (2) Settling time for 10V output step. (3) Output noise exceeds 0.01% at this gain. (4) For intermediate gains, use the higher value R_3.

TABLE I. Measured Results for Selected Composite-Amplifier Examples.

The gain of the composite amplifier is set by R_1 and R_2 alone. Errors due to R_3 and R_4 do not affect the gain of the composite amplifier. The gain of the second amplifier, set by R_3 and R_4, should be within ±5% to assure expected dynamic performance.

Slew rate and full-power response of the classical amplifier are boosted in the composite amplifier. Since the OPA603 adds gain at the output of the OPA627, the slew rate of the OPA627 is increased by the gain of the OPA603. For example, in the gain-of-100 composite amplifier, the slew rate and full-power response of the OPA627 is increased from 40V/µs min (600kHz) to over 700V/µs (11MHz).

Settling time of the classical amp is preserved, even at higher gains. Settling time of a classical op amp is limited by the time needed to slew to its final value plus the time for its internal circuitry to settle to the desired accuracy. Settling time for a classical op amp is no better than predicted by a single-pole response:

$$T_S = \frac{\ln(100/\%)}{2 \cdot \pi \cdot f_{UGBW}}$$

Where:
T_S = Settling time [µs]
f_{UGBW} = Amplifier unity-gain bandwidth [MHz]
ln(100/%) = Number of time constants needed to settle to desired accuracy, e.g:

ACCURACY (%)	BITS (TO 1/2LSB)	NUMBER OF TIME CONSTANTS
1.0%	6	4.6
0.1%	9	6.9
0.01%	12	9.2
0.0008%	16	11.7

TABLE II.

The bandwidth of a classical op amp decreases with increasing closed loop gain. In a gain of 100V/V, the bandwidth of the OPA627 decreases from 16MHz to 160kHz. The 0.1% settling time therefore can be no better than that of a 160kHz single pole system, or 6.9µs. In the composite amplifier, with the OPA603 in a gain of 52V/V, the OPA627 operates in a loop gain of 2V/V resulting in a measured 0.1% settling time of 330ns.

Care must be taken when selecting the feedback amplifier, A_2, used in the composite. Excessive phase shift through A_2 will cause instability. The OPA603 has sufficient bandwidth to ensure stability when used with amplifiers as fast as the OPA627 (16MHz).

If the bandwidth and settling time advantages of the composite amplifier are needed, but not the slew rate boost, it is possible to make a composite amplifier using a dual op amp such as the OPA2107 as shown in Figures 3 and 4. It is best to use a dual op amp because of the inherent matching of dynamic characteristics. To ensure stability and the best transient response, set the gain of A_1 two times the gain of A_2 using the following relationship:

Gain = $1 + (R_2/R_1)$ noninverting
Gain = $-(R_2/R_1)$ inverting
$R_4 = 10k\Omega$

For Figures 3 and 4,

$$R_3 = \frac{R_4}{\sqrt{R_2/(2 \cdot R_1)) - 1}}$$

For example, if Gain = 100, R_4 = 10kΩ, and R_3 = 1.65kΩ.

Cascading two gain stages (each with a gain of 10V/V) would give an overall transfer function of 100V/V and slightly better settling time, but the gain would depend on the accuracy of R_3 and R_4 in addition to R_1 and R_2. The table below shows predicted 0.01% settling time for the three cases.

CONFIGURATION	SETTLING TIME TO 0.01%
Single Amplifier	20µs
Composite Amplifier	4.6µs
Cascaded Amplifier	4.1µs(1)

NOTE: (1) For cascaded amplifier stages, the combined settling time is the square root of the sum of the squares of the individual settling times.

TABLE III. Predicted Settling Time for Gain-of-100 Amplifiers Using OPA2107 Dual Op Amp (Unity Gain Bandwidth = 5MHz).

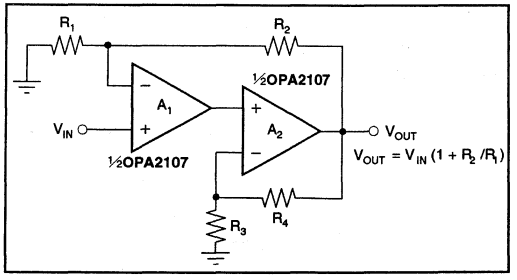


FIGURE 3. Composite Noninverting Amplifier Using Dual Op Amp Settles Fast.

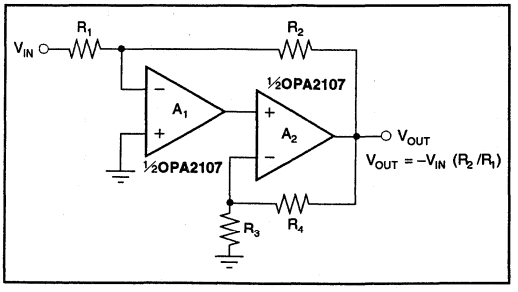


FIGURE 4. Composite Inverting Amplifier Using Dual Op Amp Settles Fast.

BURR-BROWN® APPLICATION BULLETIN

Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

VOLTAGE-FEEDBACK AMPLIFIERS vs CURRENT-FEEDBACK AMPLIFIERS: BANDWIDTH AND DISTORTION CONSIDERATIONS

by Tony Wang, (602) 746-7650

Designers specify amplifiers based on certain key parameters, one of which is bandwidth. Traditionally, the gain-bandwidth product of an amplifier told the user everything he needed to know about its small-signal AC performance. The useful bandwidth of an amplifier was determined by dividing the gain-bandwidth product (GBW) by the desired closed-loop gain. However, this simple formula cannot be used with current-feedback amplifiers.

Current-feedback amplifiers have nearly constant bandwidth for varying closed-loop gains. The reason is that the user can adjust the open-loop gain of the current-feedback amplifier by changing the feedback network without affecting the open-loop pole. The concept can be more readily understood with the aid of Figure 1, which shows a simplified AC model for the current-feedback amplifier.

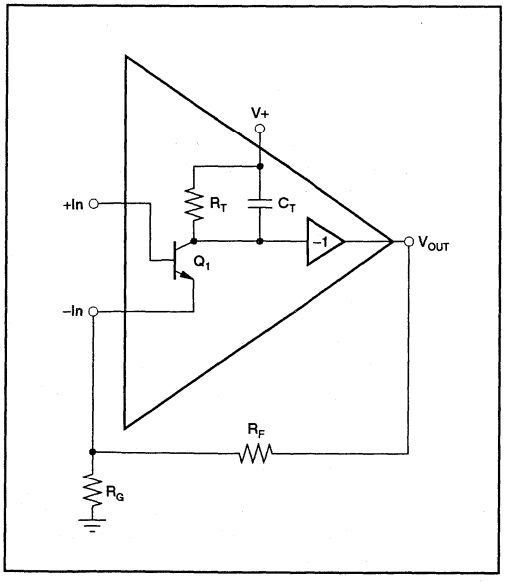


FIGURE 1. Current-Feedback Amplifier Simplified for AC Analysis.

The primary determinants of AC performance for the current-feedback amplifier are the transresistance, R_T, and the transcapacitance, C_T. A well specified current-feedback amplifier's data sheet will list these parameters. Figure 1 shows the current-feedback amplifier with a bipolar transistor as the input device. This is convenient because it has a low impedance inverting input (the emitter) and a high impedance noninverting input (the base). For this analysis, the bipolar transistor is considered ideal (i.e., infinite beta, zero base-emitter voltage, no base-collector capacitance). The collector terminates in R_T, C_T and an inverting buffer. The feedback network consists of R_F and R_G.

Figure 2 shows the same circuit reconfigured for analysis. The feedback network is now the emitter load for the input transistor. Open-loop voltage gain can be determined by inspection to be:

$$A_{OL} = \frac{R_T \,||\, (j2\pi f C_T)^{-1}}{R_F \,||\, R_G}$$

$$= \frac{R_F + R_G}{R_G} \frac{R_T}{R_F} \frac{1}{1 + j2\pi f R_T C_T}$$

$$= A_{CL} \frac{R_T}{R_F} \frac{1}{1 + j2\pi f R_T C_T}$$

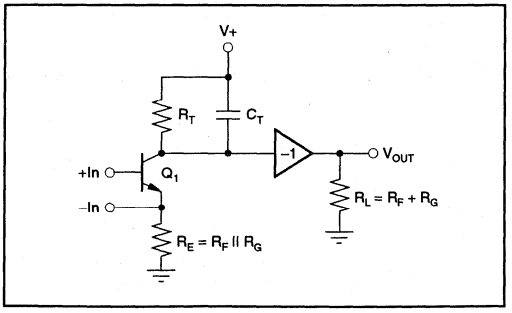


FIGURE 2. Current-feedback Amplifier Simplified and Reconfigured for Analysis.

The last expression shows that the open-loop gain for the current-feedback amplifier varies directly with closed-loop gain (for a given R_F). This is why the current-feedback amplifier has a gain-independent bandwidth. This simplified analysis holds true for low to moderate gains, less than 25V/V, but becomes limited when second-order effects start to dominate.

What this means is that the designer has to look more carefully at how the amplifier is specified. Gain-bandwidth is not meaningful when evaluating a current-feedback amplifier. However, it is an easy way to evaluate traditional voltage-feedback op amps. It is better for the designer to first determine the required gain and then make bandwidth comparisons.

For instance, assume that the application requires processing a 10MHz signal and the amplifiers under consideration are the OPA621 and the OPA603. The OPA621 is a voltage-feedback op amp with 500MHz gain-bandwidth product. The OPA603 is a current-feedback amplifier that can be configured for a useful bandwidth of 100MHz. At first glance, both amplifiers appear adequate but this assumption neglects gain considerations. The circuit configurations of Figure 3 show resistor values for gains of +2V/V and +10V/V. For these gains, the OPA621 has closed-loop bandwidths of 250MHz and 50MHz, respectively.

With the aid of the data sheets for each of these products, a reasonable comparison of open-loop gain can be made. From the OPA621 data sheet, A_{OL} = 60dB = 1,000V/V. This and the GBW are enough information to describe the open-loop gain versus frequency:

$$A_{OL} = \frac{1{,}000}{1 + jf/(500\text{MHz}/1{,}000)} = \frac{1{,}000}{1 + jf/500\text{kHz}}$$

The OPA603 data sheet gives R_T = 400kΩ and C_T = 1.8pF. For these applications, the OPA603 was configured with R_F = 1kΩ. The resulting open-loop gain curves are plotted in Figure 4.

Loop gain is the area bounded above by the open-loop gain curve and below by the desired closed-loop gain. Loop gain is important because it provides a measure of an amplifier's ability to reduce error and maintain fidelity with the original signal. For a gain of +2V/V (6dB), the OPA621 has 9dB more loop gain than the OPA603 at 10MHz. In a gain of +10V/V (20dB), the situation is reversed and the OPA603 has 5dB more loop gain than the OPA621. This is confirmed in the distortion figures tabulated below.

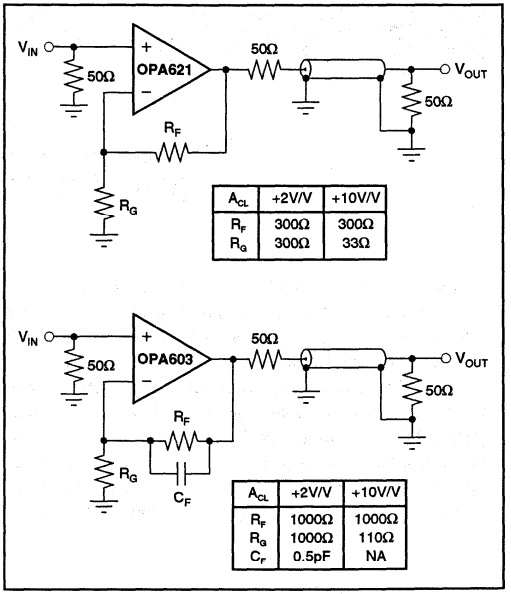


FIGURE 3. Application Circuits for OPA621 and OPA603.

This provides a simple way to compare the useful bandwidths of voltage-feedback amplifiers and current-feedback amplifiers. First, determine the closed-loop gain required, then use data sheet specifications in the formulas presented above to compare the open-loop responses as an approximate indicator of the best op amp for lower distortion.

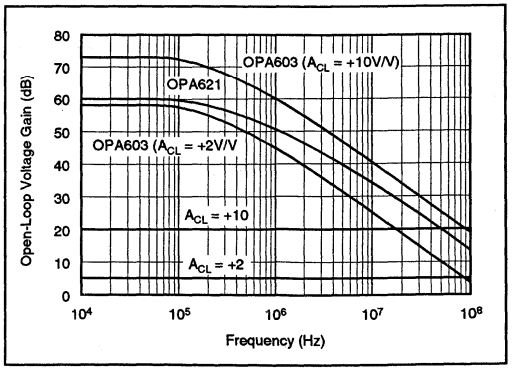


FIGURE 4. Open-Loop Gain Comparisons of the OPA621 and OPA603.

	A_{CL} = +2V/V		A_{CL} = +10V/V	
	OPA603	OPA621	OPA603	OPA621
2nd Harmonic	–65dBc	–68dBc	–63dBc	–50dBc
3rd Harmonic	–78dBc	< –90dBc	–62dBc	–70dBc
Effective Bits	10.5	11	10	8

For Immediate Assistance, Contact Your Local Salesperson

BURR-BROWN® APPLICATION BULLETIN

Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

THE CURRENT-FEEDBACK OP AMP A HIGH-SPEED BUILDING BLOCK

By Anthony D. Wang, Burr-Brown Corp.

Although current-feedback amplifiers (CFAs) have been in use for quite some time, there is a reluctance to view them in the same light as voltage-feedback amplifiers (VFAs). For instance, the gain-bandwidth curve of VFAs has a parallel in a transimpedance-bandwidth curve for CFAs. This parameter can be used to determine the closed-loop behavior of the CFA in the same way that GBW can for the VFA. Not all the fault is with the users—the amplifier manufacturers have not standardized the CFA characterization as they have done with VFAs. This paper describes the CFA and its behavior in an intuitive manner.

HISTORICAL PERSPECTIVE

The term "operational amplifier," or "op amp" in typical engineering shorthand, has generally been associated with the transistorized voltage-feedback amplifier. It is becoming more acceptable now to include the current-feedback amplifier in the same category.

Interestingly enough, the basic architecture for the CFA might have predated the VFA although it was not until the 1980s that the CFA was itself repopularized. To appreciate the evolution of the beast, it helps to look back to some early discrete transistor circuits.

The three transistor amplifier of Figure 1 is arranged in a series-shunt configuration. However, in order to analyze the amplifier, the circuit is rearranged as shown in Figure 2.

The feedback network shows up in two places—a series network at the output and a parallel network at the emitter of the input transistor. This allows for open-loop analysis while keeping the effects of loading intact.

The loading of the output by the feedback network is generally not a problem. However, the gain of the first transistor stage is dependent on the values of the resistors in the feedback network. Thus the open-loop response will change with closed-loop gain (as the feedback network changes), which could make frequency compensation an iterative chore.

The discrete transistor circuit of Figure 3 circumvents this difficulty. Adding another transistor, Q_4, to buffer the input stage transistor, Q_1, from the feedback network illustrates this modification. This is the first step to a voltage feedback amplifier topology.

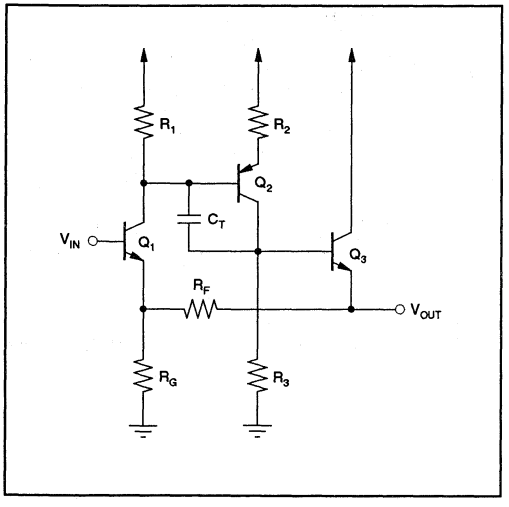


FIGURE 1. Three Transistor Amplifier.

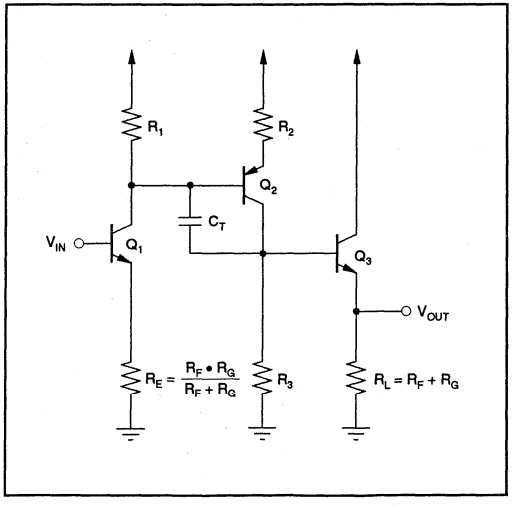


FIGURE 2. Amplifier Redrawn for Analysis.

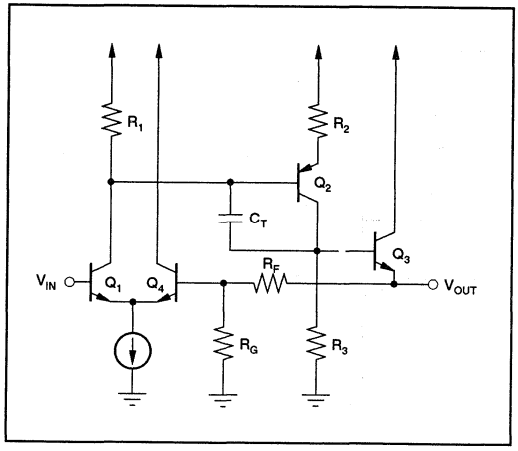


FIGURE 3. Adding a Buffer Transistor.

The added transistor presents a high impedance input to the feedback network. It also features the benefits of a balanced input, such as low offset voltage and equal input bias currents.

Of greater significance is the fact that the dynamic emitter resistance(1) of the added transistor is substituted for the parallel resistance of the feedback network in Figure 2. The first stage gain, and consequently the open-loop gain, no longer depends on the feedback network. The process of frequency compensation has one less degree of variation to be concerned with.

These two circuits illustrate the basic distinctions between current-feedback and voltage-feedback amplifiers. In both cases, the feedback network is connected to an (inverting) input node. In Figure 1, the emitter presents a low impedance input, while in Figure 3 the base presents a high impedance input.

Needless to say, the three transistor amplifier of Figure 1 can be considered the forebear for the CFA as it is known today, while Figure 3 is the template for the VFA. Figure 4 shows the same amplifier connected to a mirror-image of itself, whose transistors have been converted to the opposite polarity type. The input transistors are buffered by emitter followers for level shifting to ensure low offset voltage. This is the basis of the modern current-feedback architecture.

ANALYZING THE CFA

The study of the differential input, voltage-feedback amplifier is simplified with a technique known as "half-circuit analysis." This technique, illustrated in Figure 5, recognizes that the symmetry of the circuit presents an opportunity for simplification whereby only half the signal path needs to be considered.

NOTE: (1) The dynamic emitter resistance is tangent to the slope of the I-V curve for the base-emitter diode

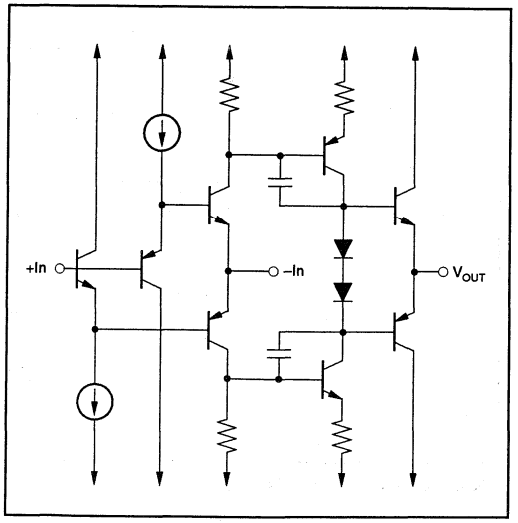


FIGURE 4. Basic CFA Topology.

The NPN current mirror of Figure 5a, which provides double-ended to single-ended conversion, still maintains balance in the circuit because the second stage output voltage is determined by the current that flows into the high impedance presented by the collectors.

Inspection of Figure 4 shows that the axis of symmetry for the CFA is centered horizontally. Therefore, the half-circuit used for analysis is the same circuit as presented in Figure 1, ignoring the input emitter follower. However, as pointed out previously, the feedback network is closely intertwined with the analysis. Therefore, the circuit of Figure 2 can be used for the analysis. The compensation capacitor, C_T, can be the intrinsic base-collector capacitor of Q_2 or an extrinsic capacitor deliberately added for compensation.

The only real difference between Figure 5b and Figure 2 is the presence of the parallel combination of the feedback network resistors in the emitter of the CFA's input transistor.

The CFA analysis is straightforward and the DC gain can be determined by inspection of Figure 2.

$$A_{VDC} = \frac{R_1}{R_E} \bullet \frac{R_3}{R_2}$$

The open-loop pole can be approximated quite accurately as the interaction of the resistor, R_1, with the Miller multiplied capacitor, C_T.

$$\omega_P \cong \frac{1}{R_1\left(\frac{R_3}{R_2} \bullet C_T\right)}$$

This analysis presumes that r_{e1}, the dynamic emitter resistance of Q_1, can be neglected ($R_E >> r_{e1}$) and that R_2 includes r_{e2}.

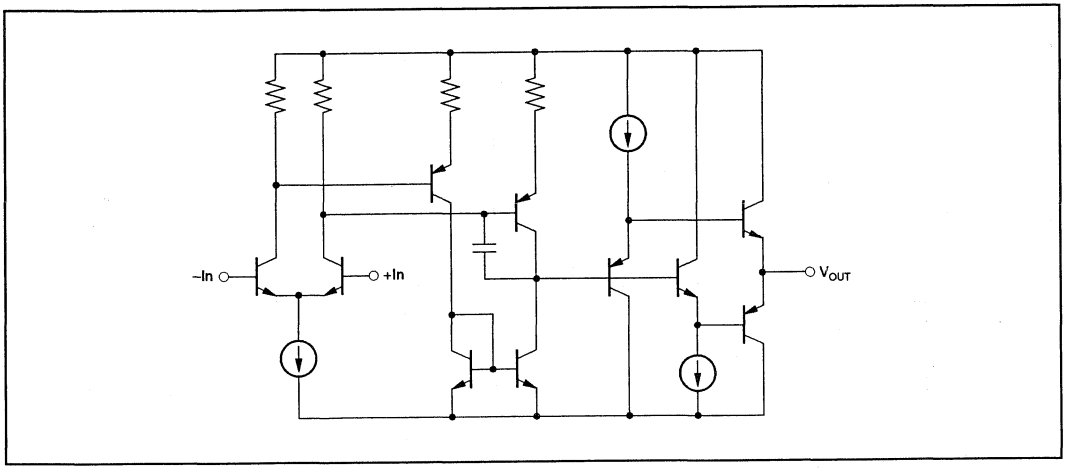


FIGURE 5a. Basic VFA Topology.

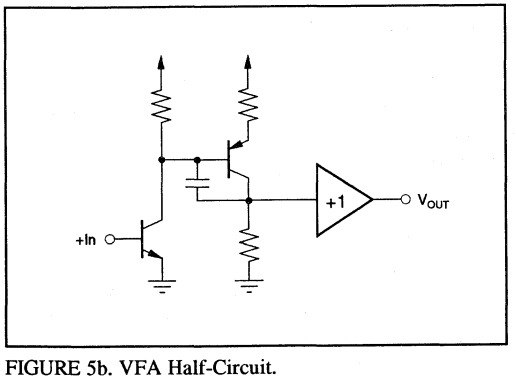


FIGURE 5b. VFA Half-Circuit.

It would be convenient at this point to define the transresistance as:

$$R_T = \frac{R_1 \bullet R_3}{R_2}$$

Note that the transresistance has the dimensions of ohms and is determined solely by elements internal to the amplifier. The previous equations can be rewritten more simply.

$$A_{VDC} = \frac{R_T}{R_E} \quad \text{and} \quad \omega_P = \frac{1}{R_T \bullet C_T}$$

Now the open-loop gain can be completely described by:

$$A_V = \frac{R_T}{R_E} \bullet \frac{1}{1 + j\frac{\omega}{\omega_P}} = \frac{R_T}{R_E} \bullet \frac{1}{1 + j\omega R_T C_T}$$

In order to arrive at this equation, it was assumed that the feedback network was known. This is the crux of the issue—the open-loop voltage gain of a CFA depends on the value of the feedback network.

Removing R_E, the feedback network term, from the equation for open-loop voltage gain yields a more general expression that describes the amplifier's open-loop performance in terms of its intrinsic characteristics. This equation would have units of ohms and would be better identified as a complex impedance, or transimpedance, Z_T:

$$Z_T = \frac{R_T}{1 + j\omega R_T C_T}$$

This is the true measure of performance for CFAs. It is now obvious why the amplifier is known as "current-feedback." The output voltage is responsive to a **current** at the low impedance inverting input node (the emitter of Q_1) that interacts with the open-loop transimpedance, Z_T.

Furthermore, the open-loop response of the amplifier is completely described by the DC transresistance, R_T, and the compensation capacitor, C_T, which is called the transcapacitance. R_T interacts with C_T to form the open-loop pole. This is graphically depicted in Figure 6.

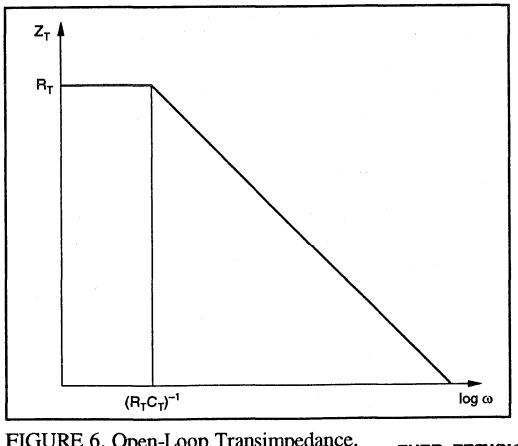


FIGURE 6. Open-Loop Transimpedance.

The ordinate axis has the dimension of ohms and is scaled logarithmically.

Having described the CFA with just two components suggests a simplified version of the half-circuit used for analysis. Figure 7 shows a convenient model that has all the essentials necessary for quick hand calculations. The inverting buffer preserves the sense of the signal as it is amplified by the Q_2 stage in Figure 2.

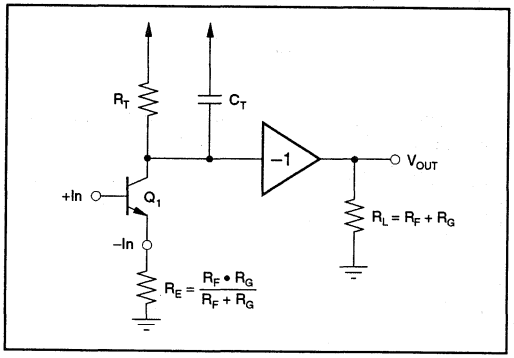


FIGURE 7. CFA Model for AC Analysis.

When determining which op amp to use for an application, comparisons with voltage-feedback amplifiers will inevitably be made. Presumably the closed-loop gain is known, which means that a feedback network can be established. Therefore, the open-loop voltage gain can be calculated for the CFA and a fair comparison with VFA can be established.

Note that the analysis described here is based on a fairly simple current-feedback topology. Although the design of integrated circuit CFAs has become more sophisticated, the open-loop transimpedance approach (Z_T) is still valid.

CLOSED-LOOP PERFORMANCE

The closed-loop response of the CFA can be described by using classical analysis:

$$A_{CL} = \frac{A_V}{1 + A_V \bullet \beta} \quad \text{where} \quad \beta = \frac{R_G}{R_F + R_G}$$

Substituting for A_V yields the following expression:

$$A_{CL} = \frac{\frac{R_T}{R_E} \bullet \frac{1}{1 + j\omega R_T C_T}}{\frac{R_T}{R_F} \bullet \frac{1 + \frac{R_F}{R_T} + j\omega R_F C_T}{1 + j\omega R_T C_T}} = \frac{\text{Open–Loop Gain}}{\text{Loop Gain}}$$

The loop gain, of course, limits the accuracy of the closed-loop gain. Note that $R_T >> R_F$ (typically $R_T > 100k$ and $R_F < 5k$), therefore the equation can be easily simplified to:

$$A_{CL} = \frac{R_F + R_G}{R_G} \bullet \frac{1}{1 + j\omega R_F C_T}$$

The DC value of closed-loop gain is set by the feedback network, while the closed-loop pole is determined by the interaction of the transcapacitance with the feedback resistor. This latter term is what gives the CFA its much touted characteristic of gain-independent bandwidth.

A closer look at the unsimplified equation for the closed-loop gain helps to clarify this property. The DC portion of open-loop gain in the numerator is modified by the parallel combination of the feedback network, which changes with desired closed-loop gain. As long as R_F is kept constant, the loop gain expression in the denominator does not vary, nor do any of the frequency dependent terms.

Figure 8 illustrates graphically that the open-loop gain curve slides vertically to keep the closed-loop intercept frequency constant. Since R_F is kept constant, the area of the curve above the closed-loop gain stays constant.

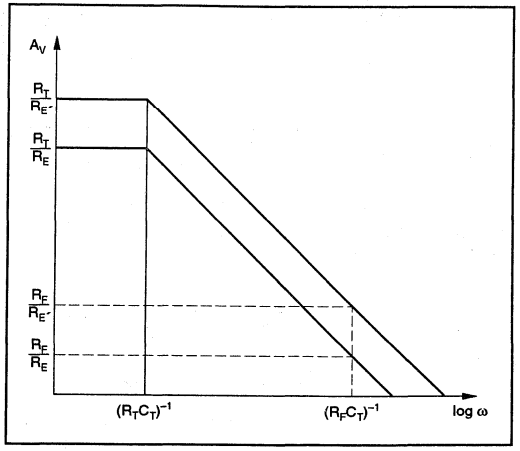


FIGURE 8. Variation of Open-Loop Gain.

The closed-loop gain expressions have been expressed as a ratio of the feedback resistor to the equivalent feedback network. This can be verified algebraically as:

$$\frac{R_F}{R_E} = \frac{R_F}{\left(\frac{R_F \bullet R_G}{R_F + R_G}\right)} = \frac{R_F + R_G}{R_G}$$

Thus, the open-loop gain varies directly with the closed-loop gain for changes in R_E as long as R_F is kept constant.

NONIDEAL CONSIDERATIONS

The assumption that the re of Q_1 can be neglected has limits. For ease of analysis, Figure 6 has been redrawn to include it as a finite input resistance, R_{IN} (Figure 9). Note that R_{IN} is internal to the CFA terminals.

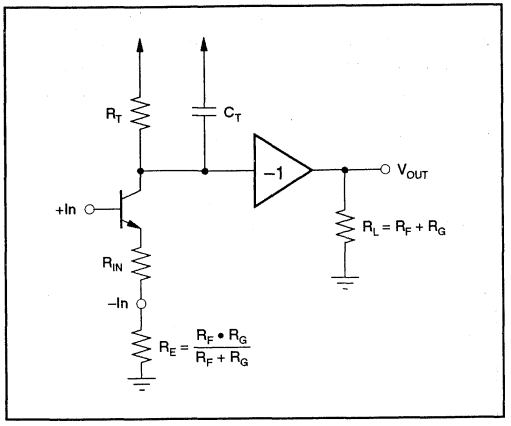


FIGURE 9. CFA Model Modified for Finite R_{IN}.

The open-loop gain equation can be modified by inspection, while a new closed-loop gain equation can again be derived using the classical approach.

$$A_V = \frac{R_T}{R_E + R_{IN}} \bullet \frac{1}{1 + j\omega R_T C_T}$$

$$A_{CL} = \frac{R_F + R_G}{R_G} \bullet \frac{1}{1 + j\omega\left(R_F + \frac{R_{IN}}{\beta}\right)C_T}$$

R_{IN} decreases the open-loop gain but not its corner frequency. On the other hand, R_{IN} does not affect the DC closed-loop gain but does modify the intercept frequency. In practice, R_{IN} includes more than just the dynamic emitter resistance—it also includes bulk resistances that are in series with the inverting input, as well as parasitic resistances external to the amplifier. Obviously, R_{IN} should be as low as possible to get the maximum benefit from a CFA.

The modified equations lead to some practical generalizations when using CFAs. The first is that the open-loop gain has a theoretical maximum and this can be conveniently estimated as:

$$A_{V(max)} \cong \frac{R_T}{R_{IN}} \bullet \frac{1}{1 + j\omega R_T C_T}$$

This is an ideal value that can never be realized since any feedback network will automatically reduce the open-loop gain. However, it is useful for estimating a CFA's merits against a particular VFA.

The second generalization is that the closed-loop bandwidth will become gain-bandwidth limited when

$$\frac{R_{IN}}{\beta} \geq R_F \Leftrightarrow R_{IN} \geq R_E$$

The latter expression makes use of the fact that the feedback factor, β, is a function of the feedback network resistors.

Once this limit has been reached, the CFA can be associated with a gain-bandwidth product, GBW.

$$GBW = \frac{1}{R_{IN} C_T}$$

The graph in Figure 10 shows an asymptotic approach to estimating a CFA's closed-loop response.

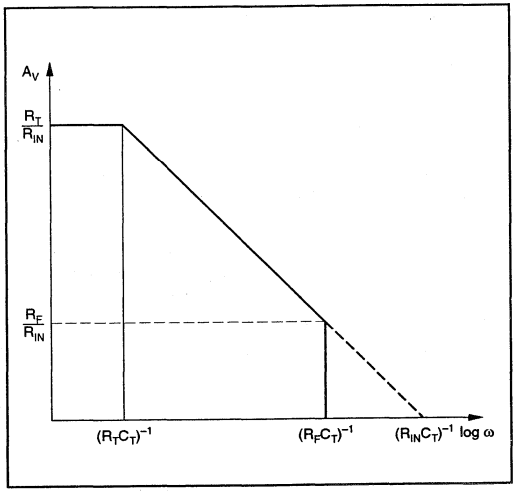


FIGURE 10. CFA Closed-Loop Performance.

To be technically accurate, it should be pointed out that the inverting input is characterized by an impedance, Z_{IN}, which does vary with frequency. Fortunately, the resistive portion, R_{IN}, dominates over most of the CFA's useful bandwidth. At high frequency, the inverting input impedance increases, which only further degrades the closed-loop performance, although the extent of the increase is generally well under an order of magnitude.

FREQUENCY COMPENSATION

The analysis so far has centered on the gain versus frequency performance without taking into account any phase shift considerations. Excess phase plagues the CFA just as it does the VFA. The open-loop transimpedance curve of Figure 6 depicts a single-pole response which would have only 90° of phase shift. Parasitic poles introduce additional phase shift to the open-loop phase response. Figure 11 displays the more complete open-loop transfer curves—both magnitude and phase.

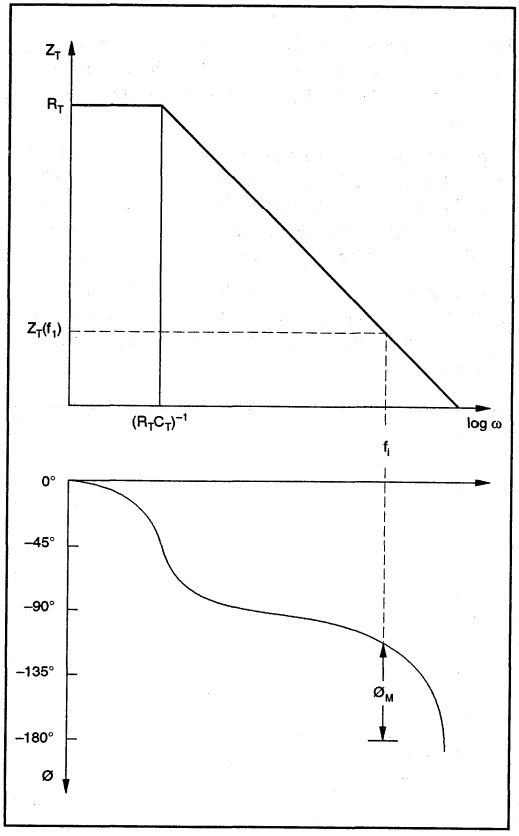


FIGURE 11. CFA Open-Loop Transfer Curves.

Since the feedback network sets the open-loop gain for the CFA, it also sets the phase margin, Φ_M. This is the crucial factor that actually determines the selection of the feedback network resistors.

The significance of phase margin would benefit from a brief review of its properties. Phase margin for operational amplifiers is measured at that frequency, f_U, where an amplifier's open-loop voltage gain has fallen to unity. It is the difference between the open-loop phase shift and –180°, where the amplifier would lose negative feedback and become unstable.

$$\Phi_M = \Phi(f_U) - (-180°)$$

The concept of phase margin is best illustrated by plotting unity gain frequency response curves as phase margin is varied (Figure 12).

As the plot shows, the optimum value for phase margin is 60°. This gives the desirable combination of broad bandwidth with flat frequency response. Note that an amplifier with 90° of phase margin, which implies a lack of excess phase, has a –3dB bandwidth less than half of the optimum response.

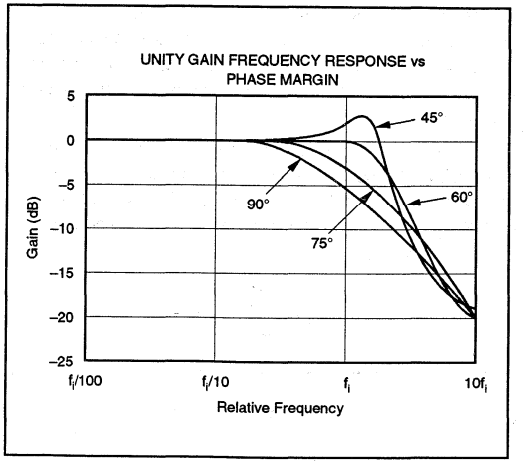


FIGURE 12. Phase Margin's Effect on Frequency Response.

A more general way of looking at this is to make the observation that the closed-loop response can be extended if the open-loop phase has fallen 120° at f_i, the frequency where the asymptote for closed-loop gain intersects the open-loop gain curve.

In VFAs, the phase margin is set by design and the user does not change it. There are a few amplifiers which allow access to the high impedance node to tailor compensation, but these are in the minority. In general, VFAs break out into two categories—compensated and decompensated.

The compensated amplifiers allow operation at unity gain but at the expense of bandwidth in higher gains. Decompensated, or undercompensated, amplifiers must be operated in gains greater than unity but have a higher gain-bandwidth product. In either case, the phase margin is predetermined.

For the CFA, phase margin is set by the user via the feedback network. However, rather than use phase margin as the design criterion, higher performance can be attained by making use of the general observations regarding phase shift and bandwidth. In other words, guarantee that the open-loop phase has fallen 120° at f_i.

The mechanics are rather straightforward because, as illustrated in Figure 8, varying the feedback network causes a simple vertical translation of the open-loop gain curve. The open-loop pole does not move and so the attendant open-loop phase shift is unaffected. The excess phase shift is also insensitive to the feedback network change. Thus, selection of a desired phase shift automatically sets the intercept frequency.

Once the intercept frequency, f_i, is determined, so is the magnitude of transimpedance, $Z_T(f_i)$. This is depicted graphically in Figure 11 by following the dashed lines up from the open-loop phase curve to the intersection with the open-loop transimpedance curve.

To realize the benefit of the –120° phase shift, the feedback network has to be selected so that the open-loop gain equals the closed-loop gain at f_i. A convenient way to visualize this problem is to concentrate on the essentials of the model in Figure 9.

The CFA model can be simplified further by ignoring the inverting buffer and focusing on that portion of the circuit which provides gain. In Figure 13 the CFA model has been reduced to an elementary transistor amplifier. The gain for this circuit is

$$|A_V| = \frac{|Z_T(f_i)|}{R_E + R_{IN}}$$

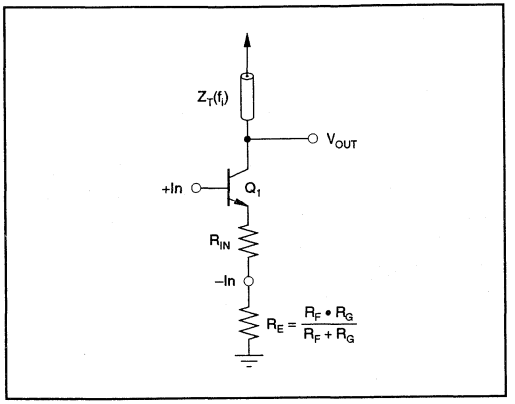


FIGURE 13. Elementary Amplifier.

The goal, therefore, is to select the necessary feedback network so that A_V equals the desired closed-loop gain. Since Z_T has previously been defined as a complex impedance, direct substitution yields a closed form solution.

$$\frac{R_F + R_T}{R_G} = \frac{|Z_T(f_i)|}{R_E + R_{IN}} = \frac{\left|\frac{R_T}{1 + j2\pi f_i R_T C_T}\right|}{R_E + R_{IN}}$$

which can be reduced to a less bulky equation:

$$R_F \cong \frac{1}{2\pi f_i C_T} - \frac{R_{IN}}{\beta}$$

Not surprisingly, this expression conforms to the plot of CFA closed-loop performance (Figure 10). For low gains, the R_{IN} term is negligible and R_F is set by f_i. As closed-loop gain increases and R_{IN}/β can no longer be neglected, R_F should be adjusted according to the equation to maintain optimum performance. When R_F approaches zero, the CFA is becoming gain-bandwidth limited and the intercept frequency must be lowered.

MODEL REPRESENTATION

The single transistor model of Figure 9 is a satisfactory vehicle to provide intuitive insight. It is by no means an accurate representation of the CFA but offers a good visual aid for the user.

A more generally accepted model for the CFA is depicted in Figure 14. This model is a very faithful rendition of the CFA from a block diagram standpoint. It can accurately account for the bipolar input and output swings that are possible with the CFA's complementary symmetry.

Comparing it to Figure 4, it is readily apparent that the unity gain buffer at the input is an accurate portrayal of the input stage between the input pins. The finite input resistance, R_{IN}, is included for completeness.

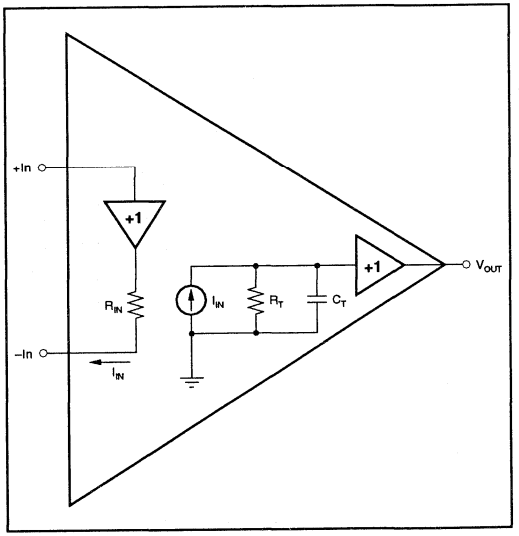


FIGURE 14. Block Diagram CFA Model.

The current-controlled current source, I_{IN}, translates the current from the inverting input to the open-loop transimpedance, again composed of R_T and C_T. The unity-gain buffer provides a low impedance source to the external load.

Either of the models is sufficient to appreciate the CFA and its performance features. Figure 9 bears a strong resemblance to the ancestral antecedent of the CFA while the latter is more readily adaptable to generating a SPICE macromodel.

Other properties of the CFA are apparent when studying these models. The slew rate is limited by the current available to charge the transcapacitance. Decreasing (R_{IN} + R_E) will certainly benefit slew performance. Minimizing C_T will increase slew rate as well as the small-signal performance.

Potential for trouble exists when parasitic capacitance is present at the inverting input. This parasitic capacitance can be the result of poor layout techniques, inappropriate use of a socket or even the wrong package. If C_P is the lumped parasitic capacitor, the open-loop gain will become:

$$A_V = \frac{R_T}{R_E + R_{IN}} \bullet \frac{1 + j\omega R_E C_P}{(1 + j\omega R_T C_T)\left(1 + j\omega \frac{R_E \bullet R_{IN}}{R_E + R_{IN}} C_P\right)}$$

This expression has added a zero and a pole to the transfer function. The zero will always occur before the pole and can be the source of trouble in some cases. If instability arises because of C_P, move the **closed-loop** pole to a lower frequency by adjusting the feedback network.

To model excess phase, the addition of a delay line can be more expedient than trying to add multiple poles and zeroes to the open-loop transimpedance. The modified transfer function is still quite compact.

$$Z_T = \frac{R_T}{1 + j\omega R_T C_T} \bullet e^{-j\omega T_D}$$

The exponential adds phase shift without affecting magnitude. A reasonable technique is to use the phase shift at the highest intercept frequency the circuit is expected to encounter.

$$T_D = \frac{1}{2\pi f_i \bullet \frac{\Phi(f_i) - 90°}{360°}}$$

Here, subtracting 90° from the open-loop phase, $\Phi(f_i)$, removes the phase shift due to the open-loop pole.

DATA SHEET SPECIFICATIONS

The open-loop transimpedance terms, R_T and C_T, and the input resistance, R_{IN}, have already been identified as necessary features to describe a CFA. Additionally, the open-loop transimpedance and phase versus frequency curves should be provided as well.

The block diagram presentation of Figure 14 suggests the other specifications that should not be overlooked. The presence of a buffer between the noninverting and inverting inputs of the CFA guarantees that the input characteristics will not match. This is the main difference between the VFA and the CFA data sheets.

The VFA data sheet typically specifies the power supply and common-mode rejection for the offset voltage only. The input bias currents are also subject to disturbances from these sources but good VFA design encourages matching impedances at the inputs to mask the effects.

The CFA does not have the privilege of bias current match, so the same effects that are specified for the offset voltage need to be measured for the two input currents. In particular, the inverting input, which is the true signal input is often the biggest source of error. It is not uncommon to see a CFA constrained to operate in an inverting gain configuration to circumvent common-mode effects.

It is not very common practice to specify power supply rejection for each supply separately but, for the CFA, it is essential. The complementary devices, NPN and PNP, should not be expected to match each other closely and usually the PNPs are the weaker. PSR measured with tracking supplies typically tend to partially cancel the errors. Real world applications usually rely on independent positive and negative voltage regulators.

The table below is for a medium performance CFA and exemplifies the amount of detail that should be provided.

PARAMETER	TYP	UNIT
INPUT OFFSET VOLTAGE		
Initial	5	mV
vs Temperature	8	µV/°C
vs Common-mode	60	dB
vs Supply (Tracking)	85	dB
vs Supply (Non-tracking)	60	dB
+INPUT BIAS CURRENT		
Initial	5	µA
vs Temperature	30	nA/°C
vs Common-mode	200	nA/V
vs Supply (Tracking)	50	nA/V
vs Supply (Non-tracking)	150	nA/V
–INPUT BIAS CURRENT		
Initial	25	µA
vs Temperature	300	nA/°C
vs Common-mode	200	nA/V
vs Supply (Tracking)	300	nA/V
vs Supply (Non-tracking)	1500	nA/V
INPUT IMPEDANCE		
+Input	5M ll 2	Ω ll pF
–Input	30 ll 2	Ω ll pF
OPEN-LOOP TRANSIMPEDANCE		
Transresistance	440	kΩ
Transcapacitance	1.8	pF
OUTPUT CHARACTERISTICS		
Voltage	12	V
Current	150	mA
Output resistance, Open-loop	70	Ω

TABLE I. Source: BB OPA603 Data Sheet.

SPICE SIMULATION

The combination of declining hardware costs with increasing computing horsepower has made circuit simulation a required part of the design cycle. This has forced the op amp vendors to supply the macromodels for their product offerings.

These simulation tools have been offered in varying degrees of complexity, from the simple Boyle model to simplified circuit models, which utilize full transistor models in the signal path. There has been a growing consensus that this latter approach is necessary for the high bandwidth amplifiers.

There can be no doubt that having these models available helps to fill in the gaps from incomplete data sheets. Although the models may not necessarily be configured for worst case process extremes, there may be some performance peculiarities that can be discovered through their use. The pitfall to be aware of is that even the simplified circuit models generally idealize the biasing circuitry, which may mask some second order PSR and CMR effects.

Figure 15 shows two alternative simulation schemes. In Figure 15a, the CFA is driven open-loop to measure the open-loop transimpedance and input resistance. This requires two separate simulations. The first uses a voltage-controlled current source to find the dc value of inverting input current to servo the output to zero. The second pass is the ac simulation to actually measure the transimpedance.

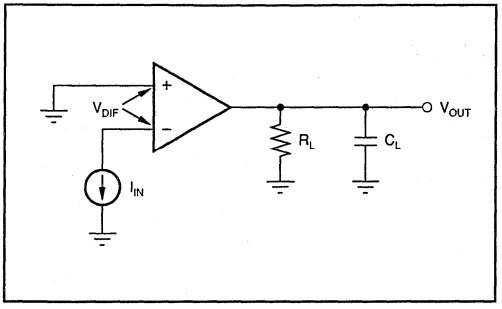


FIGURE 15a. Open-Loop Simulation.

Figure 15b uses a zero volt battery to measure the inverting input current while the op amp is in a closed-loop configuration. This measures an effective transimpedance that includes the common-mode effect.

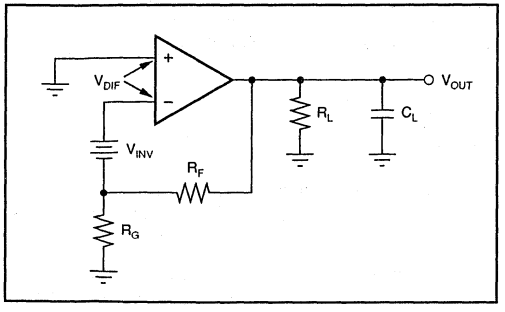


FIGURE 15b. In Circuit Measurement.

The circuit of Figure 15a was simulated with the following listing:

```
* CURRENT-FEEDBACK OPEN-LOOP SIMULATION *
* file: CFA-OL.CIR
***** Simulation Commands *****
.options noecho nomod numdgt=8
.op
.ac dec 20 10 200meg
.probe
***** Library Files *****
.lib burr_brn.lib
***** Circuit Listing *****
vp 7 0 15
vm 4 0 -15
*ginv 2 0 6 0 -1
inv 2 0 dc -38.3pa ac 1
x603 0 2 7 4 6 opa603
rl 6 0 100k
.end
```

Figure 16a is the plot of input resistance as measured by dividing the ac voltage by the ac current. Note that for the useful frequency range of the amplifier (roughly 100MHz), R_{IN} varies less than 10Ω. The open-loop transimpedance is displayed in Figure 16b. Here the magnitude has fallen from a DC value of 790kΩ to 1.5kΩ at 51.6MHz, which is where the open-loop phase has fallen to −120°.

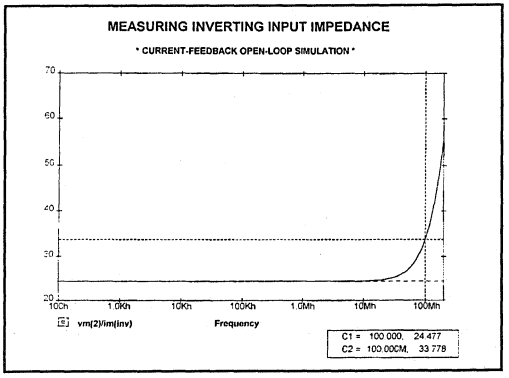


FIGURE 16a. Measuring the Inverting Input Impedance.

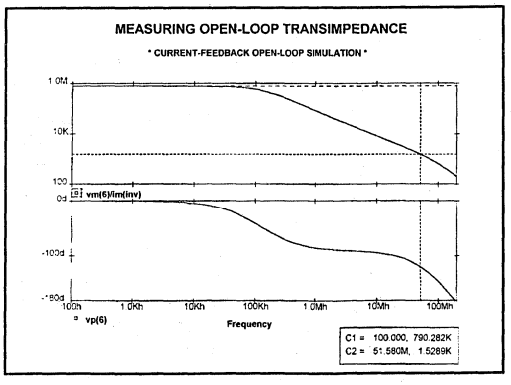


FIGURE 16b. Measuring Open-Loop Transimpedance.

The circuit of Figure 15b was simulated with the following listing:

```
* CURRENT-FEEDBACK CLOSED-LOOP SIMULATION *
* file: CFA-CL.CIR
***** Simulation Commands *****
.options noecho nomod
.ac dec 20 1000 200meg
.probe
***** Library Files *****
.lib burr_brn.lib
***** Circuit Listing *****
vp 7 0 15
vm 4 0 -15
vin 3 0 dc 0 ac 1
x603 3 inv 7 4 6 opa603
vinv inv 2 dc 0
rf 6 2 1450
rg 2 0 1450
.end
```

The plot in Figure 17 shows the intersection of the open-loop gain curve with the closed-loop gain asymptote which occurs at 45.7MHz. The open-loop phase has the value of −120° at this frequency and the broadbanding of the closed-loop gain is quite evident. Note the technique used to gencrate the open-loop gain curve.

The equation relies on the calculation of open-loop transimpedance (via the current in the battery) which is divided by the sum of the equivalent feedback network plus the input resistance.

$$|A_V| = \frac{|Z_T(f_i)|}{R_E + R_{IN}} = \frac{\frac{vm(output)}{im(battery)}}{R_E + R_{IN}}$$

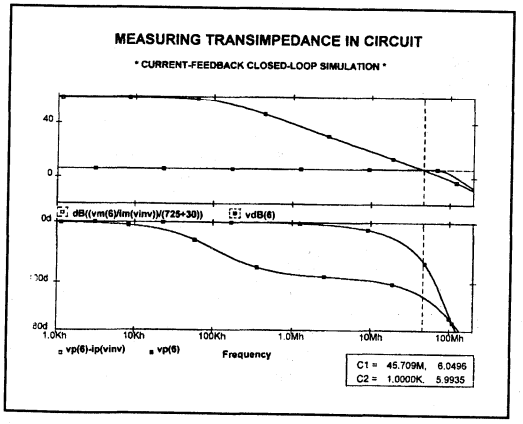


FIGURE 17. Slope Intercept Curves for CFA Circuit.

MEASUREMENT CIRCUITS

If companies could ship only simulation files to their customers, life would be so easy. Sooner or later, a reality check has to be made. The following circuits have been proven to be quite reliable for measuring the CFA performance parameters.

The low impedance of the inverting input node presents a special problem for the test engineer. Conventional op amp test circuits cannot easily separate the individual parameter variations. The most logical solution is to test the CFA with a current mode test circuit.

Figure 18 shows the basic current pump topology used in the DC test circuit. It consists of a JFET input op amp, a P-channel MOSFET and a unique current reference circuit which includes two very accurate current sources and a high precision current mirror.

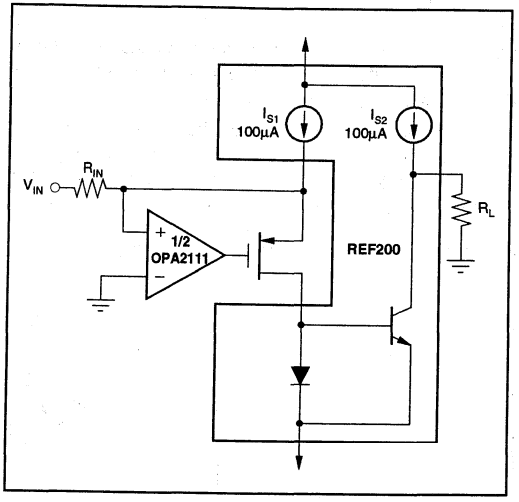


FIGURE 18. Current Pump Topology.

The high gain of the JFET input op amp (VFA) constrains its inverting input to stay at null ground by controlling the current flowing through the MOSFET. If V_{IN} is positive, a current equal to V_{IN}/R_{IN} is shunted to the current mirror input. If V_{IN} is negative, a matching V_{IN}/R_{IN} is provided by the 100µA current source, I_{S1}, and the input to the current mirror decreases. This is an inverting current pump, a positive voltage causes the output to sink current and a negative input causes the output to source current.

The full test circuit is shown in Figure 20. The input offset voltage of the DUT is measured directly by the instrumentation amplifier, A_1. The RC filters minimize noise and protect the inputs of A_1 from overload transients.

Amplifier A_2 maintains the common-mode bias by forcing the current pump (A_3, M_1, IC_1) to keep the noninverting input of the DUT equal to the input, V_{CM}. The output of A_2 driving the 100kΩ input resistor to the current pump is a measure of $+I_b$.

Amplifier A_4 constrains the DUT output to be the negative of the input voltage, V_I, by forcing the current pump (A_5, M_2, IC_2) to drive the low impedance inverting input. The amount of inverting current drive is reflected by the output of A_4.

All DC parameters, including R_T and R_{IN}, can be measured independently and directly. When adapted to a measurement card for the HP Semiconductor Analyzer, the test parameters can be displayed as slopes to determine the limits of linearity.

Figure 19 details an open-loop transimpedance test circuit which, when mated with a network analyzer, will provide the open-loop frequency response curves.

The input ladder network divides the input by 20,000 to provide a low current level signal to the inverting input of the DUT. The 500Ω value for the input resistor dominates the small but finite input resistance of the CFA. The A_1 integrator servos the output to zero by sensing the DUT output and feeding a small current back to the input. A_2 buffers the DUT output and drives the 50Ω input of the network analyzer.

The only caveat is to take into account the gain and phase rolloff of A_2. Automated network analyzers allow for compensation by storing an "offset" sweep which is subtracted from the actual signal sweep.

Although the network analyzer will scale the output in dB, the transimpedance can be determined by using the following equation:

$$Z_T = 500 \bullet \log^{-1}\left(\frac{\text{dB magnitude}}{20}\right)$$

The transcapacitance can be found by extrapolating the open-loop pole.

CONCLUSION

CFAs are not difficult to comprehend and work with if the basic relationships between R_T, C_T, R_{IN} and open-loop phase are kept in mind. The lack of balanced input nodes require extra care be taken with applications requiring DC accuracy. Simulation is a wonderful tool for the early design stages but only actual measurements will grant peace of mind.

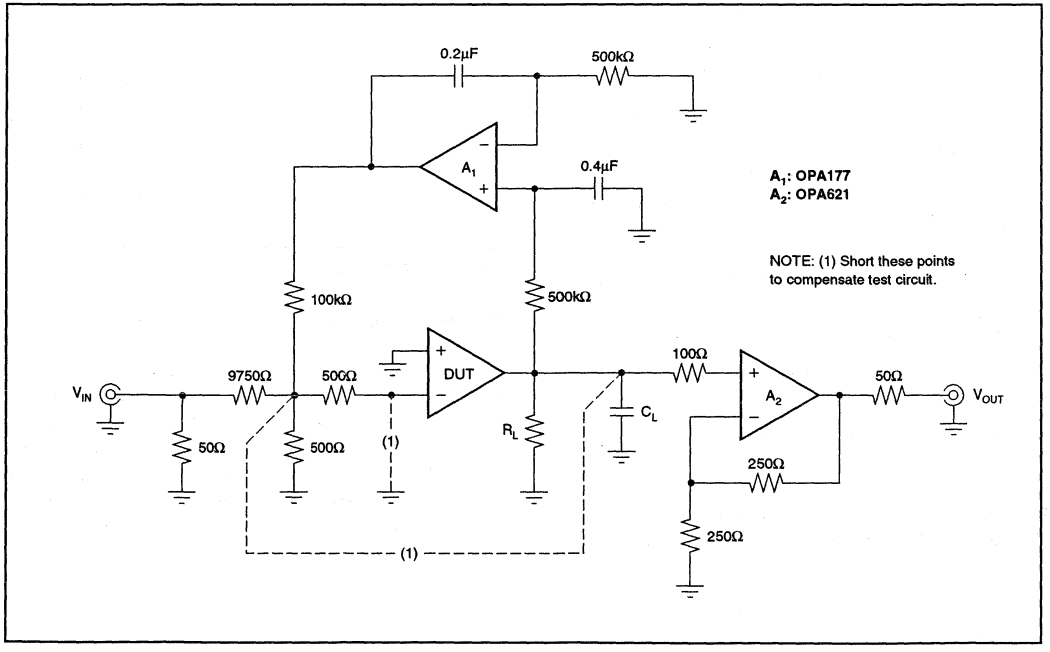


FIGURE 19. Open-Loop Frequency Response Test Circuit.

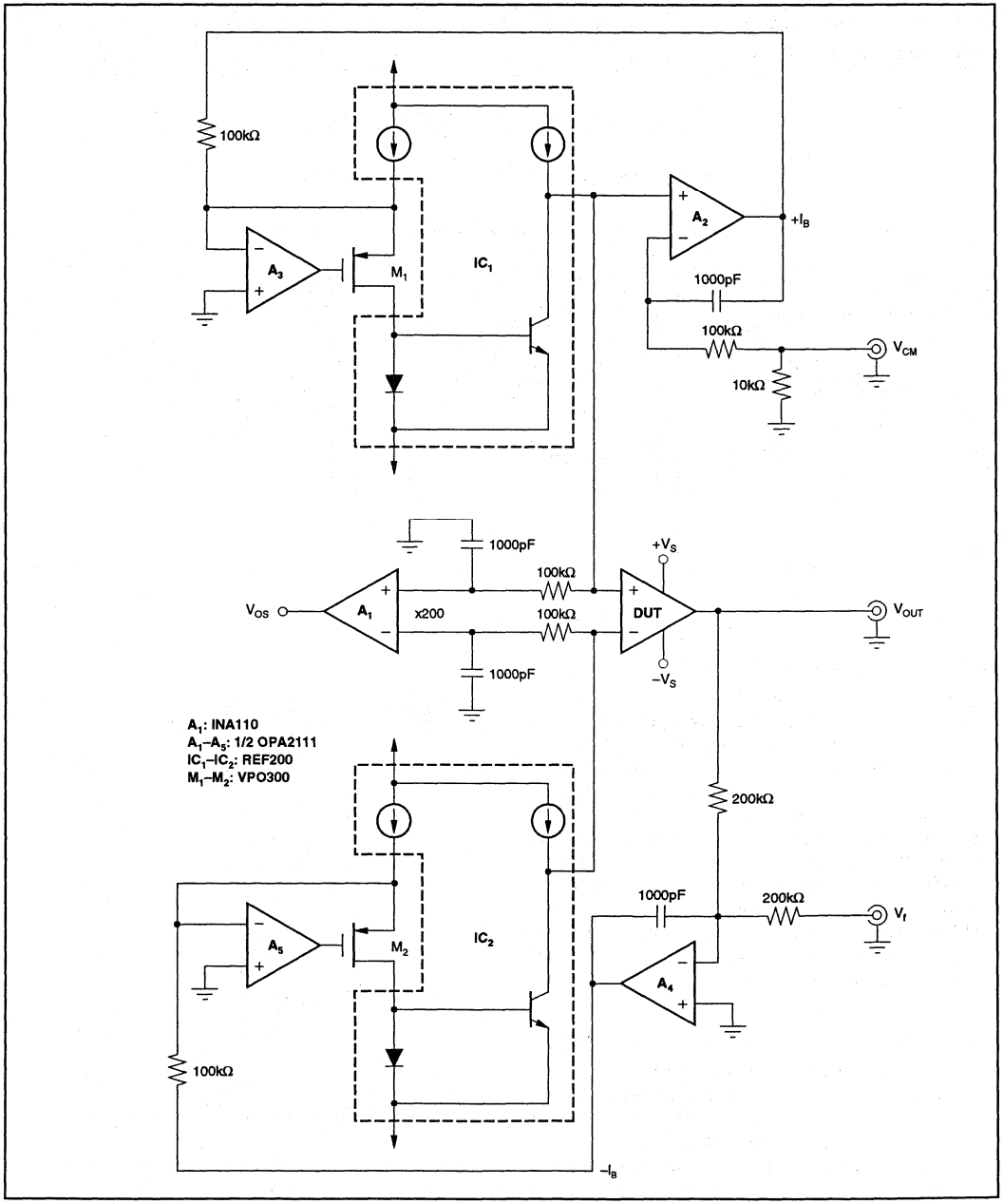
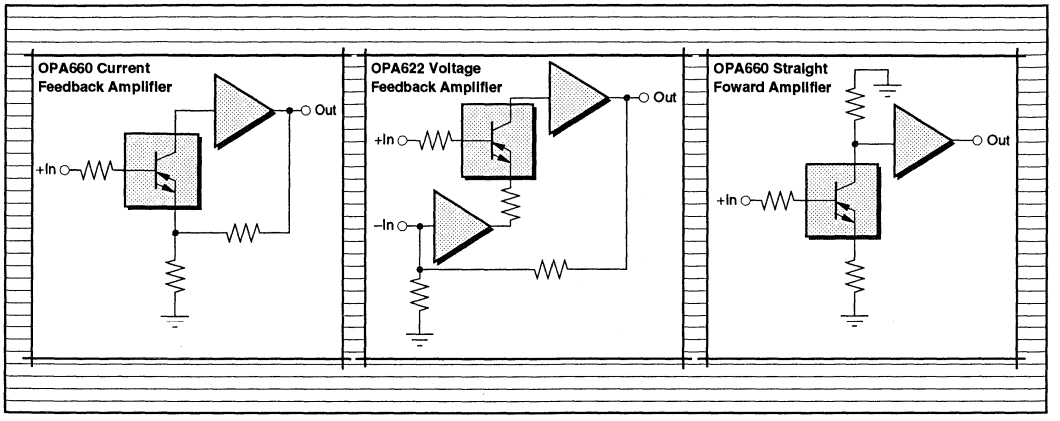


FIGURE 20. Current Mode CFA Test Circuit.

BURR-BROWN®
APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

ULTRA HIGH-SPEED ICs

By Klaus Lehmann, Burr-Brown International GmbH



QUASI-IDEAL CURRENT SOURCE

In addition to their actual operation parameter transconductance, active electronic key components such as vacuum tubes, field effect transistors, and bipolar transistors demonstrate diverse negative parameters. In applying the so-called Diamond structure, the user can obtain an improved current source with reduced disturbance parameters, as well as a programmable transconductance independent of temperature. Standard applications for the Diamond current source (DCS) can be found in buffers, operational amplifiers with voltage or current feedback, and transconductance amplifiers. The DCS simplifies the design of electronic circuits with bandwidths of up to 400MHz and slew rates of 3000V/µs with a low supply current of several mA.

VOLTAGE-CONTROLLED CURRENT SOURCES

For analog signal processing, especially current or voltage gain, previous electronic circuit techniques primarily used vacuum tubes, while today they use field effect or bipolar transistors. The triode illustrated in Figure 1 is representative of the various vacuum tubes, while the N-channel FET represents the FET variations (junctions, insulated gates, depletion, enhancements, P-channels, and N-channels), and a NPN transistor represents the range of bipolar transistors. Triodes, N-J FETs, and NPN transistors are compared with the Diamond current source (DCS). The common elements of all of these active elements are a relatively high-impedance input electrode 1 (grid, gate, basis), a low-impedance

COMPONENT	PARAMETER	TYPICAL VALUE
Triode	Grid Bias Voltage	0 to 10V
	Anode Bias Voltage	20 to 1kV
	Grid Current	nA to µA
	Anode Bias Current	µA to A
	G/K Resistance	kΩ to MΩ
	A/K Resistance	kΩ to MΩ
	Trans Grid Action	1 to 20%
N-J FET	Gate Voltage	0 to –10V
	D/S Voltage	0 to 100V
	Gate Current	fA to µA
	D Bias Current	µA to A
	G/S Resistance	MΩ to GΩ
	D/S Resistance	kΩ to MΩ
	Inverse Amplification	1 to10%
NPN Transistor	Basis Voltage	0.5 to 0.8V
	K/E Voltage	0.5 to 100V
	Basis Current	µA to mA
	K Bias Current	µA to A
	B/E Resistance	kΩ
	K/E Resistance	kΩ
	Inverse Amplification	0.1 to 1%
DCS	V_{OFF1}	–2 to +2mV
	V_{OFF3}	0V
	I_{BIAS1}	nA to µA
	I_{BIAS3}	µA
	R_{12}	kΩ to MΩ
	R_{32}	kΩ
	V_{R31}	<0.1%

TABLE I. Typical Disturbance Parameters of the Voltage-Controlled Current Sources.

input and output electrode 2 (cathode, source, emitter), and a high-impedance output electrode 3 (anode, drain collector). Thus all of these elements can be treated as special voltage-controlled current sources (VCCS = Voltage-Controlled Current Source). The limitation "special" refers to the low-impedance input and output electrode 2. The most important relation between the electrodes 1, 2, and 3 is the transconductance gm. For instance, the transconductance describes the change of the output signal (V_{OUT}) dependent upon the input signal (V_{IN}).

$$V_{OUT} = V_{IN} \times gm \times R_{OUT} \quad (1)$$

To operate each VCCS, it is necessary to adjust the DC quiescent current or voltage individually (see Figure 1).

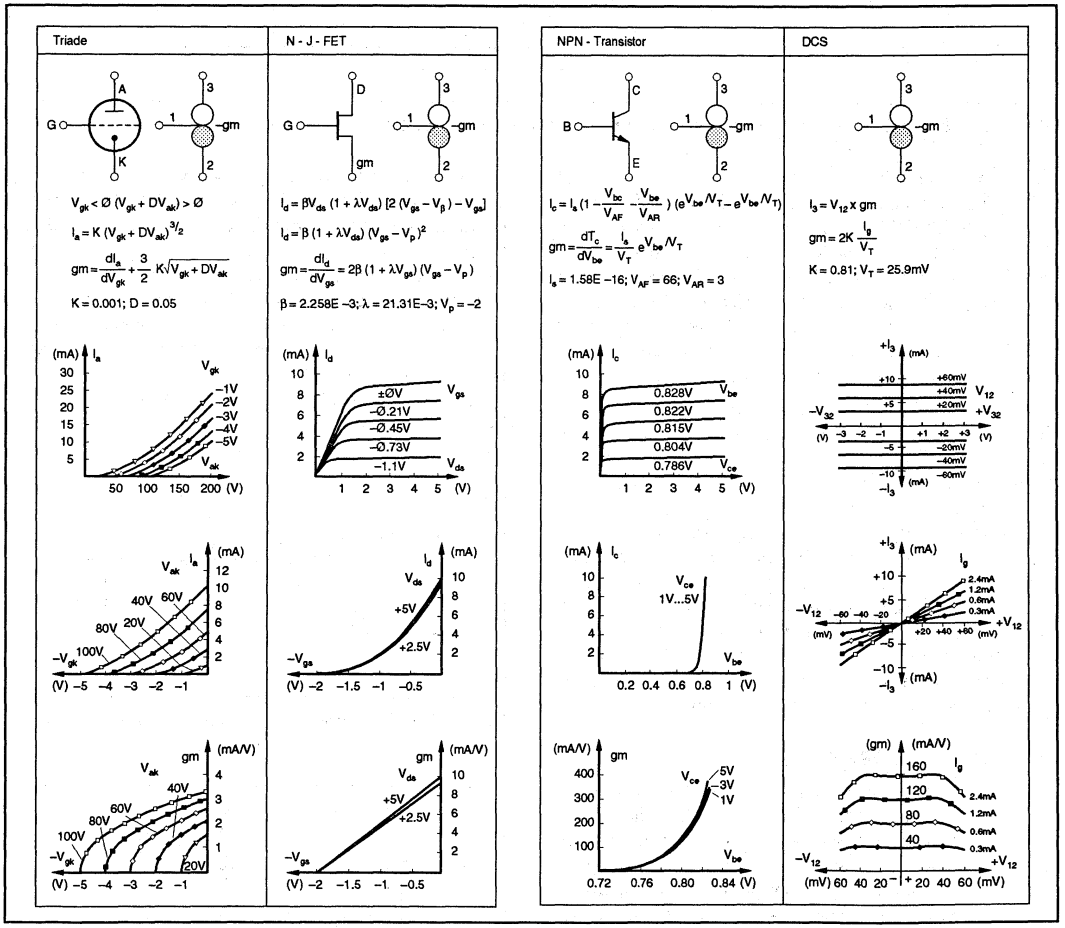


FIGURE 1. Comparison Between Voltage-Controlled Current Source (VCCS) and Diamond Current Source (DCS).

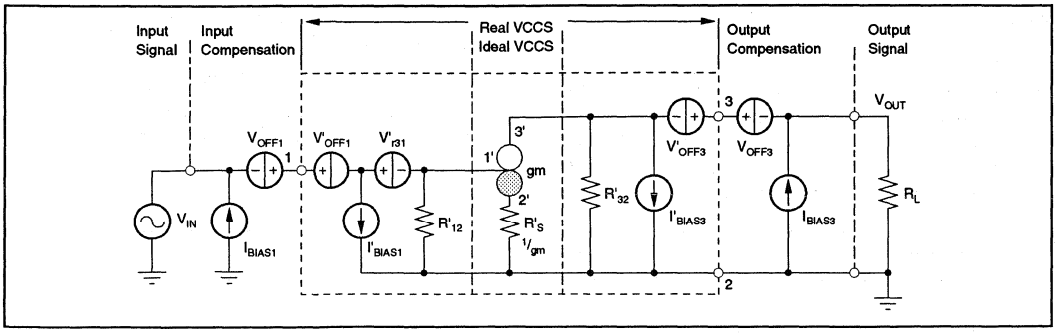


FIGURE 2. Internal and External Substitute Circuitry of a Voltage-Controlled Current Source.

Figure 2 illustrates the inner and outer substitute circuitry of a voltage-controlled current source VCCS. According to the circuitry, the VCCS (1, 2, 3) consists of an inner ideal VCCS (1', 2', 3') with transconductance gm and a row of inner disturbance parameters (V', I', R'), which determine, among other things, the adjustment of the DC point. Table I shows a rough overview of the disturbance parameters. Almost all disturbance parameters are subject to tolerances between units and show dependent temperature behavior.

Figure 2 also illustrates the correction parameters (V_{OFF1}, V_{OFF3}, I_{BIAS1}, and I_{BIAS3}), which are required primarily to compensate the internal disturbance parameters. The correction parameters, however, do not correct the effects of the internal disturbance parameters (R'_{12}, R'_{32}) and the output voltage feed-through V'_{r31}. Roughly stated, at least 50% of the design time for electronic circuit techniques goes toward dealing with the problem of compensation. Thus in complex circuits, the connection between the function parameter gm and the various disturbance parameters requires more and more modifications in circuit variations. If a VCCS without disturbance parameters was available for users, the huge variety of electronic circuit techniques could be reduced.

THE "IDEAL" CURRENT SOURCE

The macro element operational transconductance amplifier (OTA) and operational amplifier (OA) contain circuit parts for reducing the previously mentioned disturbance parameters. The feedback operation necessary with these amplifiers— i.e. the application of a control loop with its unavoidable delay time (phase delays)— causes significantly reduced time and frequency domain performance compared to the VCCS. Straight-forward amplifiers are thus more wide-banded than feedback amplifiers. An operational amplifier OA, as shown in Figure 3, consists of the series connection of an OTA with a buffer B. The OTA is a voltage-controlled current source VCCS, in which the electrode 2 can be used "only" as a high-impedance input. Because of this distinction, the OTA can only be used with an external feedback loop. In contrast to conventional operational amplifiers with voltage feedback as shown in Figure 3, the current-feedback OA contains an OTA with low-impedance input and output 2—i.e. the previously represented "ideal" VCCS. The Diamond circuit, illustrated in Figure 4, opens up the possibility of implementing the quasi-ideal VCCS [2]. In the ideal case, in which NPN and PNP transistors are identical, the disturbance parameters V_{OFF1}', V_{OFF3}', I_{BIAS1}', and I_{BIAS3}' disappear. But in real circuits, of course, this is not the case. The remaining parameter values are, however, much smaller in comparison with a conventional VCCS (compare VCCS with DCS in Figure 1 and Table I). In the modulation range being examined, from $I_3 = \pm 10mA$, the transconductance varies from 120 to 160mA/V as opposed to 0 to 350mA/V. This means that the improved VCCS (designated DCS from now on) causes a reduction in signal distortion.

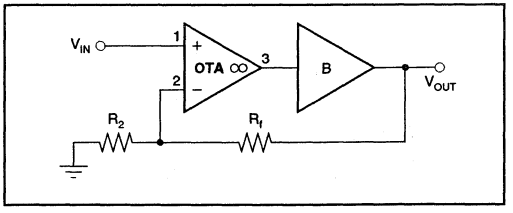


FIGURE 3. Operational Amplifiers as Series Connection Between OTA and Buffer.

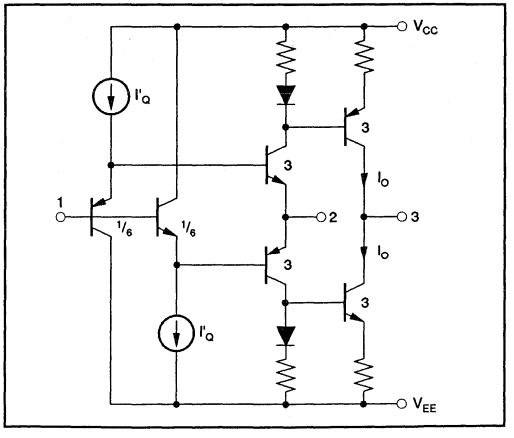


FIGURE 4. VCCS with Diamond Structure.

PROGRAMMABLE TRANSCONDUCTANCE

Conventional VCCSs allow the transconductance to be adjusted depending upon the quiescent current. In the DCS, the transconductance is adjusted primarily with the current sources I'_Q (see Figure 4). For this adjustment, one effective method is to create a current source control (Figure 5).

Using the resistor R_Q, the quiescent current I'_Q or I_Q and thus the transconductance gm can be fixed. The temperature function of gm (due to $V_T = f(T)$) is compensated for by corresponding variations of I_Q. For $R_Q \rightarrow \infty$, $I_Q \rightarrow 0$ and gm $\rightarrow 0$, and VCCS is switched off. In contrast to the conventional VCCS, the DCS functions in two quadrants at the input and in four at the output. In the VCCS, the transconductance is fixed by the choice of DC points within the usable modulation range, while the transconductance in the DCS is largely independent of the modulation and can be adjusted with the external resistor R_Q.

$gm = dI_3/dV_{12}$ is negative for all VCCSs. In contrast, the transconductance $gm = dI_3/dV_{12}$ of the DCS is positive. As previously mentioned, the following standard applications are available for the DCS (Figure 7): Buffer (B), Current-Feedback Transconductance Buffer (TB), Transconductance Amplifier (TA), Direct-Feedback Transconductance Amplifier (TD), Current-Feedback OA (TCC), and Voltage-Feedback OA (TCV).

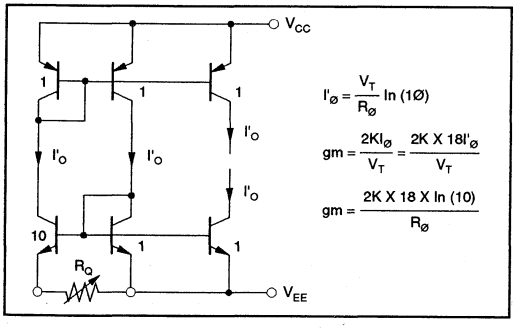


FIGURE 5. Current Source Control with Adjustable Bias Current.

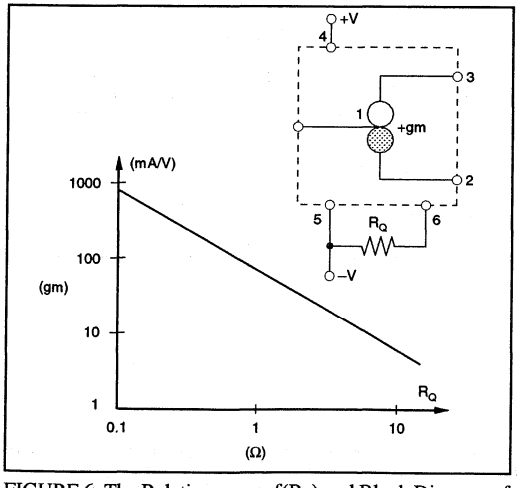


FIGURE 6. The Relations $gm = f(R_Q)$ and Block Diagram of the DCS.

OUTLOOK

To characterize typical dynamic coefficient values (Table II), a developed DCS including a SOI package was simulated in the circuit shown in Figure 8. Burr-Brown brought this DCS onto the market as OPA660.

LITERATURE

[1] Ross, D.G. et al; IEEE Journal of solid-state circuits 86, vol. 2, p. 331.

[2] Lehmann, K; Elektronik Industrie 89, vol. 5, p. 99. Strom-oder Spannungs-Gegenkopplung? (Current or Voltage Feedback? That's the question here.)

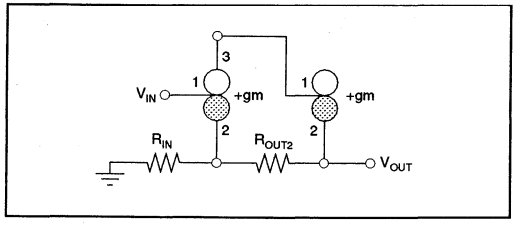


FIGURE 8. Circuit for Recording the Dynamic Characteristic of a TCC with DCS.

I_Q (mA)	0.1Vp-p f_{-3dB} (MHz)	6Vp-p f_{-3dB} (MHz)	4Vp-p SR (V/µs)	1.4Vp-o DG (%)	5MHz DP (Degrees)
2.4	400	330	2850	–0.07	–0.05
1.2	240	200	1750	–0.06	–0.06
0.6	140	100	800	–0.05	–0.10
0.3	80	55	420	–0.03	–0.19

TABLE II. Typical Dynamic Values of a TCC with DCS Corresponding to the Circuit in Figure 8.

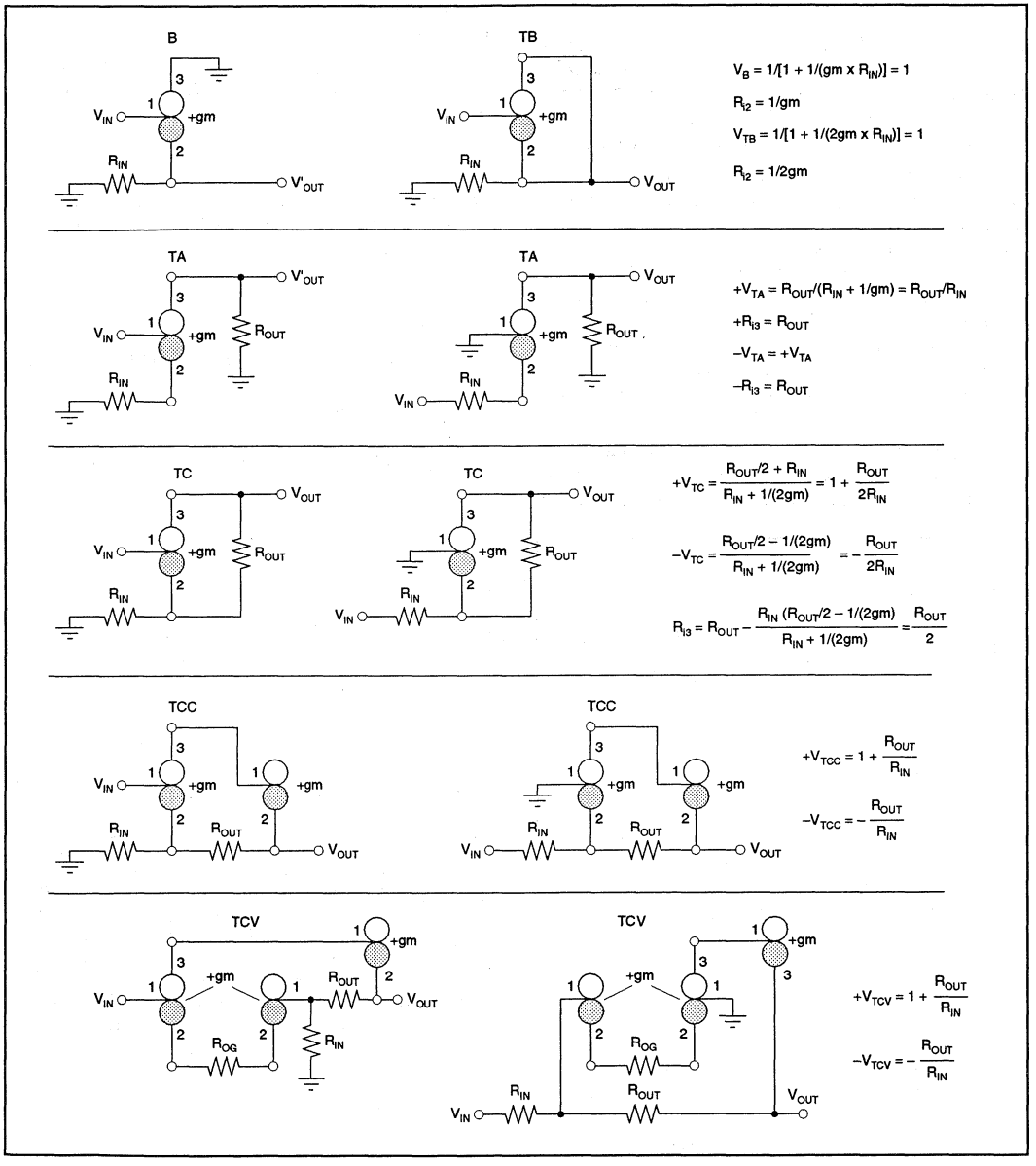


FIGURE 7. Standard Applications with the DCS.

BURR-BROWN®
APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

NEW ULTRA HIGH-SPEED CIRCUIT TECHNIQUES WITH ANALOG ICs

By Christian Henn, Burr-Brown International GmbH

With the increasing use of current-feedback amplifiers, the Diamond Structure has come to play a key role in today's analog circuit technology. Two new macro elements that function in this structure are the Diamond Transistor and its abridged version, the Diamond Buffer. These elements can be used for both voltage and current control of analog signals up to several 100MHz. The OPA660 combines both of these elements in one package. Starting with a discussion of the technical process requirements for complementary-bipolar circuit technology, we would like to focus on the basic and functional circuits of the Diamond Transistor and Buffer. These circuits can be used in areas ranging from video signal processing and pulse processing in measurement technology to interface modules in fiber optic technology.

SYMBOLS AND TERMS

In technical literature, various symbols and terms are used to describe the same circuit structure, see Figure 1. Burr-Brown has chosen the transistor symbol with opposed emitter arrows. The symbol calls attention to the functional similarity of the bipolar and Diamond Transistors, and the double arrows refer to the Diamond Transistor's complementary construction and the ability to operate it in four quadrants. Regardless of how it is depicted, this type of structure has a high-impedance input, a low-impedance input/output, high transconductance and a high-impedance current source output. The voltage is transferred with very low offset of +7mV from the high-impedance input to the low-impedance input/output.

TECHNICAL PROCESS REQUIREMENTS FOR COMPLEMENTARY CIRCUIT TECHNIQUES

Circuits implemented in push-pull arrangements, in which both NPN and PNP transistors are located in the signal path, demand a particular high level of symmetry in the electrical parameters of complementary transistors. See Figure 2.

The most important requirement is that the bandwidths be equal, since the slower transistor type determines the performance capability of the entire circuit. The bandwidth of an integrated bipolar transistor is dependent both upon the base transit time and upon various internal transistor resistances and p-n junction capacitances.

Another important point is the DC performance, which can be described best by the parameters saturation current I_S, current gain BF and early voltage. The Diamond Transistor and buffer are manufactured using a complicated process with vertically structured NPN and PNP transistors. Table I shows the most important parameters of a transistor of size 111. Two metallization layers with a gold surface simplify the connection between the circuit parts.

APPLICATION EXAMPLES

- Wide-bandwidth amplifiers
- Video signal processing
- Pulse processing in radar technology
- Ultrasonic technology
- Optical electronics
- Test and communications equipment

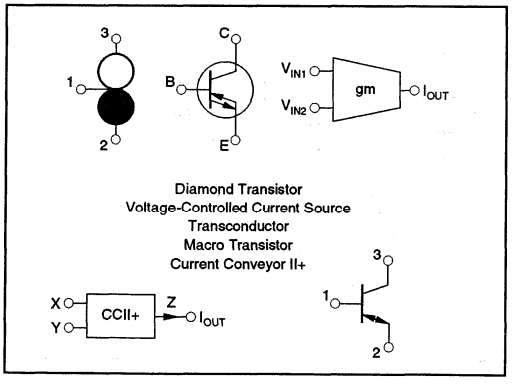


FIGURE 1. Symbols and Terms.

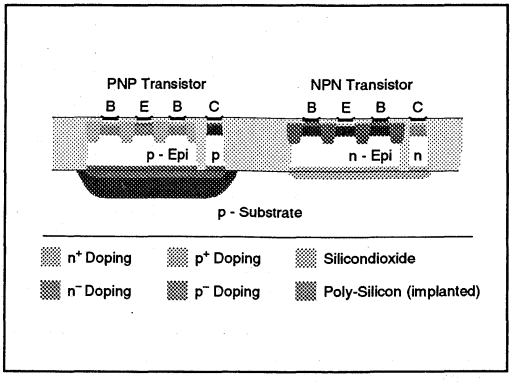


FIGURE 2. Complementary Bipolar Technique (CBip).

PARAMETER	NPN	PNP	DIM
Current Gain	220	115	
Early voltage	66	30	V
C_{JS}	0.26	0.50	pF
C_{JE}	0.02	0.02	pF
R_B	540	429	Ω
R_C	46	43	Ω
Transit Frequency	3.5	2.7	GHz
• symmetric NPN/PNP pairs		• n-epitaxy, p-collector implantation	
• complex process sequence		• complementary B/E structures	
• n-cube		• isolation variations	
• p^+ and n^+ buried layer			

TABLE I. Process Parameter.

SIMPLIFIED CIRCUIT DIAGRAM OF THE DIAMOND TRANSISTOR

The OPA660, Figure 3, is a new type of IC which can be used universally. It consists of a voltage-controlled current source (Diamond Transistor), a complementary offset-compensated emitter follower (buffer amplifier, Diamond Buffer), and a power supply. This new IC enables users to adjust the quiescent current, and through its temperature characteristics, it maintains a constant transconductance in the Diamond Transistor and Buffer. The emitter follower functions without feedback. For this reason, its gain is somewhat less than one and is slightly dependent upon the load resistance. The main task of the emitter follower is to decouple signal processing stages.

It is distinguished by its extremely short delay time of 250ps and an excellent large-signal bandwidth/quiescent current ratio. When comparing the Diamond Buffer with the Diamond Transistor, it becomes apparent that all aspects of the components are identical except for the current mirror. The Diamond Buffer can thus be called an abridged version of the Diamond Transistor.

The Operation Transconductance Amplifier section, or OTA, will be referred to as the Diamond Transistor in the following. Its three pins are named base, emitter, and collector, like the pins of a bipolar transistor. This similarity in terms points to the basic similarity in function of the two transistors. Ideally, the voltage at the high-impedance base is transferred to the emitter input/output with minimal offset voltage and is available there in low-impedance form. If a current flows at the emitter, then the current mirror reflects this current to the collector by a fixed ratio. The collector is thus a complementary current source, whose current flow is determined by the product of the base-emitter voltage and the transconductance. Because of the PTAT (Proportional to Absolute Temperature) power supply, the transconductance is independent of temperature and can be adjusted by an external resistor.

Besides these features, the Diamond Transistor and Buffer can process frequencies of up to several 100MHz with very low errors in the differential phase and gain. Thus, they are universal basic elements for the development of complex circuits designed to process fast analog signals. Current control, voltage control, and operation with or without feedback are all possible with the Diamond Transistor and Buffer. See Table II.

PARAMETER	UNIT
DT Transconductance	125mA/V
Offset Voltage	+7mV
Offset Drift	50μV/°C
Input Bias Current	2.1μA
Output Bias Current	±10μA
Input Resistance	1MΩ ll 2.1pF
Output Resistance	25kΩ ll 4.2pF
Differential Gain	0.06%
Differential Phase	0.02%
Quiescent Current	1-20mA

TABLE II. Diamond Transistor Parameter.

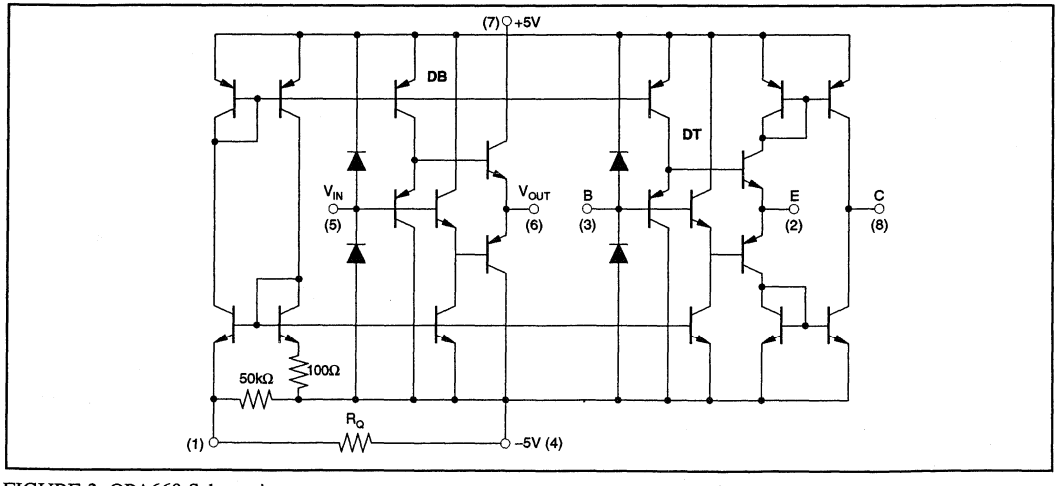


FIGURE 3. OPA660 Schematic.

PTAT POWER SUPPLY

PTAT biasing-controlled current source with adjustable quiescent current, Figure 4.

Each individual transistor stage has a current source as the load impedance. Thus, control of the current source allows adjustment of the quiescent current. The adjusted quiescent currents and the transistors used determine the transconductance of the entire circuit. An external resistor, R_Q, fixes the quiescent current. We will discuss the exact equations for the ratio of the quiescent currents R_Q and transconductance to I_Q in detail later in this paper.

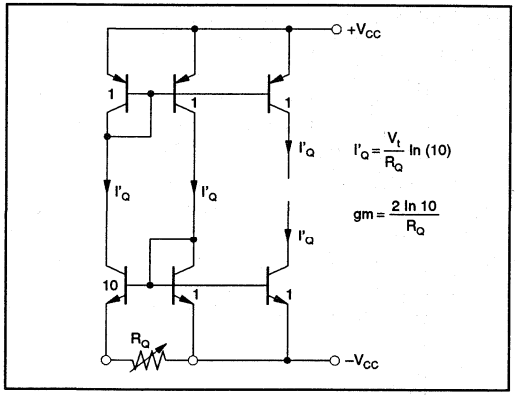


FIGURE 4. PTAT Power Supply.

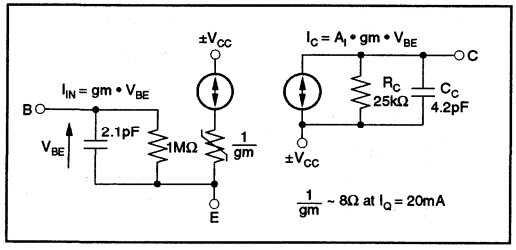


FIGURE 5. Equivalent Circuit.

EQUIVALENT CIRCUIT DIAGRAM

The user can construct a simple equivalent circuit diagram, Figure 5, for the Diamond Transistor based on the previous descriptions. The complementary emitter follower with an input impedance of 1MΩ ‖ 2.1pF at the base pin can be regarded as a controlled voltage source. Using the fact that an emitter follower is, in principle, a voltage-controlled current source whose current flow is dependent upon the voltage difference between base and emitter, it is possible to determine the output resistance of the emitter. The output resistance can best be approximated as the reciprocal value of the transconductance. A quiescent current set at 20mA results in a transconductance of 125mA/V and a low-impedance output resistance of 8Ω, which is adjustable but stable with temperature. The collector pin performs like a complementary current source, with output impedance 25kΩ ‖ 4.2pF. The possible positive or negative current flow results from the product of the input voltage difference times transconductance times current mirror factor, which is fixed at A_I = 1 in the OPA660. The model presented here shows the similarity to the small-signal behavior of the bipolar transistor.

OPA660 BASIC CONNECTIONS AND PINOUT CONFIGURATION

For trouble-free operation of the OPA660, several basic components on the power supply, as well as those components which define function, are necessary. See Figure 6. The triple configuration of the supply decoupling capacitors at pins 4 and 7 guarantees a low-impedance supply up to 1GHz and supplies the IC during large-signal high-frequency operation. The voltage supply is ±5V, resulting in a maximum rated output of ±4V. As already mentioned, the external resistor R_Q between pin 1 and –5V adjusts the quiescent current. A resistance value of 250Ω results in a quiescent current of 20mA. Process variations can cause this current to vary between 16mA and 26mA. The product data sheet illustrates the exact relation between R_Q and I_Q. As in discrete HF (high-frequency) transistors, a low-impedance resistor damps oscillation that might arise at the inputs. The circuit consists of the pin capacitances and inductances of the bond wires. The resonant frequency is between 750MHz

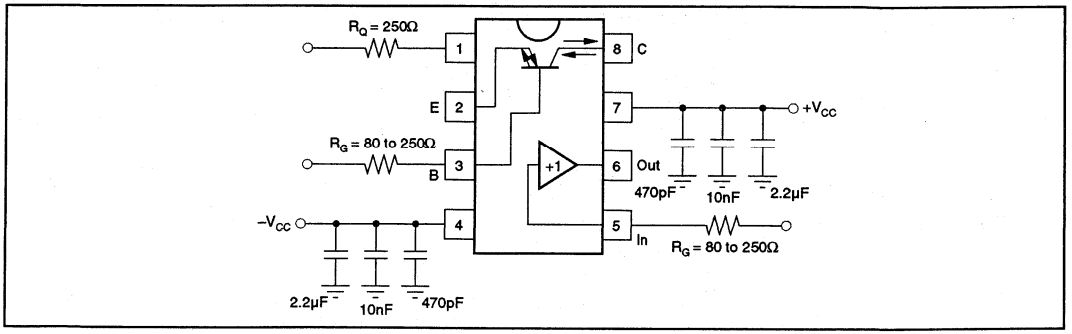


FIGURE 6. OPA660 Basic Connection

and 950MHz, depending upon the package type and layout, and is outside the operating range. The damping resistance is between 50Ω and 500Ω, depending upon the application.

TEST CONFIGURATION FOR DETERMINING THE DYNAMIC FEATURES OF THE DIAMOND TRANSISTOR

Figure 7 shows the test configuration to determine the dynamic features of the Diamond Transistor. The entire test system functions as a 50Ω transmission system to avoid reflections from the input resistances. Various signal generators and indicators can be used depending upon the measurement task. The layout of the demo boards used here is designed for minimum line length and stray capacitance and uses the three-level combination of supply decoupling capacitors and 50Ω HF-connectors. Burr-Brown offers these demo boards to support design engineers during the test phase.

FUNCTION DIAGRAMS

The diagrams introduce two important characteristics that help engineers to understand how the Diamond Transistor functions as a voltage-controlled current source with adjustable quiescent current.

Figure 8a shows the transfer curve I_O/V_{BE} with the quiescent current as a parameter. The transconductance increases with increasing quiescent current.

Figure 8b illustrates the transconductance dependency upon the input voltage. It is clear from this diagram that the transconductance of the Diamond Transistor remains more stable over the whole input voltage range than that of a bipolar transistor.

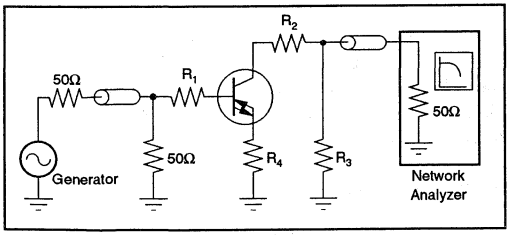


FIGURE 7. Test Circuit OTA.

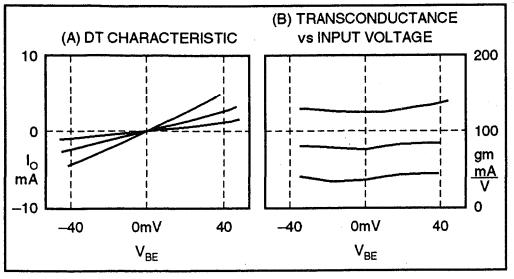


FIGURE 8. OTA Transfer Characteristics.

BASIC CIRCUITS WITH THE OPA660

Listed below are the basic circuits possible with the Diamond Transistor:

- Emitter Circuit
- Base Circuit
- Common Emitter
- Common Emitter with Doubled Output Current
- Current-Feedback Amplifier
- Direct-Feedback Amplifier

As already mentioned, the signal transmission of the Diamond Transistor is the inverse of that of the bipolar transistor. The emitter circuit functions in non-inverting mode and the base circuit in inverting mode.

The emitter-collector connection enables the user to increase the output current of the emitter follower. Since both currents flow in the same direction and the current loop factor A_I of the OPA660 equals 1, the output current doubles to ±30mA and the output resistance halves. See Figure 9.

In many applications, the high-impedance collector output is a disadvantage. One possible solution to this problem is to insert the complementary emitter follower between the collector and the output. The emitter follower then ensures that the load resistance of the collector pin is high and that the output of the circuit can drive low-impedance loads. See Figure 10.

The inverting base circuit has a low-impedance input. This current input has clear advantages in amplifying outputs of sensors which deliver currents instead of voltages.

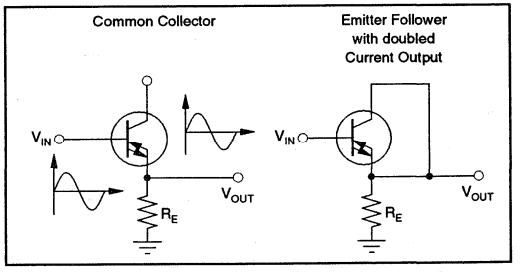


FIGURE 9. Emitter-Collection Connection.

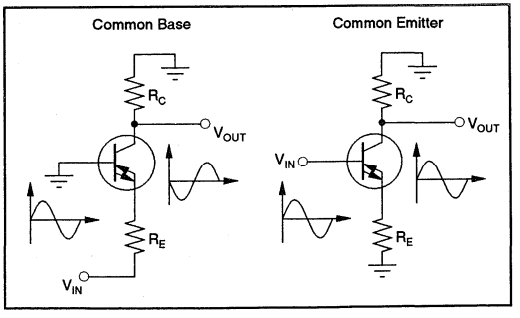


FIGURE 10. Emitter Follower.

V_{OUT}	f_{-3dB}
±100mV	351MHz
±300mV	374MHz
±700mV	435MHz
±1.4V	460MHz
±2.5V	443MHz

TABLE III. –3dB Bandwidth vs Output Voltage.

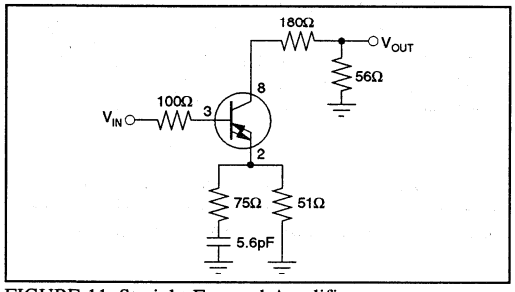


FIGURE 11. Straight Forward Amplifier.

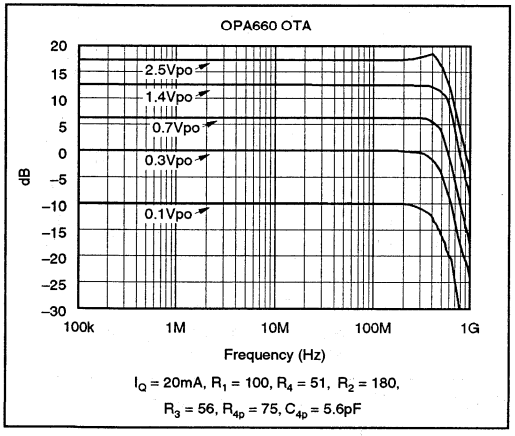


FIGURE 12. Straight-Forward Amplifier Frequency Response.

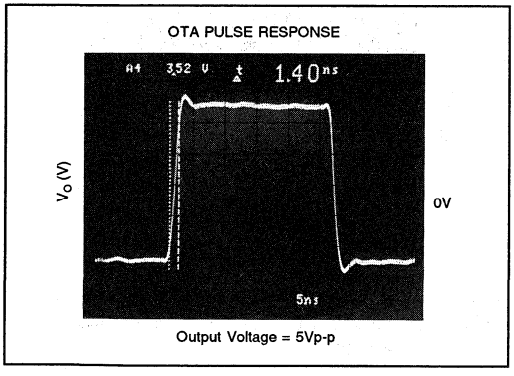


FIGURE 13. Pulse Behavior of a Straight-Forward Amplifier with Compensation.

Figures 11 through 13 show the frequency response attained with a gain of 3.85 and the pulse response achieved with an input pulse rise time of 1.3ns of the open-loop amplifier illustrated in the diagram below. We call this open-loop amplifier a "straight forward amplifier."

With a quiescent current of 20mA and the applied component values, the –3dB bandwidth of the open-loop amplifier is between 350MHz at ±100mV and 460MHz at ±1.4V, depending upon the output voltage. See Table III.

The rise/fall time at the output is 1.4ns, and the maximum overshoot is under 10% and settles to less than 1% after 5ns. The settling time at 0.1%/10-bit is 25ns.

CURRENT-FEEDBACK AMPLIFIER

Advantages:

- Fewer transistor stages (signal delay time).
- Shorter signal delay time = larger bandwidth.
- Small-signal bandwidth independent of gain compensation of the frequency response possible with feedback resistance instead of capacitance.
- Complementary-symmetric circuit technique improves large-signal performance.

Disadvantages:

- Low-impedance inverting input.
- Asymmetric differential inputs.
- Low common-mode rejection ratio.
- Relatively high input offset voltage.

ADVANTAGES A CF-AMPLIFIER HAS WITH THE OPA660

The –3dB bandwidth stays constant over the entire modulation range up to ±2.5V and gains up to 12. Quiescent current control guarantees an excellent bandwidth /quiescent current ratio. See Figure 16.

R_Q varies the quiescent current to produce the necessary bandwidth. Feedback resistances can optimize frequency response over a broad range. This configuration also provides excellent pulse behavior, even up to large pulse amplitudes. Burr-Brown offers the Current-Feedback Amplifier completely assembled as a small demo board under the part number DEM-OPA660-2GC.

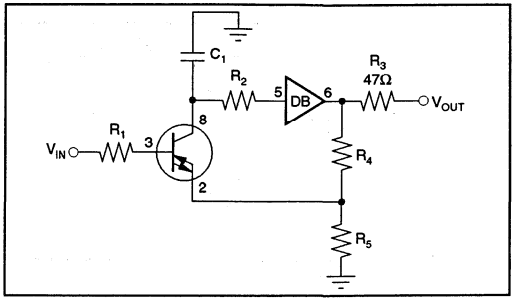


FIGURE 14. Current-Feedback Amplifier.

DIRECT-FEEDBACK AMPLIFIER

Another interesting basic circuit with the OPA660 is the so-called Direct-Feedback Amplifier, Figure 15. The idea of using voltage feedback from the collector to the emitter for Current-Conveyor structures was suggested for the first time a few years ago, and even in test configurations with simple Current-Conveyor structures, this design demonstrated excellent RF features. We named this structure the Direct-Feedback Amplifier, due to its short feedback loop across the complementary current mirror. As shown in detail with the Current-Feedback Amplifier, the open-loop gain of the Direct-Feedback Amplifier varies according to the closed-loop gain. This relation causes the product of the open-loop gain, V_O, and feedback factor, k_O, to stay constant, while the bandwidth also remains independent of the adjusted total gain. The currents at the emitter and collector always flow in the same direction. The current from the collector across R_3 causes an additional voltage drop in X_E and counteracts the base-emitter voltage. The reduced voltage difference, however, causes reduced current flow at the emitter and across the current mirror at the collector. It functions like double feedback and is adjusted by the ratio between R_3 and X_E. The Diamond Buffer decouples the high-impedance output.

Burr-Brown offers the Direct-Feedback Amplifier completely assembled as a small demo board under the part number DEM-OPA660-3GC.

Figures 17 and 18 show the excellent test results with the Direct-Feedback Amplifier.

Using a quiescent current of 20mA and the given component values and compensation at the emitter, it is possible to attain 330MHz at ±100mV and max 550MHz at ±1.4V bandwidth. The frequency response curve is extremely flat and shows peaking of 1dB only with output signals of ±2.5V. The voltage gain G is 3. The pulse diagrams shown here for small-signal modulation illustrate the excellent pulse response. There is no difference in pulse response between 300mVp-p and 5Vp-p.

The calculated slew rate is 2500V/µs during 5Vp-p signals. Previously, this slew rate could only be achieved using hybrid circuits with a quiescent current between 20mA and 500mA and a voltage supply of ±15V for ±2.5V signals. See Table IV.

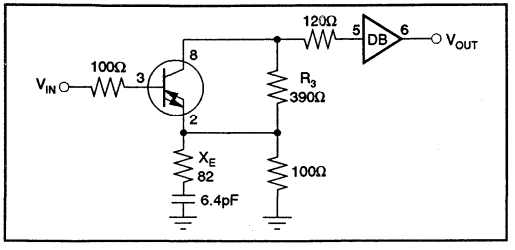


FIGURE 15. Direct-Feedback Amplifier.

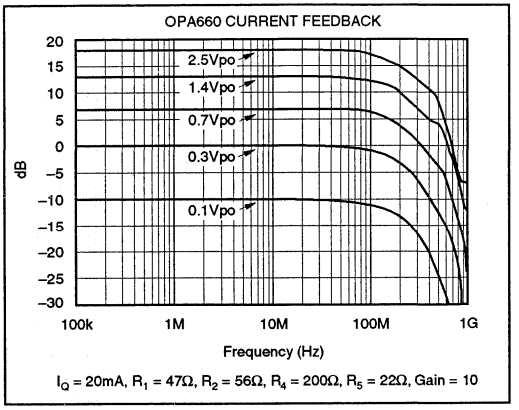


FIGURE 16. Current-Feedback Amplifier Frequency Response.

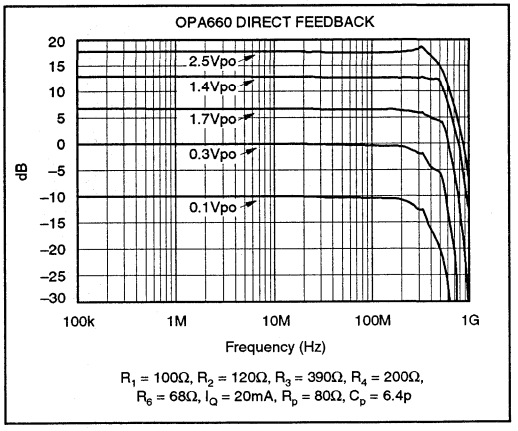


FIGURE 17. Direct-Feedback Amplifier Frequency Response.

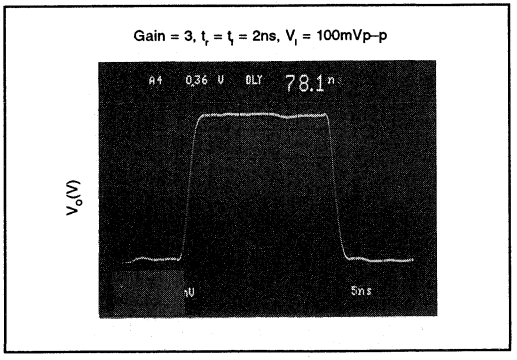


FIGURE 18. Pulse Behavior of the Direct-Feedback Amplifier.

V_{OUT}	f_{-3dB}
±100mV	331MHz
±300mV	362MHz
±700mV	520MHz
±1.4V	552MHz
±2.5V	490MHz

TABLE IV. –3dB Bandwidth vs Output Voltage.

FUNCTIONAL CIRCUITS WITH THE OPA660

- Driver Circuits for Diodes Capacitive/Inductive Loads
- Operational Amplifiers
- Line Drivers
- Integrators/Rectifier Circuits
- Receiver Amplifier for Pin Diodes
- Active Filters

The new circuit technology really comes into full use, however, in applications in which the current is the actual signal. Such applications include active filters with Current-Conveyor structures, control of LED and laser diodes, as well as control of tuning coils, driver transformers, and magnetic heads for analog and digital video recording.

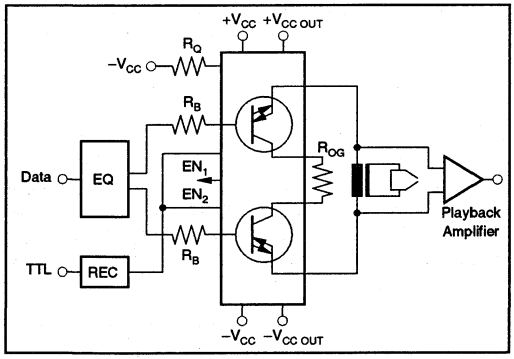


FIGURE 19. Video Record Amplifier.

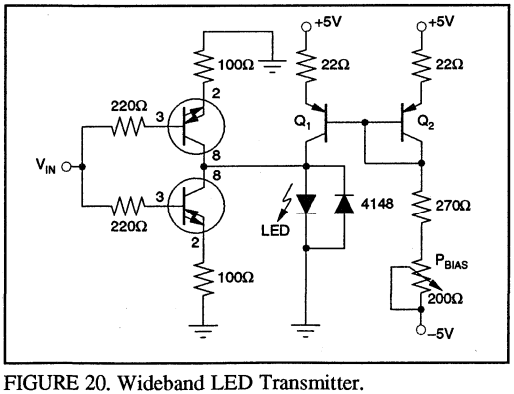


FIGURE 20. Wideband LED Transmitter.

VIDEO RECORD AMPLIFIER

A good way to see the advantages of current control over voltage control is to compare them when driving magnetic heads in video technology. Analog recording requires high linearity, while digital recording demands sharp edges and low phase distortion, since the zero crossing point contains the relevant information.

A special recording amplifier is necessary to drive the rotating video heads. This amplifier, Figure 19, delivers the current to magnetize the tape. The recording current can be between 1mA and 60mA, depending upon the amplitude, type of recording, and type of tape used. The current flowing through the video heads must be independent of the frequency and load. Current source control can deliver current through the load up to the rated output limit, independent of the voltage drop. In addition, the recording current is directly proportional to the magnetic field intensity and flux density. The record drive amplifier for digital signals shown here functions in a bridge configuration, in which the inverting and non-inverting digital data streams control the signal differentially. Bridge operation, and thus a doubled voltage range, is necessary because the voltage drop across the load inductance exceeds the voltage range of the Diamond Transistor at the 30MHz recording rate and maximum record current. The common emitter resistor allows simple adjustment of the transconductance.

In previous amplifiers, relays separated the replay and record amplifiers when switching from recording to replay. Using the OPA660 or the OPA2662, which contains two Diamond Transistors with high-current output stages, the I_Q (OPA660) or EN inputs (OPA2662) can switch the record drive amplifier into high-impedance mode. The gate in front of the output stage stops the digital data stream. In high-impedance mode, the output stage requires very little current.

DRIVER AMPLIFIER FOR LED TRANSMISSION DIODES

The advantages of current control also become apparent when driving light-emitting diodes and laser diodes in analog/digital telecommunications and in test procedures with modulated laser light. Using the OPA2662, it will be possible to control laser diodes by a complementary-bipolar current source; using the OPA660, it is already possible to control LEDs with ±30mA drive current. Figure 20 shows the circuit implementation. The quiescent current is 20mA max when R_Q = 220Ω, and the inputs of both emitter followers, which are not illustrated in the Figure, are grounded through 220Ω resistances, since these inputs are not necessary in this application. The current mirror consisting of Q_1 and Q_2 sets the quiescent current for the LED, which can then be adjusted by P_{BIAS}. Two Diamond Transistors wired parallel to each other deliver the signal current. Diamond Transistors can be connected to each other at the collector output to increase the output current, which has already increased to ±30mA in this configuration. The diode 4148 protects the transmitter diodes against excessive reverse voltages.

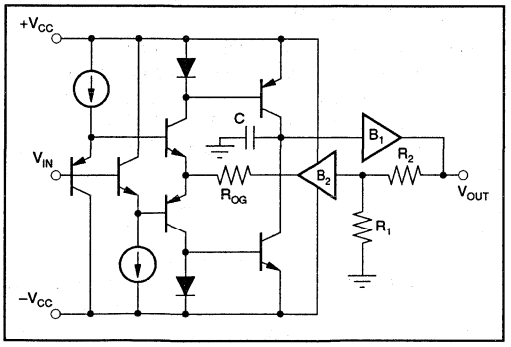


FIGURE 21. Voltage-Feedback Amplifier.

OPERATIONAL AMPLIFIER WITH VOLTAGE FEEDBACK IN DIAMOND STRUCTURE

The disadvantages of the Current-Feedback Amplifier listed above are unbalanced inputs, low-impedance inverting input, poor common-mode rejection ratio, and size of the input offset voltage. Now, we would like to present a concept which integrates the Diamond structure with voltage feedback in one circuit. An additional buffer transforms the current feedback of the Current Feedback Amplifier into voltage feedback. Figures 21 and 22 illustrate the circuit diagram and the extended Voltage-Feedback Amplifier. The feedback buffer is identical to the input section of the Diamond Transistor and forms one side of the differential amplifier, while the Diamond Transistor is the other side. Both buffer outputs are connected to R_{OG}, which determines the open-loop gain and corresponds to the emitter degeneration resistor of a conventional differential stage.

The output of this differential stage is the collector of the Diamond Transistor, which is driven in quasi open-loop mode due to the output buffer. Both inverting and non-inverting operations are possible. The ratio of the feedback resistances determines the closed-loop gain, and the user can attain optimum frequency response by adjusting the open-loop gain externally with R_{OG}. The frequency response of the differential amplifier is equivalent to that of a 2nd order low-pass Butterworth filter with gain. Due to the additional delay time in the control loop caused by the feedback buffer, the frequency response is poorer than the current feedback by 30%. The OPA622, which was recently introduced, contains a Diamond Transistor and two buffers. With the output current capability of ±100mA, this IC can drive several low-impedance outputs. The output buffer has its own supply voltage pins to decouple the output stage from differential stage and to enable external current limitation. Because of the identical high-impedance inputs, the typical offset voltage at the output is ±1mV, and the common-mode rejection ratio is over 70dB. These values are excellent results for RF amplifiers.

DRIVER AMPLIFIER FOR LOW-IMPEDANCE TRANSMISSION LINES

The ability of the Current-Feedback Amplifier to deliver ±15mA output current makes it a good choice as a driver amplifier for low-impedance (50Ω/75Ω) coaxial transmission lines. To transmit the pulse free of reflections, the transmission line must be terminated on both sides by the characteristic impedance of the line. A resistance in series to the output resistance of the driver amplifier, Figure 23, matches the output of the amplifier to the line. The total resistance of the output and series resistors should be equal to the characteristic impedance. The output resistance of operational amplifiers rises with increasing frequency. Thus, the impedances are no longer matched and reflections arise due to high-frequency components in the signal. The output resistance of Current-Feedback Amplifiers rises, for example, up to 25Ω at 50MHz.

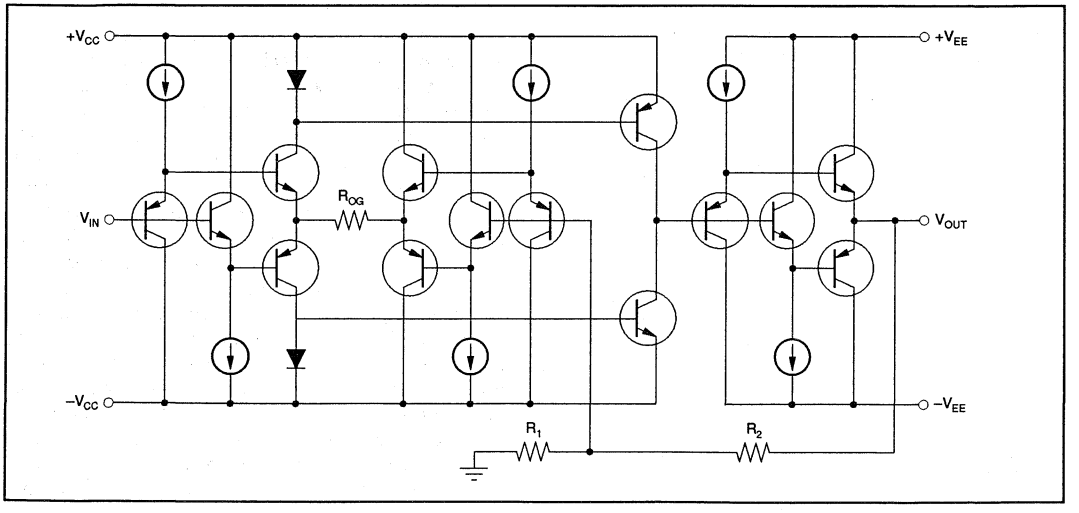


FIGURE 22. Extended Voltage-Feedback Amplifier.

DIFFERENTIAL OUTPUT

The circuit in Figure 24 is well suited to applications with larger dynamic ranges, which require a differential output to drive triax lines. A signal amplitude of ±5V is provided to drive a load which is not grounded. The load could be the input resistance of an RF device in an EMC contaminated environment. Resistances in series to each amplifier output match the output to the line. These resistances are selected at somewhat less than half of the characteristic impedance. While the rise/fall time and bandwidth do not change, the slew rate doubles.

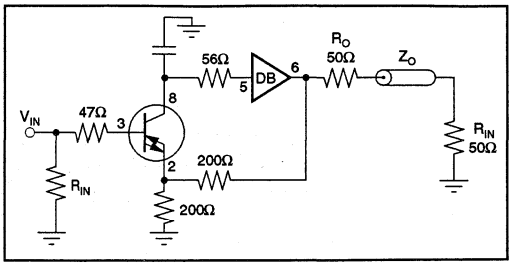


FIGURE 23. 50Ω Driver Amplifier.

MONOCHROMATIC MATRIX OR B/W HARDCOPY OUTPUT AMPLIFIER

The inverting amplifier in Figure 25 amplifies the three input voltages, which correspond to the luminance section of the RGB color signal. Different feedback resistances weight the voltages differently, resulting in an output voltage consisting of 30% of the red, 59% of the green, and 11% of the blue section of the input voltage. The way in which the signal is weighted corresponds to the transformation equation for converting RGB pictures into B/W pictures. The output signal is the black/white replay. It might drive a monochrome control monitor or an analog printer (hardcopy output).

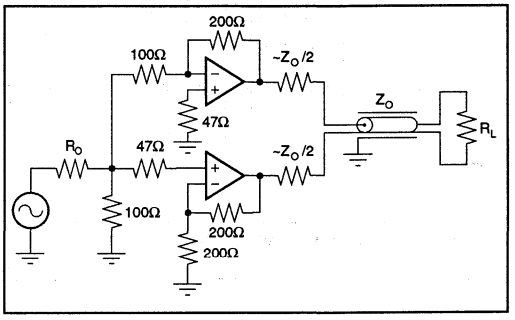


FIGURE 24. Balanced Driver.

OPERATIONAL TRANSCONDUCTANCE AMPLIFIER (OTA)

The Diamond Transistor and Diamond Buffer form a differential amplifier with two symmetric high-impedance inputs with current output. This amplifier is also known as the Operational Transconductance Amplifier, Figure 26. In this application, R_E sets the open-loop gain. The bipolar current output can be connected to a discrete cascode transistor, which enables wideband and high voltage outputs.

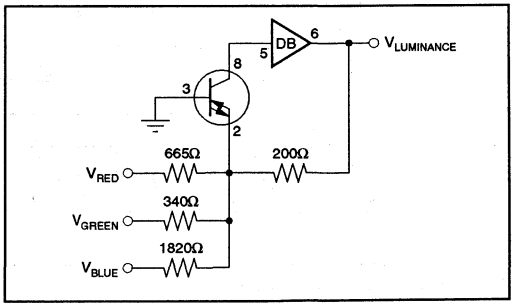


FIGURE 25. Monochrome Amplifier.

NANOSECOND INTEGRATOR

One very interesting application using the OPA660 in physical measurement technology is a non-feedback ns-integrator, Figures 27 and 28, which can process pulses with an amplitude of ±2.5V, have a rise/fall time of as little as 2ns, and pulse width of more than 8ns. The voltage-controlled current source charges the integration capacitor linearly according to the following equation:

$$V_C = V_{BE} \bullet gm \bullet t/C$$

V_C = Voltage At Pin 8
V_{BE} = Base-Emitter Voltage
gm = Transconductance
t = Time
C = Integration Capacitance

The output voltage is the time integral of the input voltage. It can be calculated from the following equation:

$$V_O = \frac{gm}{C}\int_0^T V_{BE}\, dt$$

V_O = Output Voltage
T = Integration Time
C = Integration Capacitance

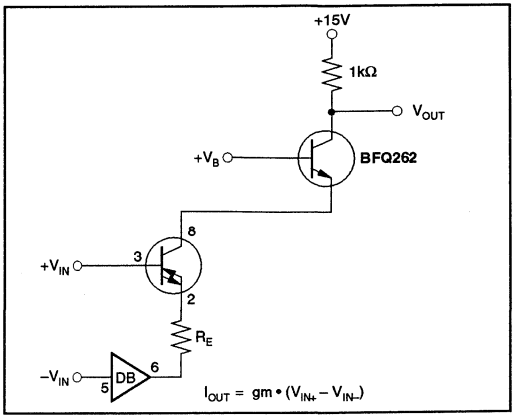


FIGURE 26. Operational Transconductance Amplifier.

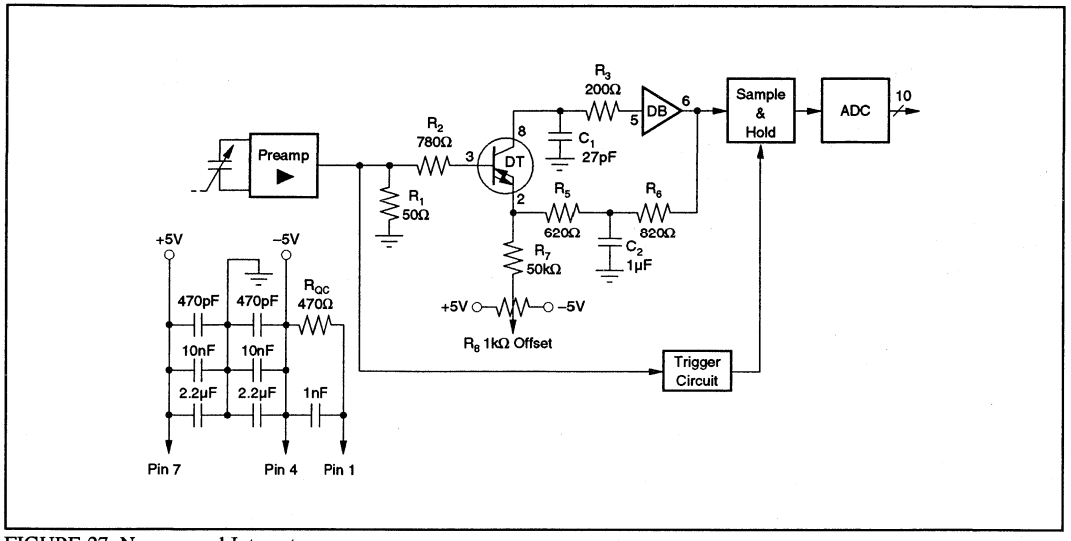


FIGURE 27. Nanosecond Integrator.

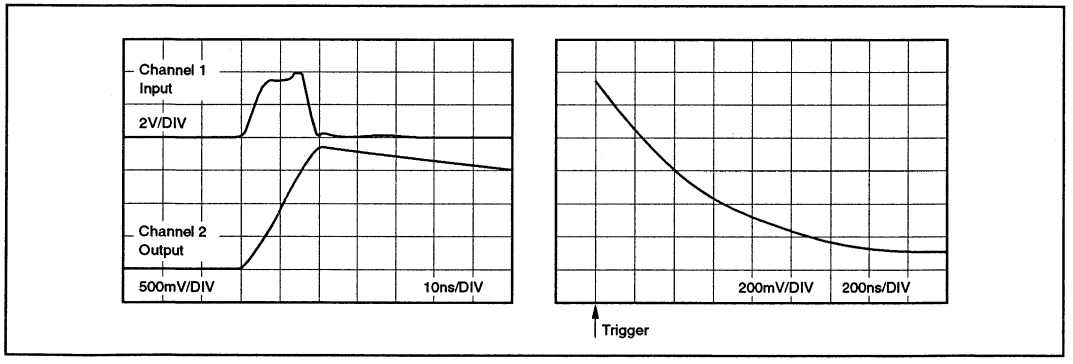


FIGURE 28. Integrator Performance.

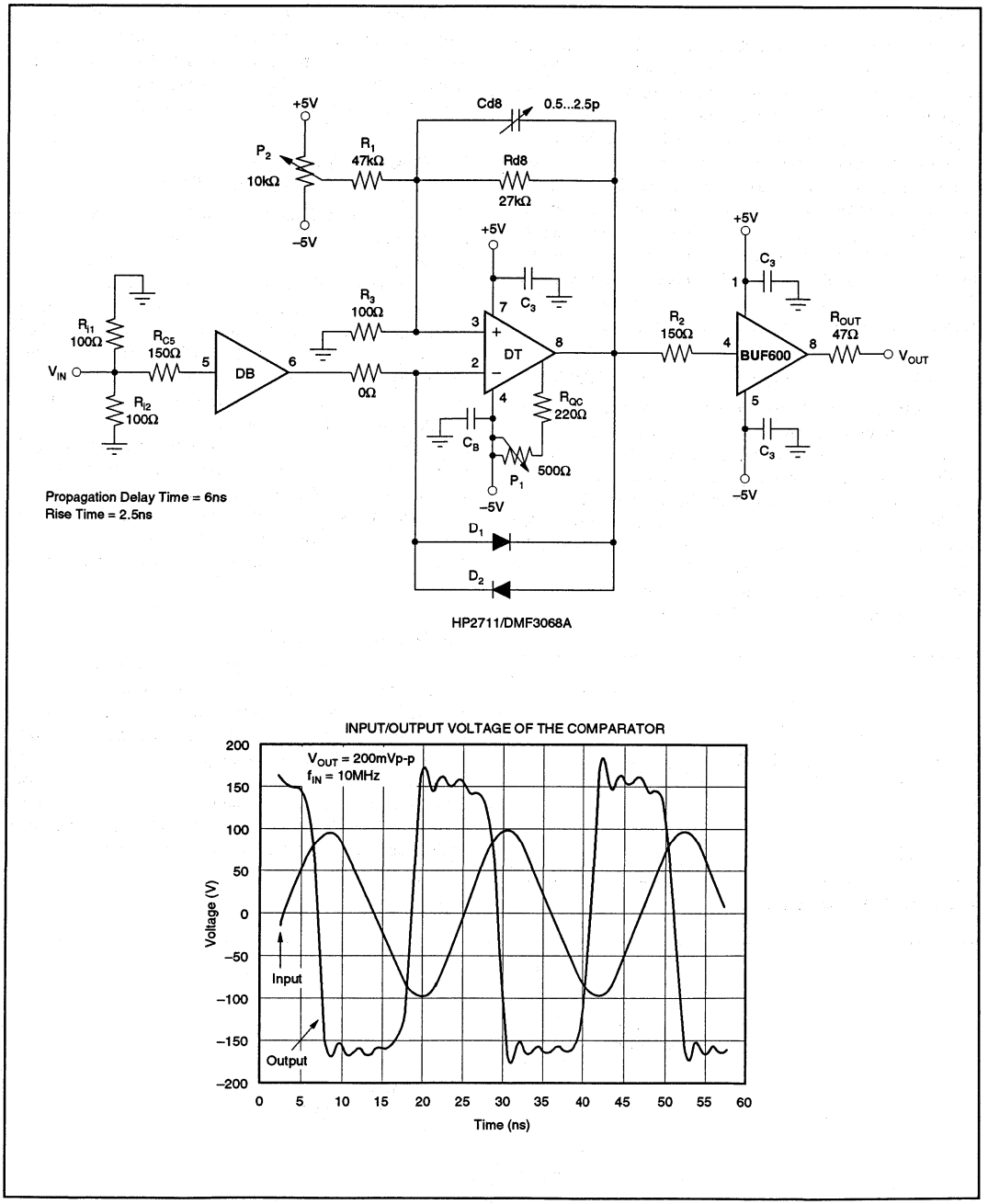


FIGURE 29. Comparator (Low Jitter).

COMPARATOR

An interesting and also cost effective circuit solution using the OPA660 as a low jitter comparator is illustrated in Figure 29. This circuit uses, at the same time, a positive and negative feedback. The input is connected to the inverting E-input. The output signal is applied in a direct feedback over the two antiparallel connected gallium-arsenide diodes back to the emitter. A second feedback path over the RC combination to the base, which is a positive feedback, accelerates the output voltage change when the input voltage crosses the threshold voltage. The output voltage is limited to the threshold voltage of the antiparallel diodes. The diagram on the right side of Figure 29 demonstrates the low jitter performance of the presented comparator circuit.

RECTIFIER FOR RF SIGNAL IN THE mV RANGE

Previously, rectifier diodes were included in the feedback loop of operational amplifier circuits to form ideal diodes for accurate detection of small signals in the mV range. In this configuration, the slew rate of the operational amplifier fixes the maximum frequency which can be rectified. The circuit in Figure 30 illustrates a new method of rectifying RF signals. The diodes at the current source output direct the current either into the load resistance or toward ground. The output current is zero even during zero crossing, resulting in a very soft transfer from one diode to the next.

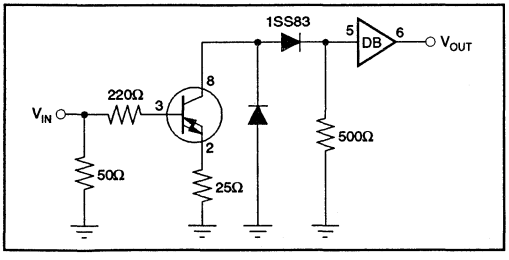


FIGURE 30. RF Rectifier.

The current source compensates for different voltage drops across the diodes up to its maximum rated voltage. It is possible to extend this circuit to a full-wave rectifier by connecting the second diode, instead to GND, over a resistor to GND, to rectify the negative half of the input signal.

CONTROLLING THE GAIN BY ADJUSTING THE BIAS CURRENT

The transfer curve of the Diamond Transistor demonstrates that the transconductance varies according to the quiescent current. The circuit, Figure 31, described here uses this relation to control the gain. As measurements have shown, it is possible to produce a gain range of 20dB, but the minimum quiescent current should not fall short of 1mA. Quiescent currents smaller than 0.5mA increase the non-linearities to a value which can no longer be tolerated. A positive current flowing into the I_Q-adjust (pin 1) disables the OPA660, the output of which goes into high-impedance state. The switch-on period lasts only a few ns, while the switch-off time is several µs. The internal capacitances are discharged at different speeds according to the load. The possibility of modulating the bias current dynamically has not yet been investigated. But based on the internal configuration, modulation frequencies up to several kHz should be possible.

PIN DIODE RECEIVER

Figure 32 illustrates a preamplifier which can recover both analog and digital signals for a fiber optic receiver. This preamplifier can amplify weak and noisy signal currents and convert them into voltage. In this arrangement, the Diamond Transistor operates in the inverting base configuration, which functions excellently in this application due to its low-impedance current input. In the ideal case, the voltage set at the base by the voltage divider appears at the low-impedance emitter free of offset errors. The voltage drop above the

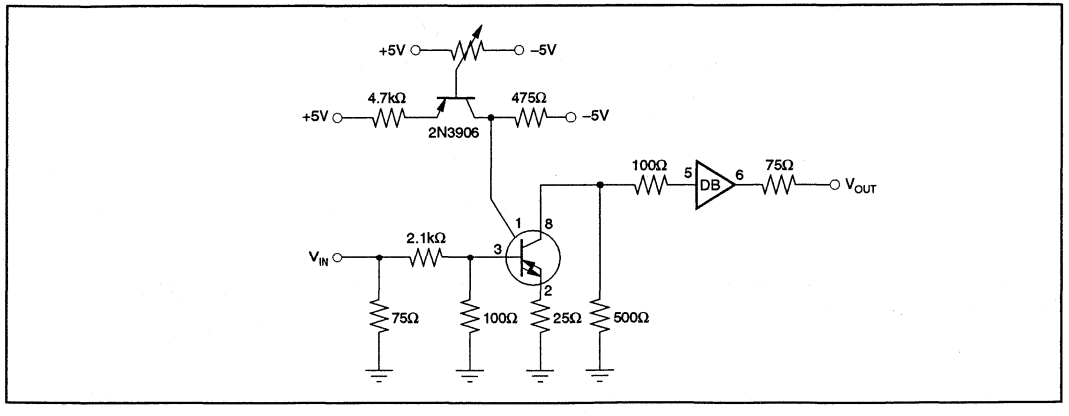


FIGURE 31. Controlled Amplifier.

diode is adjusted to zero volts. During exposure to light, the pin diode functions as a high-impedance current source and either delivers current to the emitter or removes current. The resulting voltage difference between the base and emitter controls the collector current. The current gain error is dependent both upon the dynamic output resistance of the pin diode and upon the transconductance of the Diamond Transistor. It is possible to achieve current gain factors of 200 to 400, depending upon the diode and quiescent current used. Advantages of this circuit structure include the following points:

- The transconductance and speed of the Diamond Transistor keep the voltage drop across the diode low, preventing the diode capacitance from increasing with the modulation.
- A fixed voltage across the diode improves the linearity, since the sensitivity of the diode varies with diode voltage.
- The capacitance at the emitter is only 2pF.
- The signal path is short, resulting in a very wide bandwidth.

ACTIVE FILTERS USING THE OPA660 IN CURRENT CONVEYOR STRUCTURE

One further example of the versatility of the Diamond Transistor and Buffer is the construction of active filters for the MHz range. Here, the Current Conveyor structure, Figure 33, is used with the Diamond Transistor as a Current Conveyor.

The method of converting RC circuit loops with operational amplifiers in Current Conveyor structures is based upon the adjoint network concept. A network is reversible or reciprocal when the transfer function does not change even when the input and output have been exchanged. Most networks, of course, are nonreciprocal. The networks, Figure 34, perform interreciprocally when the input and output are exchanged, while the original network, N, is exchanged for a new network N_A. In this case, the transfer function remains the same, and N_A is the adjoint network. It is easy to construct an adjoint network for any given circuit, and these networks are the base for circuits in Current-Conveyor structure. Individual elements can be interchanged according to the list in Figure 35. Voltage sources at the input become short circuits, and the current flowing there becomes the output variable. In contrast, the voltage output becomes the input, which is excitated by a current source. The following equation describes the interreciprocal features of the circuit: $V_{OUT}/V_{IN} = I_{OUT}/I_{IN}$. Resistances and capacitances remain unchanged. In the final step, the operational amplifier with infinite input impedance and 0Ω output impedance is transformed into a current amplifier with 0Ω input impedance and infinite output impedance. A Diamond Transistor with the base at ground comes quite close to an ideal current amplifier. The well-known Sallen-Key low-pass filter with positive feedback, Figure 36, is an example of conversion into Current-Conveyor structure. The positive gain of the operational amplifier becomes a negative second type of Current Conveyor (CCII), Figure 37. Both arrangements have identical transfer functions and the same level of sensitivity to deviations. The most recent implementation of active filters in a Current-Conveyor structure produced a second-order Bi-Quad filter. The value of the resistance in the emitter of the Diamond Transistor controls the filter characteristic.

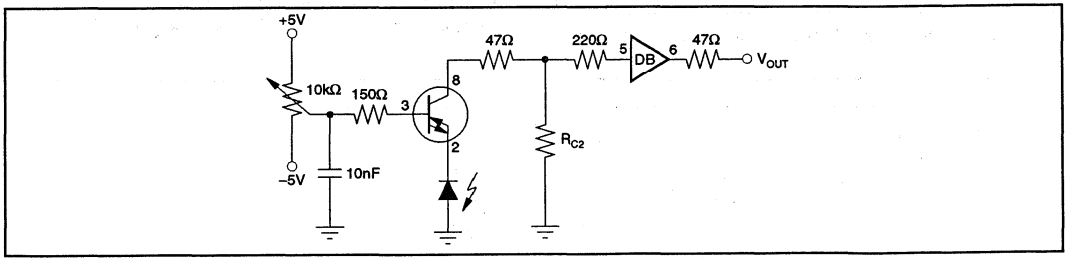


FIGURE 32. Preamplifier.

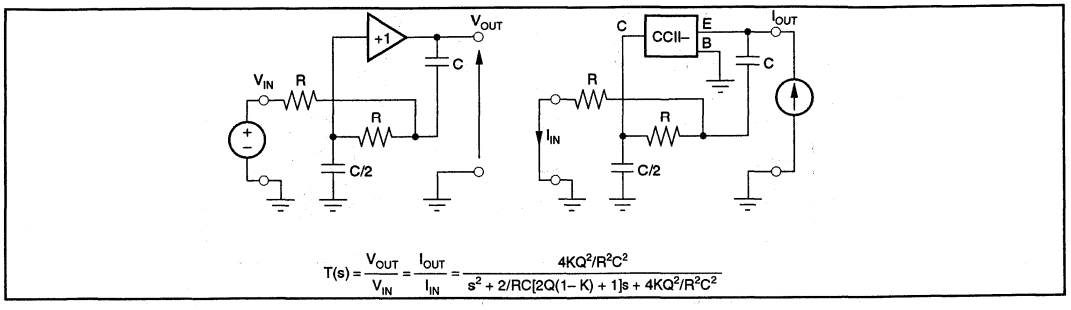


FIGURE 33. Current Conveyor.

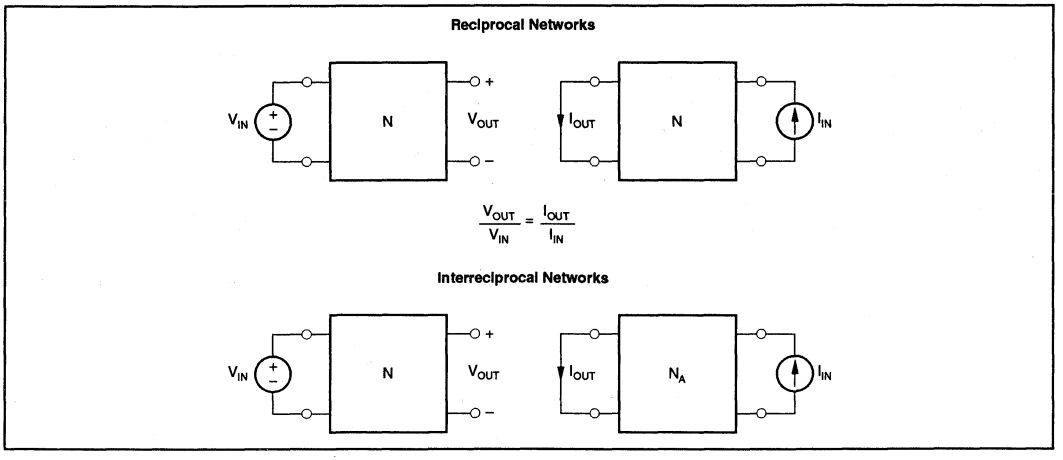


FIGURE 34. Networks.

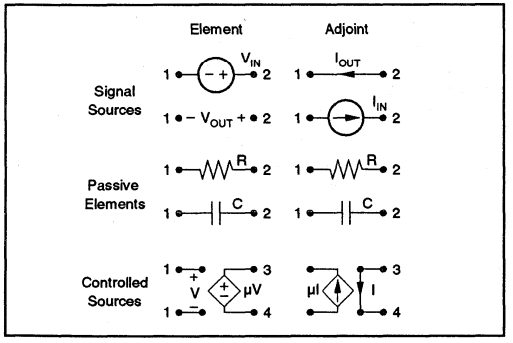


FIGURE 35. Individual Elements in the Current Conveyor.

TRANSFER FUNCTION

$$F(p) = \frac{V_{OUT}}{V_{IN}} = \frac{S^2 C_1 R_{1M} \frac{R_{2M}}{R_3} + sC_1 \frac{R_{1M}}{R_2} + \frac{1}{R_1}}{S^2 C_1 C_2 R_{1M} \frac{R_{2M}}{R_{3S}} + sC_1 \frac{R_{1M}}{R_{2S}} + \frac{1}{R_{1S}}}$$

FILTER CHARACTERISTICS

Low-pass filter:	$R_2 = R_3 = \infty$
High-pass filter:	$R_1 = R_2 = \infty$
Bandpass filter:	$R_1 = R_3 = \infty$
Band rejection filter:	$R_2 = \infty$; $R_1 = R_3$
All-pass filter:	$R_1 = R_{1S}$, $R_2 = R_{2S}$, $R_3 = R_{3S}$

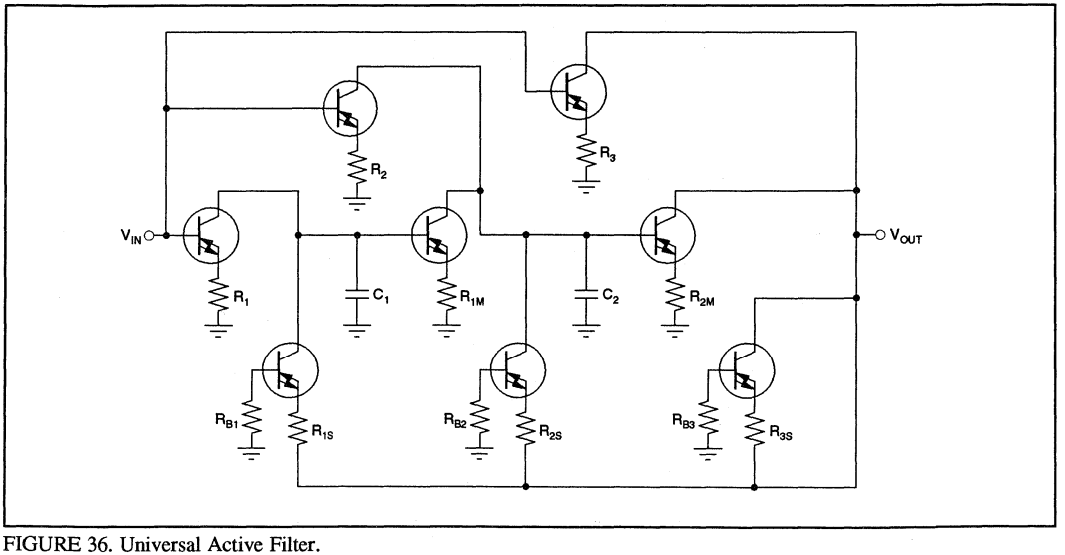


FIGURE 36. Universal Active Filter.

The design of a low-pass filter with a corner frequency of 30MHz results in the following values:

$R_{1M} = R_{2M} = 91\Omega$; $C_1 = C_2 = 100pF$
$R_1 = 142\Omega$; $R_{1S} = 161\Omega$; $R_{2S} = 140\Omega$; $R_{3S} = 426\Omega$

Figure 37 illustrates the frequency response and phase characteristics of the filter. Advantages of active filters in a Current Conveyor structure:

- The increase in output resistance of operational amplifiers at high frequencies makes it difficult to construct feedback filter structures (decrease in stop-band attenuation).
- All filter coefficients are represented by resistances, making it possible to adjust the filter frequency response without affecting the filter coefficients.
- The capacitors which determine the frequency are located between the ground and the current source outputs and are thus grounded on one side. Therefore, all parasitic capacitances can be viewed as part of these capacitors, making them easier to comprehend.
- The features which determine the frequency characteristics are currents, which charge the integration capacitors. This situation is similar to the transfer characteristic of the Diamond Transistor.

OPTIMATION WITH DIAMOND STRUCTURE

- AGC Amplifier
- DC-Restored Amp
- Analog Multiplexer
- PLL
- Sample/Hold
- Multiplier
- Oscillators
- RF-Instrumentaion Amplifiers

DYNAMIC OUTPUT IMPEDANCE INCREASE

As illustrated in Table II, the output impedance of the OTA at a quiescent current of ±20mA equals to 25kΩ || 4.2pF. The lower curve in the diagram on the right half of Figure 38 shows the behavior of the output impedance vs frequency. For some applications, like the integrator for ns-pulses of Figure 27, the relatively low output impedance is a real disadvantage. The fast discharge of the integration capacitor after (Figure 28) the pulse is over demonstrates this behavior. An easy way to improve the output impedance is a positive feedback path formed by the resistor divider from the collector to the base and the GND. The ratio of the two resistors determines the final output impedance, which can even be made negative. The capacitor between C and B supports the improvement vs frequency, which is illustrated in the diagram of Figure 38. The positive feedback results in a dynamic increase of the open loop gain, which can be made higher than 110dB.

DIFFERENTIATOR FOR WEAK AND DISTURBED DIGITIZED SIGNALS

As it is shown in Figure 39 a RC network can be connected between the E-output of the OTA and buffer output. The proposed circuit improves the pulse shape of digitized signals coming from a magnetic tape or a hard disc drive.

CONTROL LOOP AMPLIFIER

A new type of control loop amplifier for fast and precise control circuits can be designed with the OPA660. The circuit of Figure 40 shows a series connection of two voltage control current sources which have an integral and at higher frequencies a proportional behavior vs frequency. The control loop amplifiers show an integrator behavior from DC to the frequency, represented by the RC time constant of the network from the C-output to GND. Above this frequency they operate as an amp with constant gain. The series connection increases the overall gain to about 110dB and thus minimizes the control loop deviation. The differential configuration at the inputs enables one to apply the measured output signal and the reference voltage to two identical high-impedance inputs. The output buffer decouples the C-output of the second OTA in order to insure the AC-performance and to drive subsequent output stages.

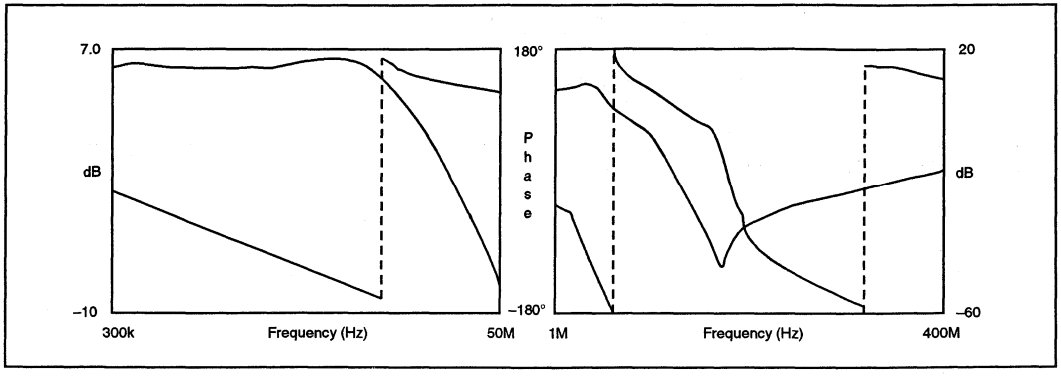


FIGURE 37. Current Conveyor LP.

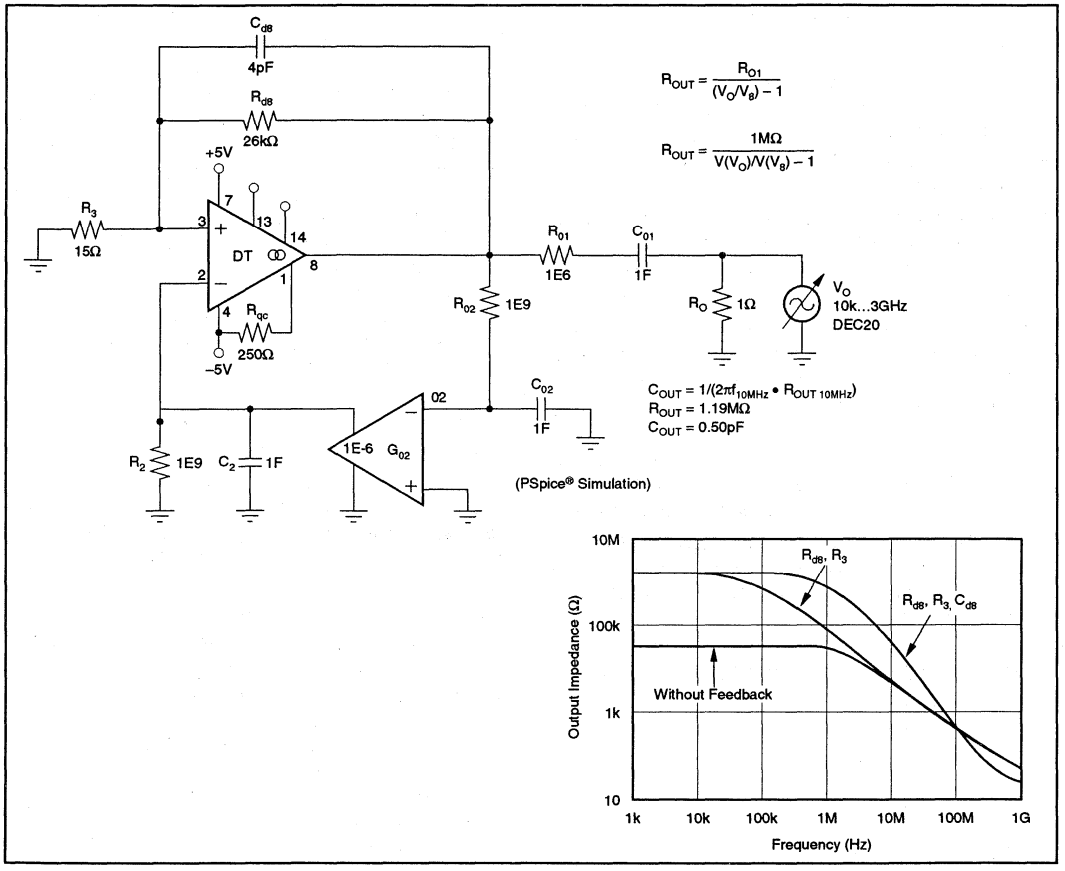


FIGURE 38. Transconductance Output Impedance (Dynamic increase with positive feedback).

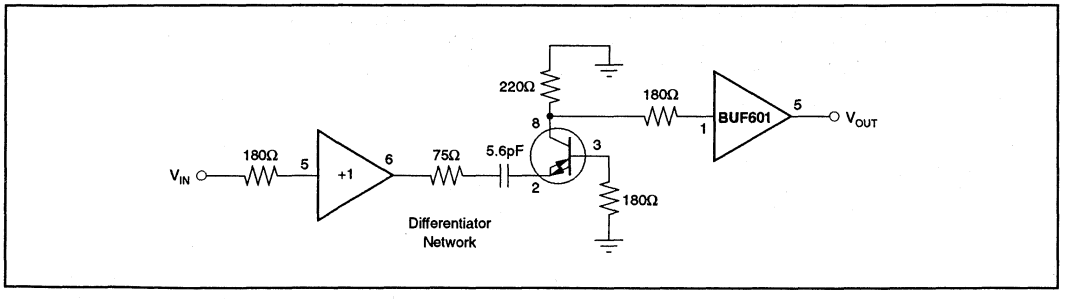


FIGURE 39. Differentiator for Digitized Video Signals.

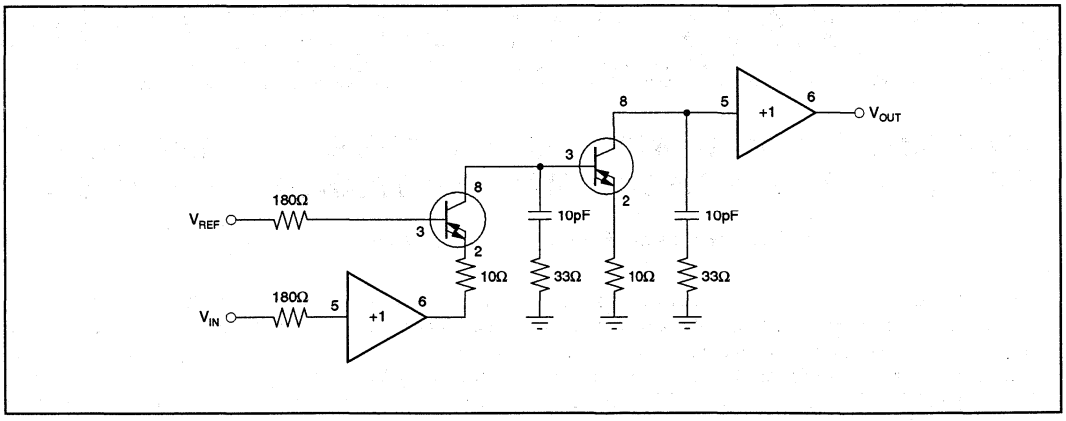


FIGURE 40. Control Loop Amplifier.

BURR-BROWN® APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

BUILDING A 400MHz WIDE-BAND DIFFERENTIAL AMPLIFIER: IT'S A BREEZE WITH THE DIAMOND TRANSISTOR OPA660.

By Christian Henn and Ernst Rau, Burr-Brown International GmbH

In radio frequency (RF) technology, signals from oscilloscopes, monitors, transient recorders, and many other devices are usually connected to sensors and generators via coaxial lines. In any transmission, however, interference voltages caused by differences in potential between the sender and receiver and by electromagnetic interference distort the results, particularly when the signals being transmitted are sensitive and wide-band. Designers of this type of transmission system need shielded, symmetrical transmission lines and input differential amplifiers with high common-mode rejection, which bring home the signals without humming or radio interference.

Designing this type of differential amplifier used to be quite a chore, involving extensive and complicated hardware. But the development of new, monolithic ICs such as the Diamond Transistor OPA660 has changed all that. The OPA660 makes it easy to design a 400MHz differential amplifier offering –60dB common-mode rejection at a 1MHz frequency. This amplifier uses an open-loop amplifier structure with two identical high-impedance inputs and no feedback. The parameters such as wide bandwidth, stable operation, and excellent pulse processing, common-mode rejection, and harmonic distortion let the performance speak for itself.

BASIC TRANSMISSION STRUCTURES

Figure 1 shows a symmetrical transmission path with signal voltage V_S and cable termination resistors R_{IN} and R_t. A symmetrical voltage source normally uses amplifiers with complementary outputs or transformers to balance or adapt the circuits. The relatively high-impedance input resistor R_b limits the input potential drift through the input bias currents (I_{BIAS}), and the symmetrical differential amplifier input rejects interference voltages superimposed upon the input signal and its reference potential. The voltage-controlled current source converts the symmetrical input voltage V_{IN} either into an output current or into the asymmetrical output voltage V_{OUT} when a voltage drop is present at the external resistor R_{OUT}. V_{IN} and V_{OUT} are related as follows: $V_{OUT} = V_{IN} \bullet gm \bullet R_{OUT}$, where gm is the transconductance of the operational transconductance amplifier (OTA). The buffer following the input amplifier decouples the low-impedance load resistor from the high-impedance OTA output.

Instead of symmetrical signal excitation, many applications use the type of transmission path shown in Figure 2. A single-ended signal voltage V_{IN} drives an asymmetrical coaxial cable terminated on both sides. In this structure as well, the symmetrical differential amplifier input rejects interference voltages superimposed on the signal.

INSTRUMENTATION AMPLIFIER WITH FEEDBACK

OTAs and buffers have conventionally been designed using differential amplifiers as shown in Figure 3. The feedback path from the op amp output over R_4 generates a relatively low-impedance inverting input, which is equal to the R_3 resistor value. Inserting the buffer amplifier, BUF2, converts the low-impedance input to high impedance, while inserting the buffer amplifier, BUF1, optimizes the input symmetry and thus the common-mode rejection at DC and vs frequency.

The gain is R_4/R_3 during signal excitation at the inverting input and $1 + R_4/R_3$ during signal excitation at the noninverting input. A divider is inserted between R_1 and R_2 to compensate for these differing gains. Buffer 1 also synchronizes the signal delay times of the two inputs, which is important for good common-mode rejection at high frequencies. To achieve high common-mode rejection over frequency, it is important that the gain curve of the two input buffers be as identical as possible.

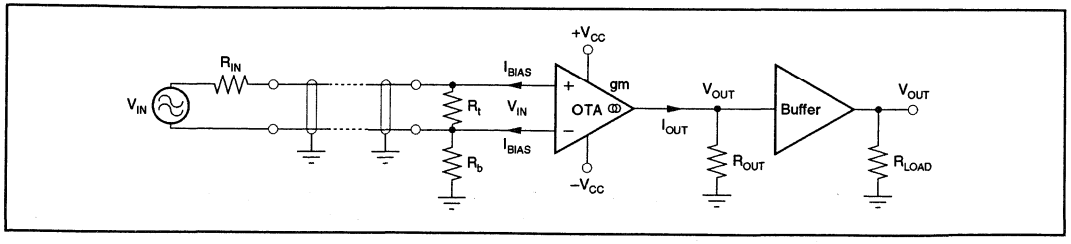


FIGURE 1. Basic Structure of a Symmetrical Transmission Path.

In addition to requiring more hardware, this type of system also has smaller bandwidth than the open-loop amplifier shown in Figure 2 due to the delay time in its amplifier feedback loop (phase shift).

A SYNTHESIS: OPEN-LOOP AMPLIFIER USING THE DIAMOND TRANSISTOR

The open-loop amplifier using the Diamond Transistor OPA660 and buffer amplifier BUF601 combines the best of both worlds, offering better bandwidth than a normal open-loop amplifier, excellent pulse responses down to rise/fall times of 1ns, and reduced hardware. The basic concept is shown in Figure 4.

The gain can be determined according to the following equation:

$$V_{OUT} = V_{IN} \frac{R_{OUT}}{R_E + 2/gm}$$

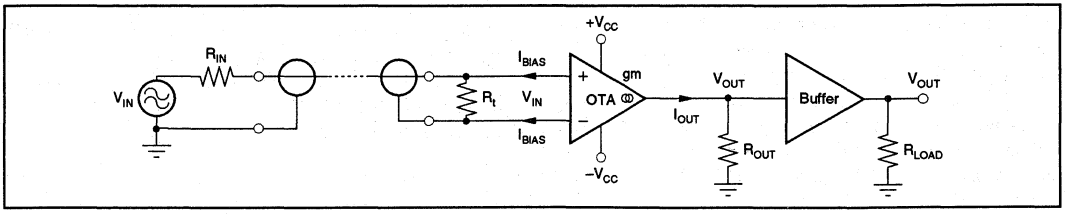


FIGURE 2. Signal Transmission Using an Asymmetrical Coaxial Cable and a Signal Voltage Referred to Ground.

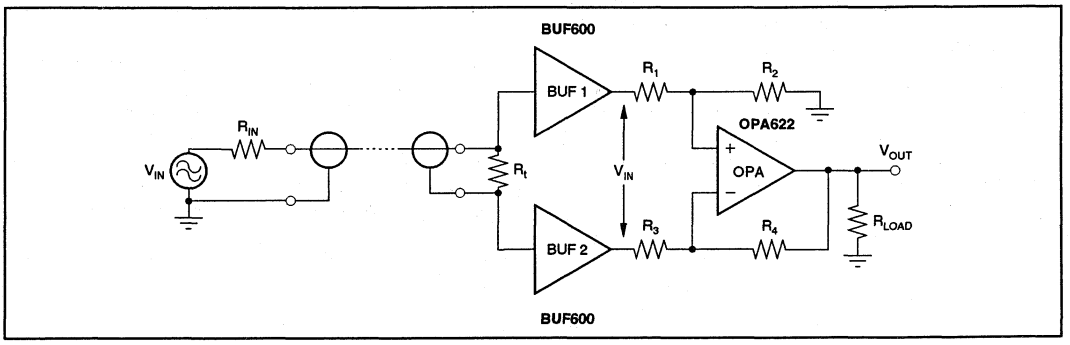


FIGURE 3. Instrumentation Amplifier with Feedback.

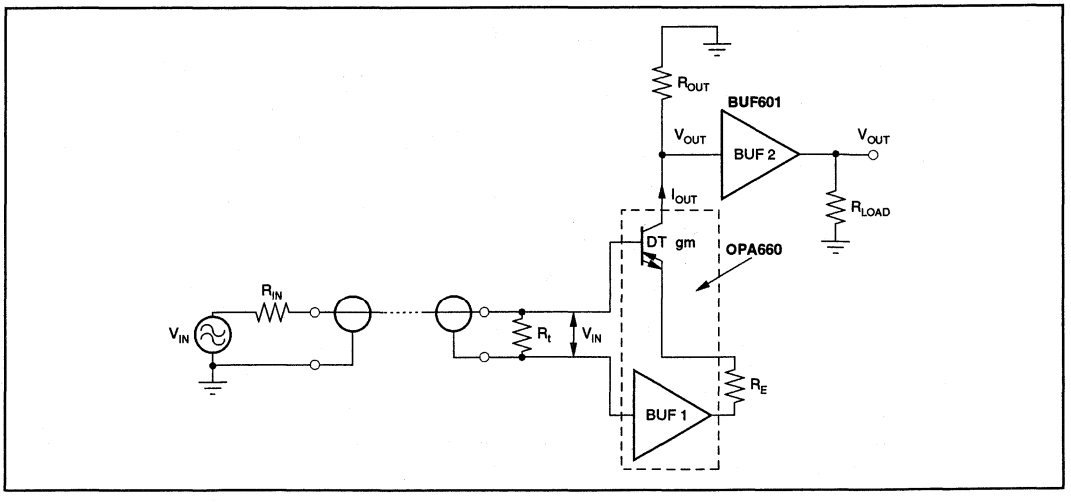


FIGURE 4. Wide-Band Open-Loop Amplifier.

Since the actual symmetrical structure of the circuit layout greatly effects the bandwidth and common-mode rejection, a demo board was used to determine the characteristic transmission parameters that this configuration shows in practice. Figure 5 illustrates the demo board in detail. The silkscreen and layout tips can be extremely useful in designing your own layouts.

The OPA660 contains a transconductance amplifier nicknamed the Diamond Transistor and a buffer called the Diamond Buffer in an 8-pin package. The Diamond Transistor itself consists of a buffer identical to the Diamond Buffer, followed by a current mirror. On the output side, the buffers are connected to each other via the resistor R_8, forming the differential input stage. When the input voltage is differential, a current flows through R_8, is reflected in high-impedance form to Pin 8, and produces the output voltage at R_9. To drive low-impedance transmission lines or input resistors, the buffer amplifier BUF601 decouples the relatively high-impedance output of the differential amplifier. Both inputs and the output are laid out for 50Ω systems, but they can also be adapted to other characteristic impedances by replacing the resistors R_3, R_7, and R_{11}. Capacitor C_5 parallel to R_8 compensates the parasitic capacitor at Pin 8 of the OPA660, thus expanding the achievable bandwidth.

The resistors, R_4, R_6, and R_{10}, located at the front of the circuit in series to the high-impedance inputs, make it possible to set the frequency response at the end of the bandwidth for a flat response. The quiescent current of the OPA660 is ±20mA at an R_{16} of 560Ω.

TEST RESULTS

The amplifier stage is set to a gain of +4 at an R_9 of 240Ω and R_8 of 43Ω. The total gain from input to output, including the output divider R_{11}/R_L, is +2. Figure 6 illustrates the frequency response of the two inputs In+ and In–. The –3dB frequency (fg) is 400MHz. Figure 7 shows the impact of the capacitor C_5 on the bandwidth.

The common-mode gain over frequency curve shown in Figure 8 demonstrates the rejection of interference voltages on both input voltages. The interference remains less than –18dB over the entire bandwidth, starting at a common-mode gain of –68dB. While the 400MHz differential amplifier amplifies differential signals by 4, the common-mode noise of the same frequency that appears at the output is multiplied only by 0.125. Table I lists the common-mode gain for several frequency levels.

f_{IN}	CG
1MHz	–60dB
10MHz	–45dB
100MHz	–23dB

TABLE I. Several Common-Mode Gains.

The harmonic distortions shown in Figure 9 and Table II for two different output voltages over frequency are outstanding parameters for a 400MHz differential amplifier and prove that the OPA660 and BUF601 provide excellent reproduction of wide-band input signals even without feedback. Furthermore, the low noise voltage density of 7.7nV/√Hz makes it possible to process even very small signals.

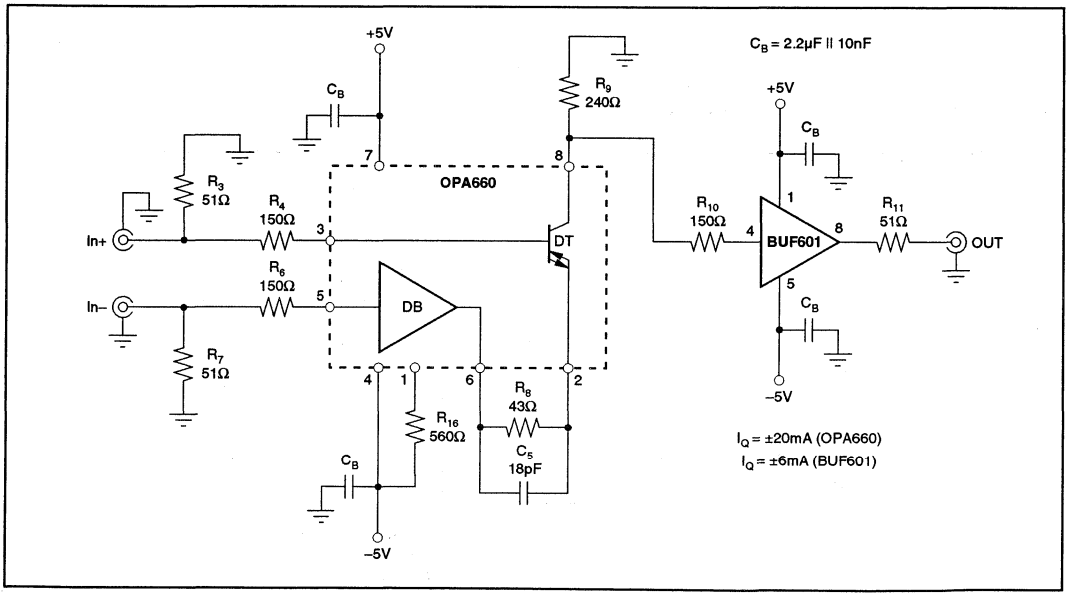


FIGURE 5. Circuit Diagram of the Demo Board.

HIGH PROCESSING POWER, LOW POWER REQUIREMENTS

The most important job of a differential amplifier is to reject common-mode interference arising during the transmission of analog signals. The 400MHz differential amplifier using the OPA660 impressively demonstrates how easy it now is to design wide-band input amplifiers for test devices, monitors, transient recorders, and other RF devices. While achieving excellent parameters for bandwidth, common-mode rejection, and frequency response, the OPA660 and BUF601 also offer such low power consumption that the entire differential amplifier can be powered from a separate battery supply—a truly compact, high-performance alternative.

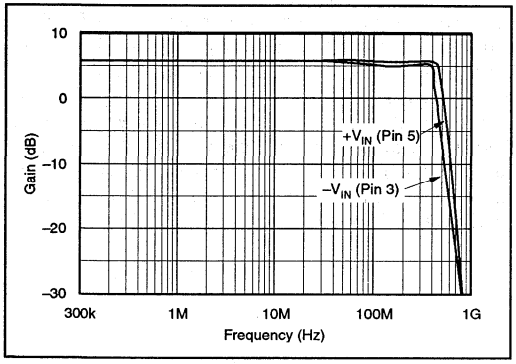


FIGURE 6. Frequency Responses of the Inputs In+ and In–.

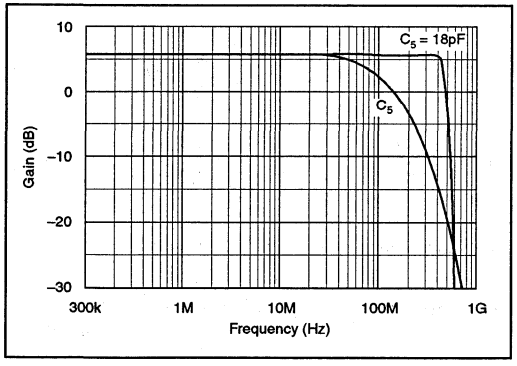


FIGURE 7. Impact of Capacitor C_S on the Bandwidth.

f	V_{OUT}	HARMONIC DISTORTION
10MHz	1Vp-p 1st Harmonic	–61dB
10MHz	1Vp-p 2nd Harmonic	–64dB
10MHz	2Vp-p 1st Harmonic	–57dB
10MHz	2Vp-p 2nd Harmonic	–55dB

TABLE II. Harmonic Distortion.

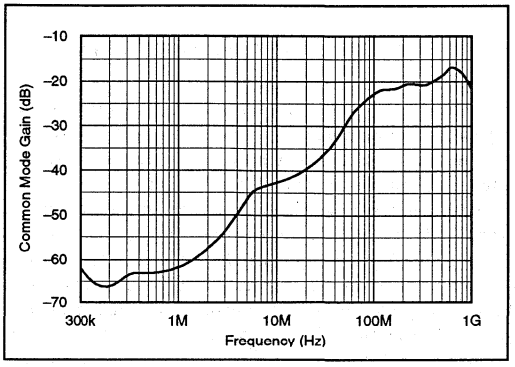


FIGURE 8. Common-Mode Gain.

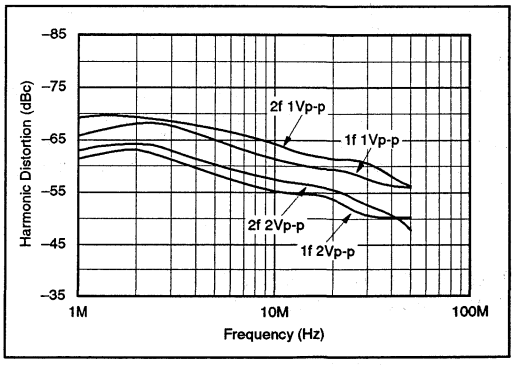


FIGURE 9. Harmonic Distortion.

BURR-BROWN® APPLICATION BULLETIN

Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

DESIGNING ACTIVE FILTERS WITH THE DIAMOND TRANSISTOR OPA660

Part 1

By Christian Henn and Klaus Lehman, Burr-Brown International GmbH

Signal frequency bandwidth limitation, fast pulse shaping, separation between telecommunications signals, and suppression of unwanted carrier and disturbance frequencies are among the most important jobs of filter circuits. While active filters with operational amplifiers and switched capacitor filters are used for lower frequency applications, passive filter versions dominate the application spectrum at frequencies above 5MHz. Now, however, a new active filter design has been developed that makes use of the open loop pole and delay time of an operational amplifier. The filter circuits consist of OPA660s, which provide the necessary bandwidth and allow access to the first open-loop pole and internal amplifier delay time. After presenting an overview of conventional filter circuits using 2nd, 3rd, and 5th order active filters with Tschebyscheff approximation, this Application Note will discuss the new filter structure in detail.

The filter circuits presented in Part One are optimized for the minimum possible number of components, while the filter circuits that will be analyzed in Part Two require more components, and board space, but are optimized for easy adjustment of the important filter parameters.

1.0 2ND ORDER LOW-PASS FILTER USING OPERATIONAL AMPLIFIERS

1.1 2nd Order Low-Pass Filter With An Ideal Op Amp

Figure 1 shows a classical example of an active 2nd order low-pass filter designed using an op amp. In this example, the op amp, IOPA, is assumed to be ideal.

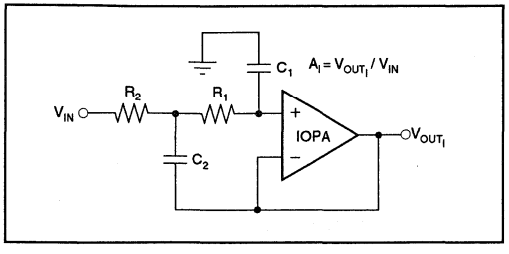


FIGURE 1. 2nd Order Low-Pass Filter Using an Ideal Op Amp.

Equation 1 can be derived from Figure 1 and describes the filter transfer function. In the following analyses, all parameters are assumed to be normalized to the –3dB frequency, ω_g, at which the amplitude $|A_I|$ is reduced to –3dB. When normalized to the –3dB frequency, Equation 1 becomes Equation 2. Technical literature about passive filters commonly uses the coefficients a_i and b_i (or a_i or b_i). Equation 3 is the result of comparing these coefficients and shows their relation to the circuit parameters τ_1 and τ_2. The coefficients ω_{0i} (or ω_{0i}) and Q_i (or Q_i) are easier to calculate and explain using circuit elements. Equation 4 shows these coefficients and those of a_i and b_i (or a_i and b_i).

$$A_I = \left[1 + j\omega \bullet (2\tau_1) + (j\omega)^2 \bullet (\tau_1\tau_2)\right]^{-1} \quad (1)$$

$$A_I = \left[1 + j\frac{\omega}{\omega_g} \bullet (2\tau_1\omega_g) + \left(j\frac{\omega}{\omega_g}\right)^2 \bullet (\tau_1\tau_2\omega_g^2)\right]^{-1} \quad (2)$$

$$A_I = \left[1 + j\frac{\omega}{\omega_g} \bullet a_1 + \left(j\frac{\omega}{\omega_g}\right)^2 \bullet b_1\right]^{-1} \quad (3)$$

$$A_I = \left[1 + j\frac{\omega}{\omega_g} \bullet \frac{1}{Q_1(\omega_{01}/\omega_g)} + \left(j\frac{\omega}{\omega_g}\right)^2 \bullet \frac{1}{(\omega_{01}/\omega_g)^2}\right]^{-1} \quad (4)$$

These equations can be rearranged, resulting in:

$$a_1 = 2\tau_1\omega_g = \frac{1}{Q_1(\omega_{01}/\omega_g)}; b_1 = \tau_1\tau_2\omega_g{}^2 = \frac{1}{(\omega_{01}/\omega_g)^2} \quad (5)$$

Rearranging Equation 5 gives dimensioning rules for the active filter circuit shown in Figure 1:

$$\tau_1 = \frac{1}{2Q_1(\omega_{01}/\omega_g)\omega_g}; \tau_2 = \frac{2Q_1}{(\omega_{01}/\omega_g)\omega_g} \quad (6)$$

The values for Q_i and $\omega_{0i}/\omega_g = f_{0i}/f_g$ can be found in Tables I to V for the various passband ripple specs and for filter orders from 1 to 4.

STATUS		DESIGN				TEST AND ADJUST		
I	f_p/f_g	AI	BI	f_{oi}/f_g	Q_i	f_{gi}/f_g	f_{xi}/f_g	IHXII
1	0.152620	1.000000	0.000000	1.000000	—	1.000000	—	—
1	0.509545	1.404882	1.162191	0.927601	0.767360	1.000000	0.360303	0.100000
1	0.719945	1.432831	0.000000	0.697919	—	0.697919	—	—
2	—	0.796864	1.141772	0.935859	1.340928	1.308626	0.795164	3.198263
1	0.821643	2.402002	2.377929	0.648486	0.618801	0.557823	—	—
2	—	0.483444	1.113711	0.947575	2.182931	1.417296	0.896485	7.014844
1	0.881276	2.105565	0.000000	0.474932	—	0.474932	—	—
2	—	1.555941	2.024763	0.702769	0.914522	0.854957	0.445671	0.766191
3	—	0.316283	1.077536	0.963350	3.282011	1.472181	0.940726	10.42479
1	0.913549	3.558215	4.549720	0.468822	0.599460	0.387303	—	—
2	—	0.985106	1.720656	0.762347	1.331570	1.064307	0.645976	3.147338
3	—	0.222328	1.060948	0.970852	4.632900	1.496039	0.959477	13.36794
1	0.936329	2.834566	0.000000	0.352788	—	0.352788	—	—
2	—	2.195827	3.454179	0.538056	0.846397	0.624395	0.295713	0.415494
3	—	0.666183	1.514331	0.812624	1.847213	1.196561	0.750728	5.660789
4	—	0.163930	1.044104	0.978652	6.233234	1.513678	0.972334	15.92230

TABLE I. Passband Ripple, P = 0.1dB.

STATUS		DESIGN				TEST AND ADJUST		
I	f_p/f_g	AI	BI	f_{oi}/f_g	Q_i	f_{gi}/f_g	f_{xi}/f_g	IHXII
1	0.327091	1.000000	0.000000	1.000000	—	1.000000	—	—
1	0.586283	1.394652	1.234406	0.900059	0.796642	1.000000	0.414565	0.200000
1	0.779147	1.575499	0.000000	0.634720	—	0.634720	—	—
2	—	0.739619	1.165269	0.926375	1.459503	1.318092	0.810393	3.826278
1	0.859762	2.568461	2.752149	0.602787	0.645897	0.546179	—	—
2	—	0.436287	1.128618	0.941297	2.435013	1.418697	0.900734	7.917111
1	0.909791	2.382160	0.000000	0.419787	—	0.419787	—	—
2	—	1.469586	2.163607	0.679846	1.000908	0.865129	0.481160	1.254646
3	—	0.280509	1.081198	0.961717	3.706857	1.475016	0.944058	11.45986
1	0.933323	3.718489	5.417686	0.429629	0.625951	0.374863	—	—
2	—	0.894401	1.780075	0.749516	1.491718	1.070693	0.659959	3.991311
3	—	0.195864	1.065000	0.969003	5.268903	1.496012	0.960237	14.47369
1	0.952210	3.238203	0.000000	0.308813	—	0.308813	—	—
2	—	2.091516	3.758594	0.515807	0.926940	0.632143	0.333514	0.834338
3	—	0.592804	1.539416	0.805976	2.092989	1.201365	0.758586	6.670542
4	—	0.143584	1.044744	0.978352	7.118671	1.514831	0.973513	17.06946

TABLE II. Passband Ripple, P = 0.2dB.

STATUS		DESIGN				TEST AND ADJUST		
I	f_p/f_g	AI	BI	f_{oi}/f_g	Q_i	f_{gi}/f_g	f_{xi}/f_g	IHXII
1	0.267431	1.000000	0.000000	1.000000	—	1.000000	—	—
1	0.632596	1.383913	1.291188	0.880046	0.821081	1.000000	0.447312	0.300000
1	0.813628	1.685318	0.000000	0.593360	—	0.593360	—	—
2	—	0.699249	1.178457	0.921177	1.552476	1.324872	0.820079	4.296095
1	0.880317	2.604074	3.023945	0.575060	0.667780	0.541312	—	—
2	—	0.405955	1.138083	0.937374	2.627901	1.418992	0.902803	8.552317
1	0.925452	2.590454	0.000000	0.386033	—	0.386033	—	—
2	—	1.403876	2.247589	0.667024	1.067898	0.871851	0.499850	1.645308
3	—	0.258290	1.082606	0.961092	4.028354	1.477015	0.946169	12.16998
1	0.943675	3.797733	6.042962	0.406794	0.647292	0.369527	—	—
2	—	0.834824	1.814592	0.742353	1.613595	1.074126	0.667278	4.594292
3	—	0.179775	1.067584	0.967830	5.747404	1.495732	0.960477	15.22243
1	0.960769	3.540230	0.000000	0.282468	—	0.282468	—	—
2	—	2.007356	3.943811	0.503549	0.989313	0.637414	0.352175	1.187620
3	—	0.546919	1.552727	0.802514	2.278372	1.204173	0.762886	7.366854
4	—	0.131337	1.044759	0.978345	7.782533	1.515687	0.974298	17.84038

TABLE III. Passband Ripple, P = 0.3dB.

STATUS		DESIGN				TEST AND ADJUST		
I	f_p/f_g	AI	BI	f_o/f_g	Q_I	f_{pi}/f_g	f_{xi}/f_g	IHXII
1	0.310609	1.000000	0.000000	1.000000	—	1.000000	—	—
1	0.665456	1.372811	1.339700	0.863965	0.843127	1.000000	0.470548	0.400000
1	0.837887	1.779279	0.000000	0.562025	—	0.562025	—	—
2	—	0.667162	1.187067	0.917830	1.633076	1.330380	0.827331	4.687601
1	0.893939	2.621387	3.244945	0.555132	0.687183	0.539051	—	—
2	—	0.383191	1.145162	0.934473	2.792661	1.418897	0.904021	9.061859
1	0.936086	2.766593	0.000000	0.361455	—	0.361455	—	—
2	—	1.349474	2.307395	0.658323	1.125632	0.876917	0.512217	1.982446
3	—	0.241967	1.083152	0.960849	4.301189	1.478649	0.947776	12.73086
1	0.950419	3.841285	6.548634	0.390773	0.666191	0.366864	—	—
2	—	0.789577	1.838770	0.737456	1.717391	1.076372	0.672047	5.082044
3	—	0.168103	1.069542	0.966943	6.152101	1.495388	0.960535	15.80925
1	0.966515	3.794785	0.000000	0.263520	—	0.263520	—	—
2	—	1.935768	4.076623	0.495279	1.043030	0.641397	0.364090	1.499892
3	—	0.513081	1.561398	0.800282	2.435403	1.206176	0.765808	7.918443
4	—	0.122504	1.044564	0.978436	8.342904	1.516405	0.974915	18.44197

TABLE IV. Passband Ripple, P = 0.4dB.

STATUS		DESIGN				TEST AND ADJUST		
I	f_p/f_g	AI	BI	f_o/f_g	Q_I	f_{pi}/f_g	f_{xi}/f_g	IHXII
1	0.349311	1.000000	0.000000	1.000000	—	1.000000	—	—
1	0.690638	1.361436	1.382743	0.850412	0.863721	1.000000	0.488355	0.500000
1	0.856542	1.863635	0.000000	0.536586	—	0.536586	—	—
2	—	0.640186	1.193074	0.915517	1.706190	1.335117	0.833192	5.030512
1	0.903889	2.628161	3.434139	0.539624	0.705110	0.538096	—	—
2	—	0.364824	1.150866	0.932154	2.940553	1.418624	0.904802	9.495995
1	0.944056	2.923552	0.000000	0.342050	—	0.342050	—	—
2	—	1.302495	2.353418	0.651854	1.177805	0.880993	0.521307	2.284474
3	—	0.229001	1.083268	0.960798	4.544965	1.480065	0.949099	13.20349
1	0.955298	3.864492	6.979727	0.378513	0.683639	0.365535	—	—
2	—	0.752778	1.857255	0.733777	1.810376	1.077986	0.675491	5.499967
3	—	0.158910	1.071138	0.966223	6.512856	1.495030	0.960511	16.30110
1	0.970789	4.021119	0.000000	0.248687	—	0.248687	—	—
2	—	1.872914	4.179506	0.489145	1.091553	0.644589	0.372636	1.783643
3	—	0.486126	1.567604	0.798697	2.575546	1.207745	0.768006	8.384227
4	—	0.115575	1.044265	0.978576	8.841816	1.517046	0.975442	18.94474

TABLE V. Passband Ripple, P = 0.5dB.

The following equations are helpful when observing the effects of component deviations and temperature changes upon the filter transfer curve and phase behavior:

$$\omega_{01} = \frac{1}{\sqrt{\tau_1\tau_2}} = \frac{1}{\sqrt{R_1R_2C_1C_2}}; Q_1 = \frac{1}{2}\sqrt{\frac{\tau_2}{\tau_1}} = \frac{1}{2}\sqrt{\frac{C_2}{C_1}} \quad (7)$$

The equation for the corner frequency, ω_{01}, describes the signal response over frequency, while Q_1 denotes the peaking of the frequency response in the passband.

Equations 8-10 give values for the frequency response expressed in the same variables used in Equations 2, 3, and 4.

$$|A_I| = \left[1 + 2\tau_1(2\tau_1 - \tau_2)\omega^2 + (\tau_1\tau_2)^2\omega^4\right]^{-\frac{1}{2}} \quad (8)$$

$$|A_I| = \left[1 + (a_1 - 2b_1)\left(\frac{\omega}{\omega_g}\right)^2 + b_1^2\left(\frac{\omega}{\omega_g}\right)^4\right]^{-\frac{1}{2}} \quad (9)$$

$$|A_I| = \left[1 + \left(\frac{1}{Q_1^2} - 2\right)\left(\frac{\omega/\omega_g}{\omega_{01}/\omega_g}\right)^2 + \left(\frac{\omega/\omega_g}{\omega_{01}/\omega_g}\right)^4\right]^{-\frac{1}{2}} \quad (10)$$

Figure 2 shows the theoretical frequency response curve of the second order filter using an ideal op amp. The definitions given here will be used later on for comparison with and optimation of the filter response.

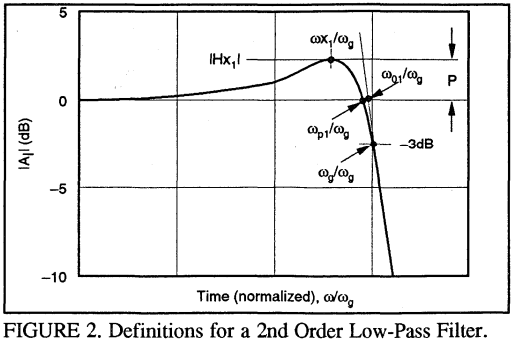


FIGURE 2. Definitions for a 2nd Order Low-Pass Filter.

Example Calculation
For a Low-Pass Filter

p = +0.1dB; f_g = 10MHz; $R_1 = R_2 = 300\Omega$

$Q_1 = 0.767360$

$f_{01}/f_g = 0.927601$

Q_1 and f_{01}/f_g are derived from the filter table.

$$\tau_1 = \frac{1}{2Q_1(f_{01}/f_g)\cdot 2\pi f_g} = \frac{1}{2\cdot 0.767360\cdot 0.927601\cdot 2\pi\cdot 10\text{MHz}} = 11.18\text{ns}$$

$$\tau_2 = \frac{2Q_1}{(f_{01}/f_g)\cdot 2\pi f_g} = \frac{2\cdot 0.767360}{0.927601\cdot 2\pi\cdot 10\text{MHz}} = 26.33\text{ns}$$

$$C_1 = \frac{\tau_1}{R_1} = \frac{11.8\text{ns}}{300} = 37.27\text{pF};$$

$$C_2 = \frac{\tau_2}{R_2} = \frac{26.33\text{ns}}{300} = 87.77\text{pF}$$

Figure 3 shows the frequency response $|A_f|$ of the filter circuit from Figure 1 using the filter component values calculated above.

1.2 2ND ORDER LOW-PASS FILTER WITH AN OP AMP MODEL

Unlike the ideal op amp used for the analyses above, op amps used in real circuits do not always behave as one might wish. For this reason, the following analyses use the OPA660 in current-feedback configuration. Figure 4 shows the circuit schematic of the OPA660 using the PT_2 model to describe the AC behavior.

These components values produce the following results with an optimally flat frequency response adjustment:

f_g = 357MHz $\qquad R_{OUT\,DC} = 45m\Omega$

$G_{OPEN\ LOOP\ DC}$ = 70dB $\qquad R_{OUT\ 100MHz} = 2.9\Omega$

If the ideal op amp shown in Figure 1 is replaced by the OPA660 PT_2 model (MOPA660), the resulting circuit diagram looks like that shown in Figure 5.

Slight changes in the capacitors C_1 and C_2 are necessary to correct the frequency response to a –3dB frequency of 10MHz. At 100MHz and above, the modeled frequency

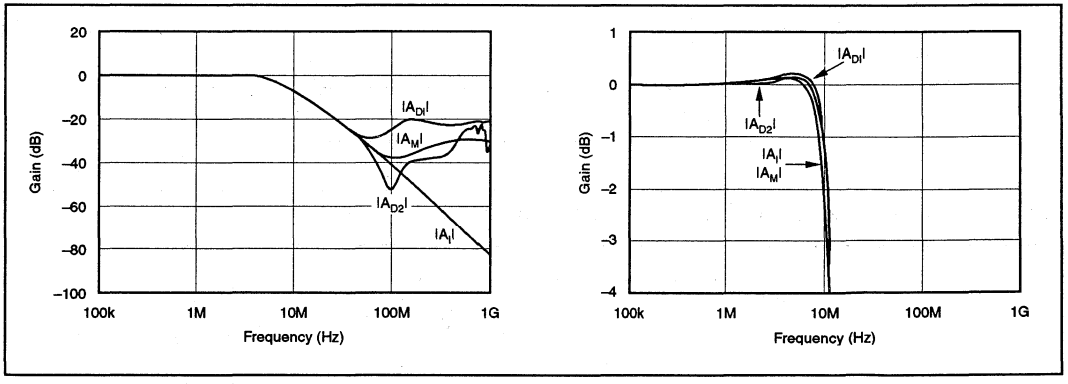


FIGURE 3. Frequency Response of the 2nd Order Low-Pass Filter from Figure 1 with Ideal Op Amp.

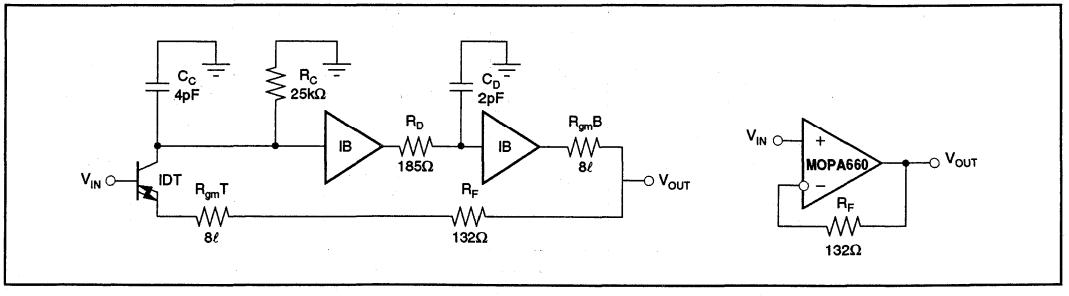


FIGURE 4. PT_2 Model Describing the OPA660 as Current-Feedback Amplifier.

response $V_{OUT\ M}$ begins to deviate from the ideal frequency response $V_{OUT\ I}$, since in practice the open-loop gain of the OPA660 decreases with increasing frequency. For this reason, the output impedance R_{OUT} rises from 45mΩ at DC to 2.9Ω at 100MHz.

1.3 TESTS WITH THE DEMO BOARD

As also shown in Figure 3, a demo board with the circuit shown in Figure 6 produces extremely poor stopband attenuation at the output $V_{OUT\ D1}$, primarily due to the package inductance in series to the resistor R_{gmB}. At 500MHz, for example, the package inductance of the output buffer (IB), which is about 10nH, causes R_{gmB} to increase by approximately 31Ω.

Poor stopband attenuation can be avoided by inserting the buffer, BUF600, and generating the output voltage at the capacitor, C_1. The BUF600 makes the original output $V_{OUT\ D1}$ superfluous. The rise in frequency response at 300MHz and above can be explained as a product of the direct crosstalk between input and output on the demo board.

2.0 2nd ORDER LOW-PASS FILTER USING THE FIRST AND SECOND OPEN-LOOP POLE OF WIDE-BAND AMPLIFIERS

2.1 Analyses Using The PT_2 Model

Wide-band op amps behave quite similarly to 2nd order low-pass filters. For this reason, their parameters can be determined by the equations used for the PT_2 model (see Figure 7).

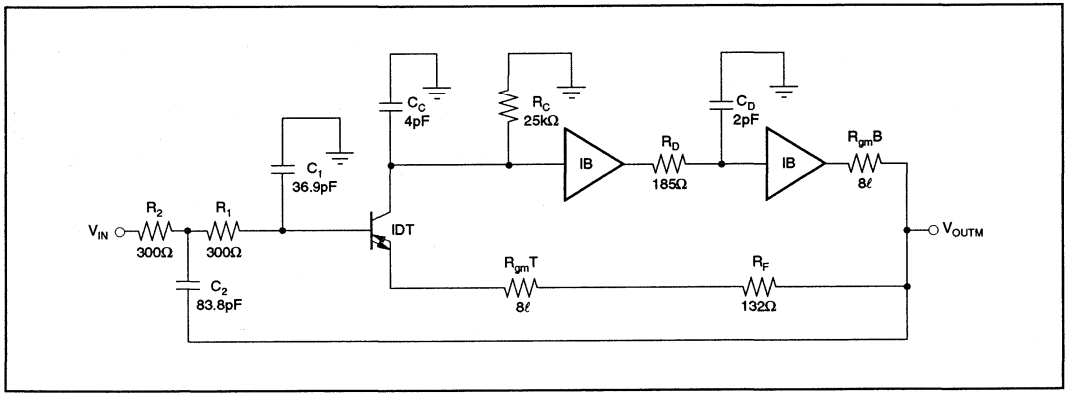


FIGURE 5. 2nd Order Low-Pass Filter Using the Modeled OPA660.

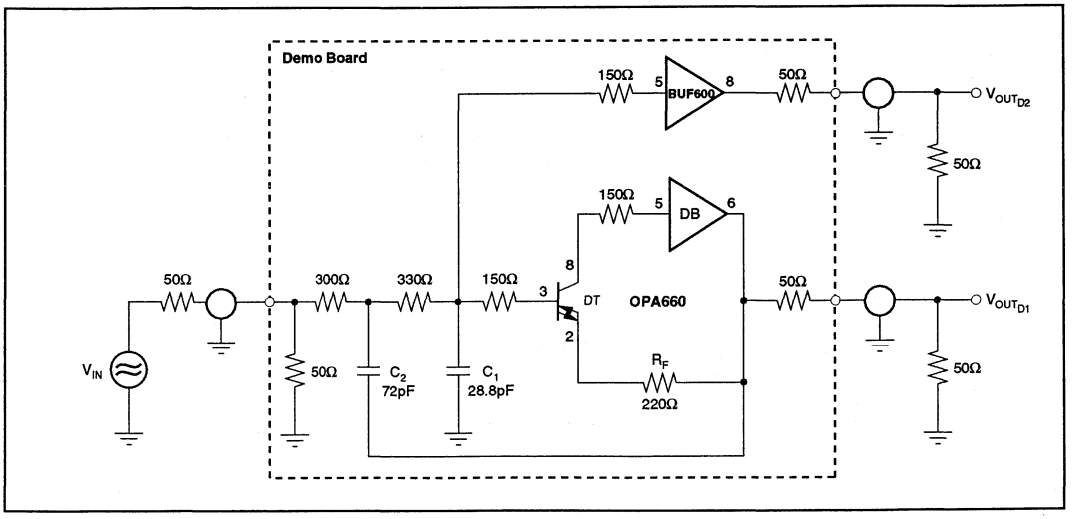


FIGURE 6. Demo Board Circuit Schematic for the 2nd Order Low-Pass Filter Using the OPA660.

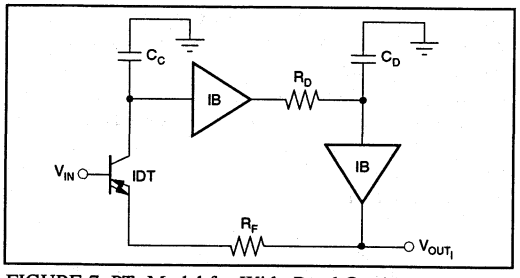


FIGURE 7. PT_2 Model for Wide-Band Op Amps.

The results are similar to the equations listed under point 1.1:

$$A_I = \left[1 + j\omega \bullet (\tau_C) + (j\omega)^2 \bullet (\tau_C \tau_D)\right]^{-1} \quad (11)$$

$$a_1 = \tau_C \omega_g = \frac{1}{Q_1(\omega_{01}/\omega_g)}; \qquad b_1 = \tau_C \tau_D \omega_g{}^2 = \frac{1}{(\omega_{01}/\omega_g)^2} \quad (12)$$

$$\tau_C = \frac{1}{Q_1(\omega_{01}/\omega_g)\omega_g}; \tau_D = \frac{Q_1}{(\omega_{01}/\omega_g)\omega_g} \quad (13)$$

$$\omega_{01} = \frac{1}{\sqrt{\tau_D \tau_C}} = \frac{1}{\sqrt{R_D R_F C_C C_D}}; \qquad Q_1 = \sqrt{\frac{\tau_D}{\tau_C}} = \sqrt{\frac{R_D C_D}{R_F C_C}} \quad (14)$$

$$|A_I| = \left[1 + \tau_C(\tau_C - 2\tau_D)\omega^2 + (\tau_C \tau_D)^2 \omega^4\right]^{-\frac{1}{2}} \quad (15)$$

When the curves described in Equations 8 and 15 are compared to each other, the result is a transfer response as shown in Figure 2.

2.2 Modified PT_2 Model

The customary PT_2 model shown in Figure 7 can be modified to produce the circuit shown in Figure 8 without significantly changing the transfer response.

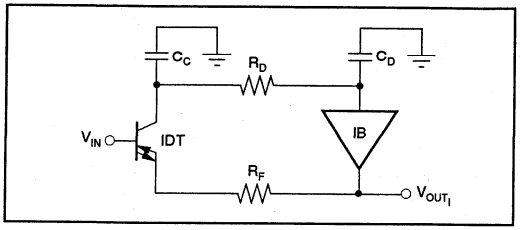


FIGURE 8. Modified PT_2 Model.

$$A_I = \left[1 + j\omega \bullet (\tau_C + \tau_D) + (j\omega)^2 \bullet (\tau_C \tau_D)\right]^{-1} \quad (16)$$

$$a_1 = (\tau_C + \tau_{CD})\omega_g = \frac{1}{Q_1(\omega_{01}/\omega_g)}; \qquad b_1 = \tau_C \tau_D \omega_g{}^2 = \frac{1}{(\omega_{01}/\omega_g)^2} \quad (17)$$

$$\tau_C = \tau_{CD} = \frac{1}{2Q_1(\omega_{01}/\omega_g)\omega_g}; \tau_D = \frac{2Q_1}{(\omega_{01}/\omega_g)\omega_g} \quad (18)$$

$$\omega_{01} = \frac{1}{\sqrt{\tau_D \tau_D}} = \frac{1}{\sqrt{R_D R_F C_C C_D}}; \qquad Q_1 = \sqrt{\frac{R_D C_C C_D}{R_F (C_C + C_D)^2}} = \frac{1}{2}\sqrt{\frac{R_D}{R_F}} \quad (19)$$

$$|A_I| = \left\{1 + \left[(\tau_C + \tau_{CD})^2 - 2\tau_C \tau_D\right]\omega^2 + (\tau_C \tau_D)^2 \omega^4\right\}^{-\frac{1}{2}} \quad (20)$$

The modified version no longer requires a buffer, but the capacitor C_C must be equal to C_D. This condition is similar to Figure 1, in which R_1 must be equal to R_2.

Example Calculation
For a Low-Pass Filter

p = +0.1dB; f_g = 10MHz; $C_C = C_D$ = 30pF

Q_1 = 0.767360

f_{01}/f_g = 0.927601

a_1 and f_{01}/f_g can be derived from the filter table.

$$\tau_C = \tau_{CD} = \frac{1}{2Q_1(f_{01}/f_g) \bullet 2\pi f_g} = \frac{1}{2 \bullet 0.767360 \bullet 0.927601 \bullet 2\pi \bullet 10\text{MHz}} = 11.18\text{ns}$$

$$\tau_D = \frac{2Q_1}{(f_{01}/f_g) \bullet 2\pi f_g} = \frac{2 \bullet 0.767360}{0.927601 \bullet 2\pi \bullet 10\text{MHz}} = 26.33\text{ns}$$

$$R_F = \frac{\tau_C}{C_C} = \frac{11.18\text{ns}}{30\text{pF}} = 372.7\Omega; \qquad R_D = \frac{\tau_D}{C_D} = \frac{26.33\text{ns}}{30\text{pF}} = 877.7\Omega$$

Figure 9 shows the frequency response $|A_I|$, which is identical to the frequency response shown in Figure 3.

2.3 2nd Order Low-Pass Filter Based On Adjusted Open-Loop Poles

The circuit shown in Figure 10 combines the ideal circuit from Figure 8 with the OPA660 model.

The resistors R_D and R_F are used to fine-tune the frequency response $|A_M|$, resulting in the curve shown in Figure 9. The conditions listed in section 1.2 for signals at 100MHz and above also apply here.

The 2nd order low-pass filter shown in Figure 5 contains 4 time constants: the dominating external time constants τ_1 and τ_2, which determine the actual filter curve, and the two parasitic internal time constants τ_C and τ_D. The 2nd order low-pass filter in Figure 10, however, contains only τ_C and τ_D. The unavoidable internal parasitic time constants $\tau_{C\ IN}$ and $\tau_{D\ IN}$ are included in the dominating external time constants $\tau_{C\ OUT}$ and $\tau_{D\ OUT}$.

2.4 Tests Using The Demo Board

The circuit shown in Figure 10 was used to construct the demo board shown in Figure 11. Figure 9 contains the frequency responses $|A_{D1}|$ and $|A_{D2}|$ measured at the outputs $V_{OUT\ D1}$ and $V_{OUT\ D2}$.

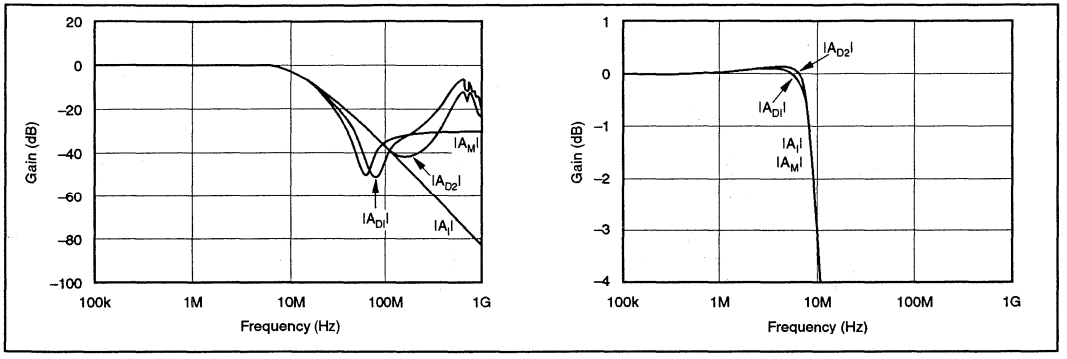


FIGURE 9. Frequency Responses of a 2nd Order Low-Pass Filter According to the Structure in Figure 8.

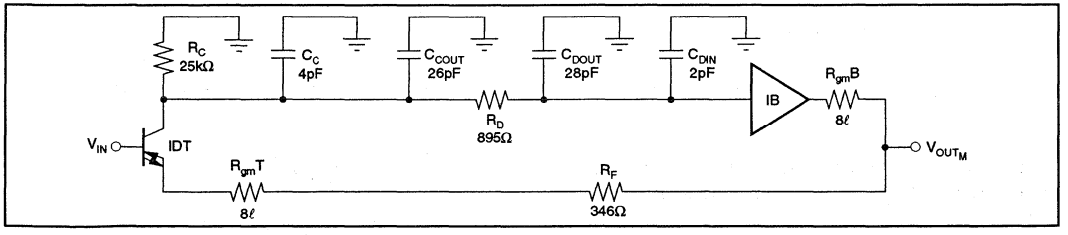


FIGURE 10. 2nd Order Low-Pass Filter Using the Modelled OPA660.

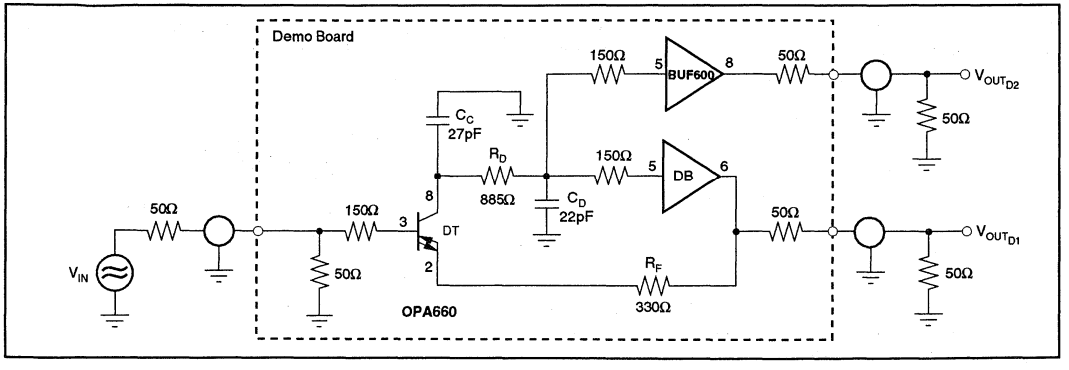


FIGURE 11. Demo Board with a 2nd Order Low-Pass Filter Using the OPA660.

As already explained in section 1.3, the output $V_{OUT\,D2}$ here also shows the improved frequency response $|A_{D2}|$.

3.0 3RD ORDER LOW-PASS FILTER BASED ON ADJUSTED OPEN-LOOP POLES

3.1 Modified PT_2 Model With Preceding Low-Pass Filter

The structure shown in Figure 8 does not contain a prefilter. Instead, the idealized Diamond Transistor IDT has to handle the full bandwidth of the input signal. In Figure 1, the low-pass filter in front of the op amp IOPA reduces the demands on its bandwidth. Consequently, the 2nd order filter structure in Figure 11 is extended by a passive RC filter at the input. This filter improves the overall filter performance, especially at frequencies above twice the –3dB frequency, where the increase in output impedance begins to degrade the filter curve.

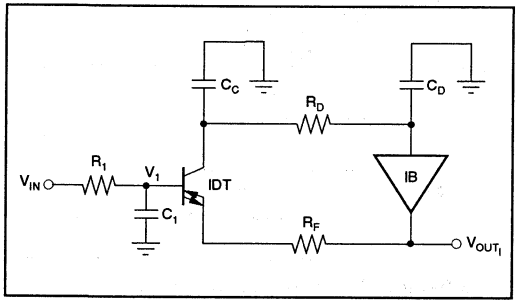


FIGURE 12. Modified PT_2 Model with Preceding Low-Pass Filter τ_1.

$$A_I = \left\{\left[1 + j\omega \bullet (\tau_1)\right]\left[1 + j\omega \bullet (\tau_C + \tau_{CD}) + (j\omega)^2 \bullet (\tau_C \tau_D)\right]\right\}^{-1} \tag{21}$$

$$a_1 = \tau_1 \omega_g = \frac{1}{(\omega_{01}/\omega_g)} \qquad a_2 = (\tau_C + \tau_{CD})\,\omega_g = \frac{1}{Q_2(\omega_{02}/\omega_g)} \tag{22}$$

$$b_2 = \tau_C \tau_D \omega_g{}^2 = \frac{1}{(\omega_{01}/\omega_g)^2} \tag{23}$$

$$\tau_1 = \frac{1}{(\omega_{01}/\omega_g)\,\omega_g};\ \tau_C = \tau_{CD} = \frac{1}{2Q_2(\omega_{02}/\omega_g)\,\omega_g};\ \tau_D = \frac{2Q_2}{(\omega_{02}/\omega_g)\,\omega_g} \tag{24}$$

$$\omega_{01} = \frac{1}{R_1 C_1};\ \omega_{02} = \frac{1}{\sqrt{R_D R_F C_C C_D}};\ Q_2 = \frac{\sqrt{R_D C_C C_D}}{R_F (C_C + C_D)^2} = \frac{1}{2}\sqrt{\frac{R_D}{R_F}} \tag{25}$$

$$|A_I| = \left[1 + A\omega^2 + B\omega^4 + C\omega^6\right]^{\frac{1}{2}}$$
$$A = \tau_1{}^2 + (\tau_C + \tau_{CD})^2 - 2\tau_C\tau_D$$
$$B = \tau_1{}^2\left[(\tau_C + \tau_{CD})^2 - 2\tau_C\tau_D\right] + (\tau_C\tau_D)^2 \tag{26}$$
$$C = (\tau_1\tau_C\tau_D)^2$$

Figure 14 shows the theoretical (ideal) frequency response curve of a 3rd order low-pass filter. The definitions in Figure 13 support the readings from the filter table.

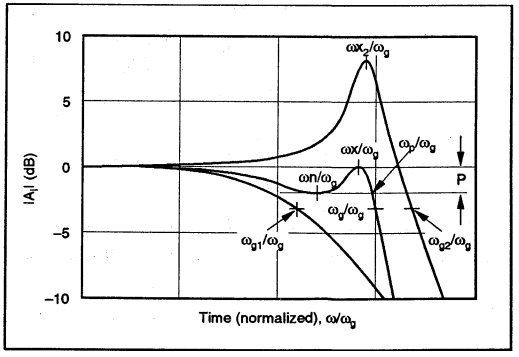


FIGURE 13. Definitions of a 3rd Order Low-Pass Filter.

Example Calculation For a Low-Pass Filter

p = +0.1dB; f_g = 10MHz; $C_1 = C_C = C_D$ = 30pF

f_{01}/f_g = 0.697919

f_{02}/f_g = 0.935859

Q_2 = 1.340928

Q_2 and f_{01}/f_g are derived from the filter table.

$$\tau_1 = \frac{1}{(f_{01}/f_g) \bullet 2\pi f_g} = \frac{1}{0.697919 \bullet 2\pi \bullet 10\text{MHz}} = 22.80\text{ns}$$

$$\tau_C = \tau_{CD} = \frac{1}{2Q_2(f_{02}/f_g) \bullet 2\pi f_g} = \frac{1}{2 \bullet 1.340928 \bullet 0.935859 \bullet 2\pi \bullet 10\text{MHz}} = 6.341\text{ns}$$

$$\tau_D = \frac{2Q_2}{\left(f_{02}/f_g\right)\bullet 2\pi f_g} = \frac{2\bullet 1.340928}{0.935859\bullet 2\pi\bullet 10\text{MHz}} = 45.61\text{ns}$$

$$R_1 = \frac{\tau_1}{C_1} = \frac{22.80\text{ns}}{30\text{pF}} = 760\Omega; R_F = \frac{\tau_C}{C_C} = \frac{6.341\text{ns}}{30\text{pF}} = 211.4\Omega$$

$$R_D = \frac{\tau_D}{C_D} = \frac{45.61\text{ns}}{30\text{pF}} = 1520\Omega$$

3.2 3rd Order Low-Pass Filter With A Modeled Op Amp

In Figure 15, the 3rd order low-pass filter circuit using an ideal op amp has been replaced by a modeled OPA660.

Figure 14 also shows how by inserting a passive prefilter, this 3rd order low-pass filter produces an improvement in stopband attenuation over a 2nd order filter while maintaining the same hardware in the active filter.

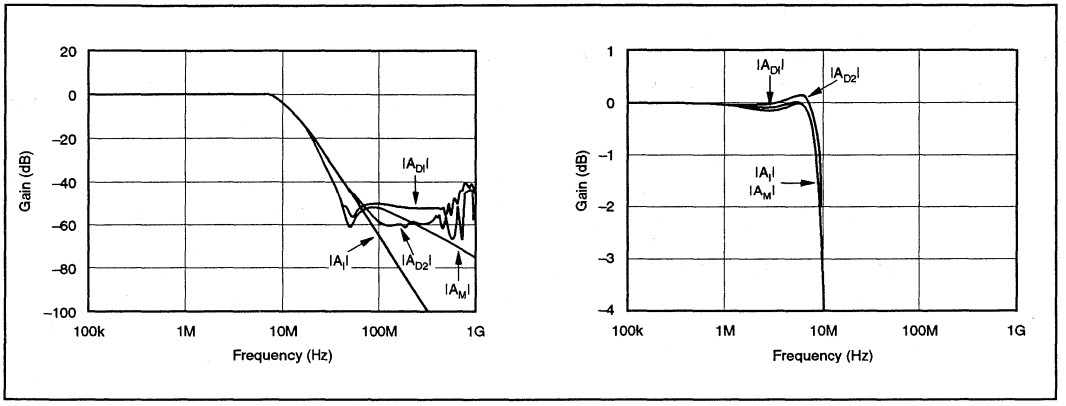


FIGURE 14. Ideal Frequency Responses of a 3rd Order Low-Pass Filter Based on Adjusted Open-Loop Poles.

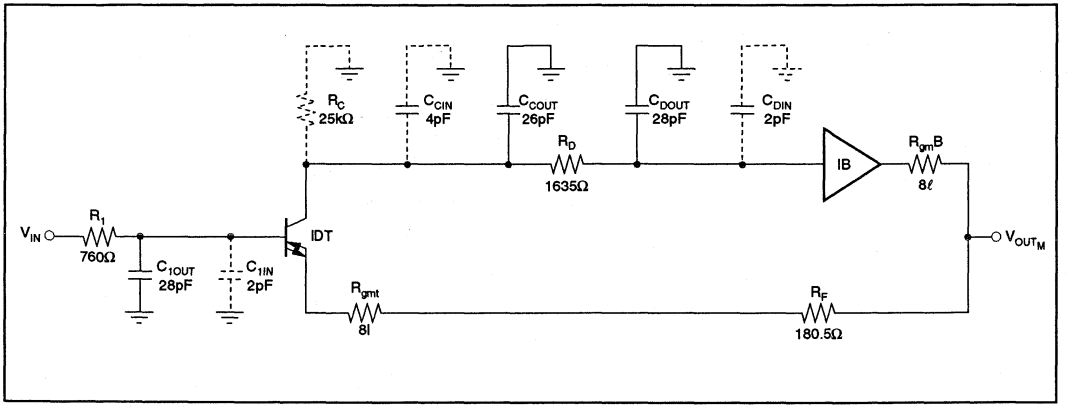


FIGURE 15. 3rd Order Low-Pass Filter with the Modeled OPA660.

3.3 Tests Using The Demo Board

Figure 14 shows frequency responses measured using the demo board illustrated in Figure 16. As with 2nd order low-pass filters, the best curve results when the frequency response $|A_{D2}|$ is decoupled separately by the BUF600 at V_{OUTD2}.

4.0 5TH ORDER LOW-PASS FILTER BASED ON ADJUSTED OPEN-LOOP POLES

4.1 5th Order Low-Pass Filter With Ideal Amplifiers

Figure 17 shows the 3rd order low-pass filter from Figure 12 in series with the 2nd order low-pass filter from Figure 8.

$\tau_1 = R_1C_1$ $\quad \tau_{CD2} = R_{F2}C_{D2}$ $\quad \tau_{C3} = R_{F3}C_{C3}$

$\tau_{C2} = R_{F2}C_{C2}$ $\quad C_{C2} = C_{D2}$ $\quad \tau_{D3} = R_{D3}C_{D3}$

$\tau_{D2} = R_{D2}C_{D2}$ $\quad C_{C3} = C_{D3}$ $\quad \tau_{CD3} = R_{F3}C_{D3}$

$$A_1 = \left\{\left[1+j\omega(\tau_1)\right]\left[1+j\omega(\tau_{C2}+\tau_{CD2})+(j\omega)^2(\tau_{C2}\tau_{D2})\right]\left[1+j\omega(\tau_{C3}+\tau_{CD3})+(j\omega)^2(\tau_{C3}\tau_{D3})\right]\right\}^{-1} \quad (27)$$

$$a_1 = \tau_1\omega_g = \frac{1}{(\omega_{01}/\omega_g)};$$

$$a_2 = (\tau_{C2}+\tau_{CD2})\omega_g = \frac{1}{Q_2(\omega_{02}/\omega_g)}$$

$$b_2 = \tau_{C2}\tau_{D2}\omega_g{}^2 = \frac{1}{(\omega_{02}/\omega_g)^2};$$

$$a_3 = (\tau_{C3}+\tau_{CD3})\omega_g = \frac{1}{Q_3(\omega_{03}/\omega_g)} \quad (28)$$

$$b_3 = \tau_{C3}\tau_{D3}\omega_g{}^2 = \frac{1}{(\omega_{03}/\omega_g)^2}$$

$$\tau_1 = \frac{1}{(\omega_{01}/\omega_g)\omega_g};\tau_{C2} = \tau_{CD2} = \frac{1}{2Q_2(\omega_{02}/\omega_g)\omega_g};$$

$$\tau_{D2} = \frac{2Q_2}{(\omega_{02}/\omega_g)\omega_g}$$

$$\tau_{C3} = \tau_{CD3} = \frac{1}{2Q_3(\omega_{03}/\omega_g)\omega_g};\tau_{D3} = \frac{2Q_3}{(\omega_{02}/\omega_g)\omega_g} \quad (29)$$

$$\omega_{01} = \frac{1}{R_1C_1};\omega_{02} = \frac{1}{\sqrt{R_{D2}R_{F2}C_2C_{D2}}};$$

$$Q_2 = \sqrt{\frac{R_{D2}C_{C2}C_{D2}}{R_{F2}(C_{C2}+C_{D2})^2}} = \frac{1}{2}\sqrt{\frac{R_{D2}}{R_{F2}}}$$

$$\omega_{03} = \frac{1}{R_{D3}R_{F3}C_{C3}C_{D3}};Q_3 = \sqrt{\frac{R_{D3}C_{C3}C_{D3}}{R_{F3}(C_{C3}+C_{D3})^2}} = \frac{1}{2}\sqrt{\frac{R_{D3}}{R_{F3}}} \quad (30)$$

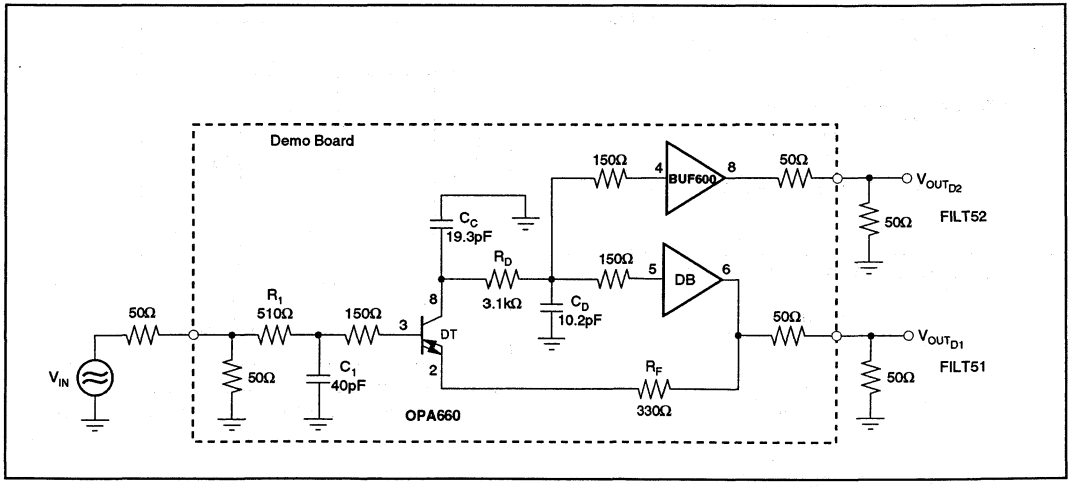


FIGURE 16. Demo Board with a 3rd Order Low-Pass Filter Using the OPA660.

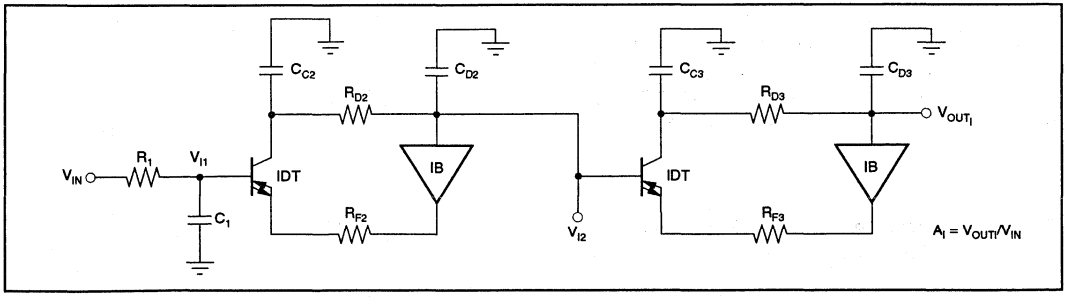


FIGURE 17. 5th Order Low-Pass Filter with Ideal Amplifiers.

Example Calculation
For A Low-Pass Filter

p = +0.2dB, f_g = 10MHz, C_1 = 70pF, $C_{C2} = C_{D2}$ = 30pF; $C_{C3} = C_{D3}$ = 9pF

$f_{01}/f_g = 0.419787$ $\quad Q_2 = 1.000908$
$f_{02}/f_g = 0.679846$ $\quad Q_3 = 3.706857$
$f_{03}/f_g = 0.961717$

f_{01}/f_g, f_{02}/f_g, f_{03}/f_g, Q_2 and Q_3 are derived from the filter table.

$$\tau_1 = \frac{1}{(f_{01}/f_g)\cdot 2\pi f_g} = \frac{1}{0.419787\cdot 2\pi\cdot 10\text{MHz}} = 37.91\text{ns}$$

$$\tau_{C2} = \tau_{CD2} = \frac{1}{2Q_2(f_{01}/f_g)\cdot 2\pi f_g}$$

$$= \frac{1}{2\cdot 1.000908\cdot 0.679846\cdot 2\pi\cdot 10\text{MHz}} = 11.69\text{ns}$$

$$\tau_{D2}\frac{2Q_2}{(f_{02}/f_g)\cdot 2\pi f_g} = \frac{2\cdot 1.000908}{0.679846\cdot 2\pi\cdot 10\text{MHz}} = 46.86\text{ns}$$

$$\tau_{C3} = \tau_{CD3} = \frac{1}{2Q_3(f_{03}/f_g)\cdot 2\pi f_g}$$

$$= \frac{0.1}{2\cdot 3.706857\cdot 0.961717\cdot 2\pi\cdot 10\text{MHz}} = 2.2322\text{ns}$$

$$\tau_{D3} = \frac{2Q_3}{(f_{03}/f_g)\cdot 2\pi f_g} = \frac{2\cdot 3.706857}{0.961717\cdot 2\pi\cdot 10\text{MHz}} = 122.69\text{ns}$$

$$R_1 = \frac{\tau_1}{C_1} = \frac{37.91\text{ns}}{70\text{pF}} = 541.6\Omega$$

$$R_{F2} = \frac{\tau_{C2}}{C_{C2}} = \frac{11.69\text{ns}}{30\text{pF}} = 389.8\Omega$$

$$R_{D2} = \frac{\tau_{D2}}{C_{D2}} = \frac{46.86\text{ns}}{30\text{pF}} = 1562\Omega$$

$$R_{F3} = \frac{\tau_{C3}}{C_{C3}} = \frac{2.2322\text{ns}}{9\text{pF}} = 248.0\Omega$$

$$R_{D3} = \frac{\tau_{D3}}{C_{D3}} = \frac{122.69\text{ns}}{9\text{pF}} = 13.632\text{k}\Omega$$

Figure 18 shows the ideal frequency response $|A_I|$ of a 5th order low-pass filter.

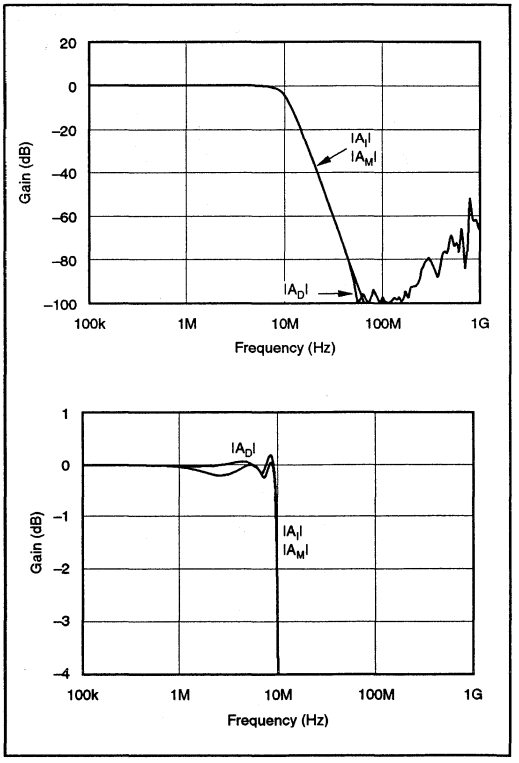


FIGURE 18. Frequency Responses of a 5th Order Low-Pass Filter Based on Adjusted Open-Loop Poles.

4.2 5th Order Low-Pass Filter With A Modeled Op Amp

By adjusting the resistors R_{FX} and R_{DX}, it is possible to include the effects of the parasitic resistors R_{CX} and capacitors $C_{XX\ IN}$ in the frequency response curve while changing the curve only slightly. This process is comparable to changing $|A_I|$ to $|A_M|$ as shown in Figure 18. The output impedance R_{CX} produces more and more disturbances with increasingly higher order filters. The size of the filter capacitors C_{CX} and C_{DX} also increases with higher order filters and –3dB frequencies. Experiments are currently in progress to develop filter circuits using the OPA660 that are much less susceptible to filter quality and capacitance; we will present the results in Part Two.

4.3 Tests Using The Demo Boards

Figure 18 shows the frequency response $|A_D|$ measured using the demo board in Figure 20.

Further application notes about the OPA660:

AN-179 "Current or Voltage Feedback? That's the Question Here."

AN-180 "Quasi-Ideal Current Source"

AN-181 "Circuit Technology with the Diamond Transistor OPA660"

AN-183 "New Ultra High-Speed Circuit Techniques with Analog ICs"

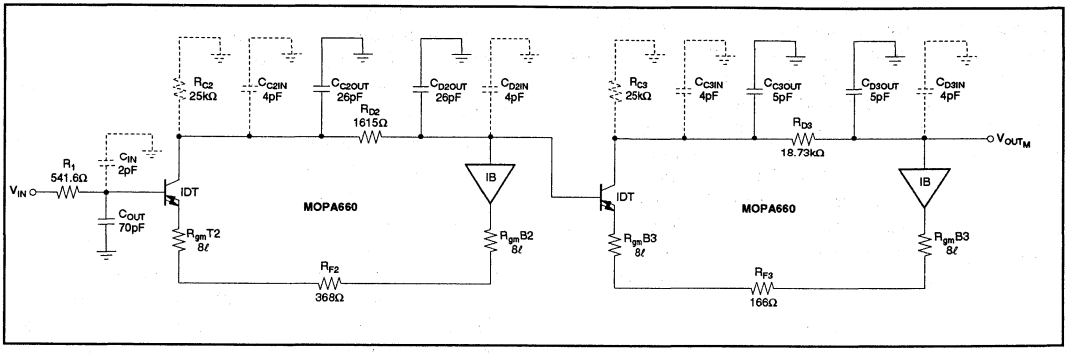


FIGURE 19. 5th Order Low-Pass Filter with the Modeled OPA660.

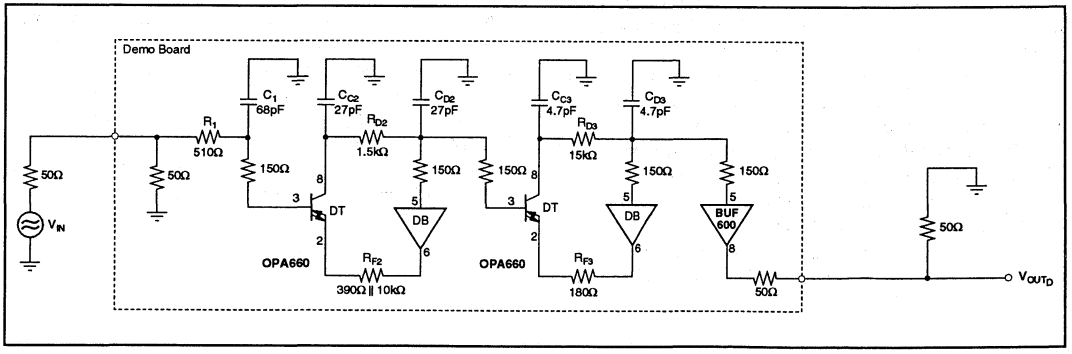


FIGURE 20. Demo Board with a 5th Order Low-Pass Filter Using the OPA660.

BURR-BROWN® APPLICATION BULLETIN

Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

FIBER OPTIC TRANSMISSION

By Christian Henn, Burr-Brown International GmbH

Fiber optic transmission is assuming an increasingly important role in systems for wide-band analog signals and digital signals with high data rates. Although the number of applications for digital networks and telecommunications systems is skyrocketing, analog transmission is still vital to many applications. Analog systems with bandwidths of up to 150MHz are used for wide-band RGB signal distribution, HDTV video signal transmission, and many types of EMI- and EMC-disturbed environments. Also important are medical applications, which demand the precision of fiber optic technology for safety reasons. The many features of fiber optic cables make them vital for all of these types of applications. Fiber optic cables enable transmission over long distances, ensure low damping vs frequency, are light and flexible, and provide high immunity against disturbances from magnetic and electric fields. State-of-the-art fiber optic transmission systems are now available even for data networks with transmission rates of up to 1.2Gbit/s, and gallium arsenide technology is used for their transmitter and receiver circuits.

The fiber optic transmission interface presented here uses new complementary bipolar integrated circuits from Burr-Brown. The OPA660, which is used as an LED driver and AGC multiplier, contains an operational transconductance amplifier and a buffer in an 8-pin package. The OPA621 is a low-noise, wide-band op amp in classical configuration, which functions as an amplifier in the I/V conversion section behind the photodiode and as an I/V converter behind the AGC multiplier. The current-feedback amplifier OPA623 provides additional gain in the AGC section and drives the 75Ω output. A discrete differential amplifier functions as an AGC error amp and controls the quiescent current of the OPA660 together with a FET. The CA3080 stabilizes the DC performance, and the LM1881 functions as a sync separator. The interface uses the IA184A as LED and the SFH202 as pin diode.

FIBER OPTIC INTERFACE BASICS

A fiber optic interface generally consists of five major functions as shown in Figure 1. On the transmitter side, a circuit processes the input signal in order to drive the electro-optical converter. This converter, which can be an LED or a laser diode, generates the signal-dependent light intensity modulation, and its mechanical case eases transmission of the signal into the fiber. At the fiber end, a pin diode converts the optical signal back into a low electrical current. The low-noise transimpedance preamplifier converts the current signal into a voltage and also amplifies it to an acceptable level.

Because the photodiode input signal can vary in amplitude, and AGC amplifier adjusts the peak-to-peak signal level to 1.4Vp-p and restores the DC level for no signal to 0V.

The quality of a fiber optic interface is characterized by several factors such as signal-to-noise ratio, linearity, bandwidth, power consumption, and transmission distance. The S/N ratio should be at least 50dB for analog systems to achieve an image that is free of noise. In conventional designs, there are basically two ways to improve the S/N ratio. One is to increase the diode drive current, which, though, leads to higher harmonic distortion. The second is to use a very low-noise transimpedance amplifier as a receiver. Both alternatives increase the component count and add manufacturing costs. The circuits presented here, however, are a new approach to simplifying and minimizing the design of an analog fiber optic interface and to provide an interface that is more integrated and offers lower power consumption. Table I summarizes the parameters of this new type of wide-band analog fiber optic interface.

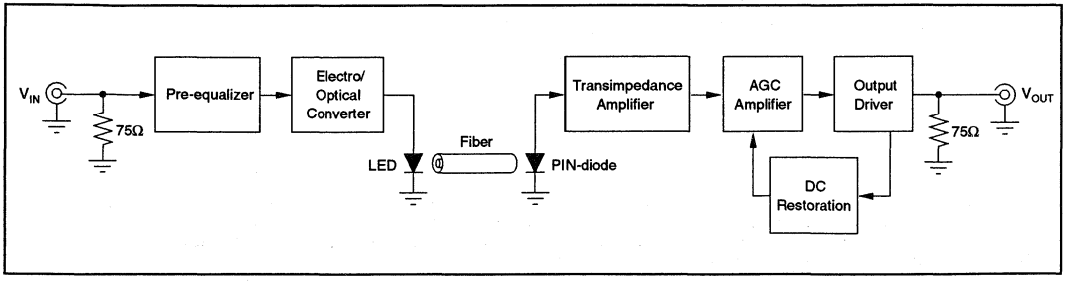


FIGURE 1. Block Diagram of a Fiber Optic Transmission Interface.

PARAMETER	UNIT
Bandwidth	120MHz
Differential Gain	≤ 3%
Differential Phase	≤ 3°
S/N Ratio	≥ 50dB
AGC Range	20:1
Input Voltage	+0.7V/–0.3V terminated in 75Ω
Output Voltage	+0.7V/–0.3V terminated in 75Ω
Supply Voltage	±5V

TABLE I. Interface Parameters.

TRANSMITTER

The block diagram illustrated in Figure 2 can be divided into three major blocks. The preequalizer compensates for the nonlinearity of the diode. The driver circuit converts the input signal into an output current, which generates the optical signal when flowing through the LED. For the LED to function linearly in the forward region, a positive DC current has to flow through it to adjust its bias point and keep it constant over temperature variations. Figure 3 shows the discrete circuit to adjust the LED bias point. R_{QC} can be calculated by the following equation:

$$R_{QC} = \frac{V_+ - V_{BEQ2}}{I_{EI}} - R_{D2} \qquad (1)$$

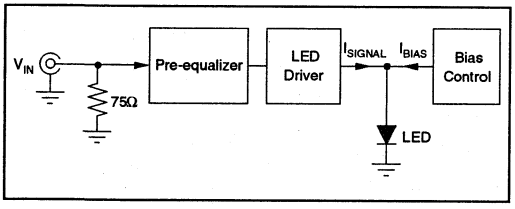


FIGURE 2. Block Diagram of Transmitter.

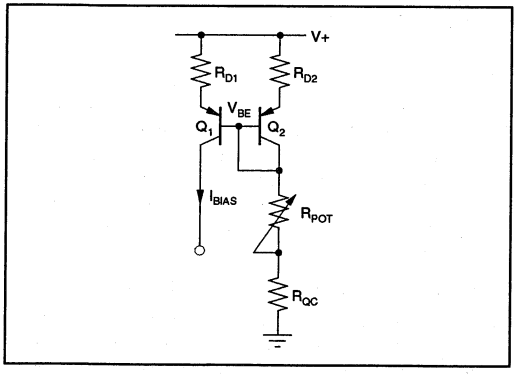


FIGURE 3. Bias Control.

One characteristic of a current source is its high impedance. To avoid current distribution, the output impedance should be much higher than the load impedance. The transmitter diode is a 2Ω to 4Ω load adjusted to the correct bias point. The high output impedance of 10kΩ for the current source prevents any distribution.

To modulate the diode current, the OTA of the OPA660 operates as a voltage-controlled current source and converts the input voltage into output current. As shown in Figure 4, the resistor R_E is the only element that has to be selected in order to define the conversion factor between input voltage and output current according to equation 2:

$$R_E = \frac{V_{IN}}{I_{OUT}} - R_e \qquad (2)$$

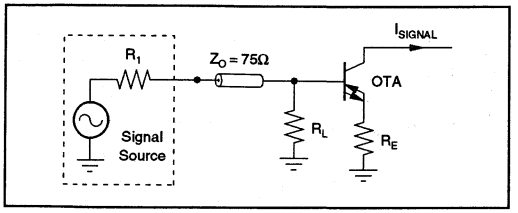


FIGURE 4. Voltage-to-Current Converter.

R_E is the output impedance of the OTA's emitter output and is 8Ω or 1/125mA/V at a +20mA quiescent current. The transfer curve between the diode current and optical power is only fairly linear within a small modulation range around the bias point. The larger the modulation range, the larger the nonlinearity. The equalization circuit proposed in Figure 5, however, can be used to improve the linearity or extend the modulation range. The diodes function like switches and connect the resistors in parallel to R_E when the corresponding diode is forward biased. The equalization circuit varies the voltage-to-current conversion according to the input voltage factor (mV/A) and partly compensates the diode nonlinearity.

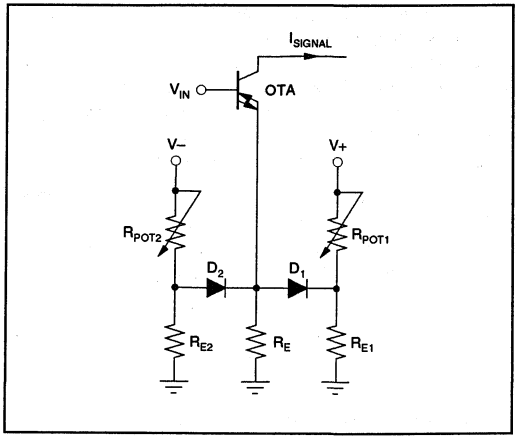


FIGURE 5. Transmitter with Preequalization.

As shown in Figure 6, the differential gain of the entire transistor circuit decreases from 25% without equalization to 6% with equalization. With more hardware, a further improvement down to 2% would be feasible. Figure 6 also presents the differential gain errors for the diode current, which impressively demonstrate that the conversion from a current to an optical power generates most of the nonlinearities.

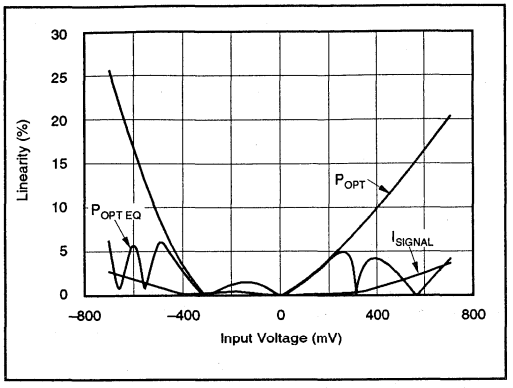


FIGURE 6. Transmitter Linearity Performance.

The complete transmitter is shown in Figure 7. Using the component values given in Figure 7, the discrete biasing circuit adjusts the diode current without modulation to +35mA, which produces a +1.55V voltage drop across the diode. Even at the highest modulation current of 30mA, the voltage drop of +1.7V remains far below the collector-emitter saturation voltage.

The drive capability of the OPA660 is limited to ±15mA. For this reason, two OTA current source outputs are connected together to increase the drive capability to ±30mA.

The input signal is applied to both bases of the OTA. In this application, each OPA660 operates with 20mA quiescent current, and requiring a R_{QC} resistor of 250Ω. The unused buffers of the OPA660s can either be connected to GND by a resistor or used for other circuit functions such as compensation of the OTA input offset voltage (in this case, R_E should be connected to the buffer output).

Figure 8 shows the frequency response of the diode current and optical power. Equation 3 gives a reasonable calculation for the 3dB frequency based on the effective capacitance at the diode anode and the total resistance:

$$f = \frac{1}{2\pi R(C_P + C_{DT})} \qquad (3)$$

R = Diode resistance, 3Ω
C_P = Biasing circuit, 25pF
C_{DT} = Input capacitance OTA-C, 8pF

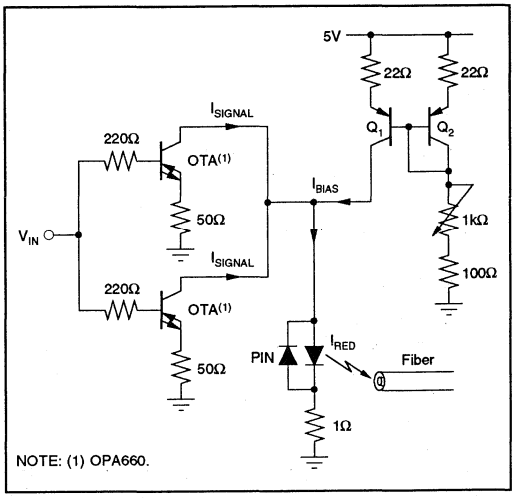


FIGURE 7. Transmitter Circuit.

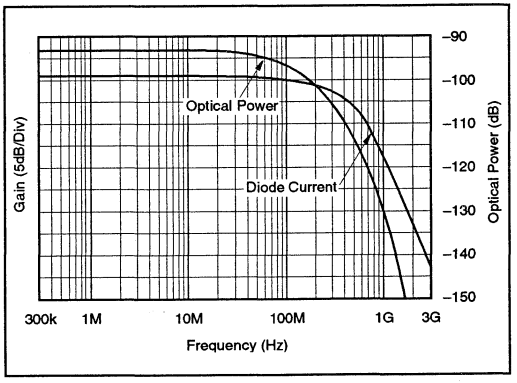


FIGURE 8. Bandwidth Transmitter.

When these values are put into the equation, the transmitter has a –3dB bandwidth of 800MHz, which corresponds to that in actual measurements. Comparing the curves in Figure 8 with each other shows that the transmitter diode and not the transmitter is the bandwidth-limiting factor. However, the 115MHz optical power matches the figures provided in the diode specification.

LOW-NOISE TRANSIMPEDANCE AMPLIFIER

On the receiver side, the electronic circuitry converts the optical power into a voltage, amplifies the normally weak signal, and stabilizes the output voltage for different cable lengths via an AGC control loop. A sensitive, small, fairly linear PIN-diode such as the SFA202 used here delivers output currents in the µA to mA range in typical applications. To convert weak, wide-band signals into voltages, while simultaneously amplifying them, is a tough job for

wide-band amplifiers. Figure 9 shows the typical transimpedance configuration. The PIN-diode cathode is directly connected to the inverting op amp input. The positive input is tied to GND. The effective transimpedance resistor connects the output to the inverting input. For low frequencies, the output voltage is calculated by:

$$V_{OUT} = -I_P \bullet \frac{R_F}{1+1/G_{OL}} \approx -I_P \bullet R_F \qquad (4)$$

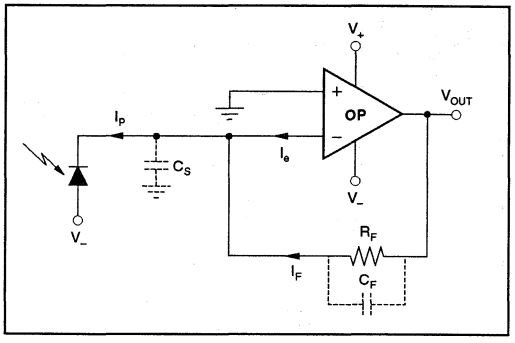


FIGURE 9. Transimpedance Amplifier.

Obviously, amplification does not work at higher frequencies where the open-loop gain (G_{OL}) decreases. Op amps, like the OPA621 used here, are internally compensated, and the open-loop gain rolls off by –20dB/decade.

Equation 5 allows an estimation of the maximum R_F size for a given –3dB bandwidth.

$$R_F = \frac{1}{2\pi 100MHz \bullet 0.5pF} \approx 3.2k\Omega \qquad (5)$$

The minimum detectable input current depends upon the noise performance, which in turn is based upon the noise of the low-noise preamplifier. The various noise sources of a transimpedance amplifier are shown in Figure 10. After the op amp noise, the next most important noise factor is the total thermal noise from all of the resistances. The thermal noise can be calculated by the following equation:

$$V_{th}^2 = 4 \bullet kT \bullet R \bullet B \qquad (6)$$

Thus, the effective noise voltage increases with temperature, T, bandwidth, B, and resistor size. Another often negligible noise factor is the pin diode itself. The diode's noise is mostly 1/f noise and is much higher in the forward than in the reverse region of the diode biasing. It can be calculated as follows:

$$i_s^2 = 2eI_P \bullet B \qquad (7)$$

To analyze the noise from all effective noise sources at the transimpedance amplifier output, determine the effective noise from all of the individual sources and add them

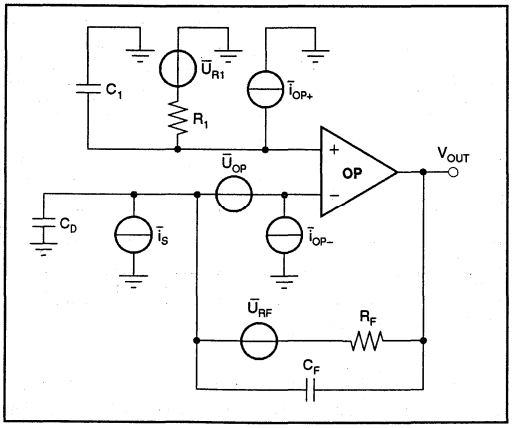


FIGURE 10. Noise Sources of a Transimpedance Amplifier.

geometrically to find the square sum. The purpose of a noise analysis is to ascertain the minimum detectable input signal current from the pin diode. The preamplifier noise performance also determines the required transmitter power, maximum cable length for a given transmitter current, dynamic range of the receiver, and signal-to-noise ratio. By dividing the voltage noise at the output by the transimpedance resistor R_F, it is possible to calculate the equivalent input noise current, which is also the minimum detectable input signal.

The noise performance of any op amp varies over frequency, because in any integrated circuit, different noise sources are effective in different frequency ranges.

Table II summarizes the voltage noise density and effective noise voltage for the OPA621 vs frequency. The input current noise density is listed as 3.3pA/$\sqrt{Hz}$ in the PDS. Table III adds up the single noise sources to find the effective noise voltage at the amplifier output for three different frequencies. It can be derived that the equivalent noise voltage is dependent upon the system bandwidth. Thus, for any given transimpedance amplifier, the S/N ratio decreases with increasing bandwidth.

FREQUENCY/Hz	VOLTAGE NOISE/nV/$\sqrt{Hz}$	EFF. NOISE/μVrms
0 - 200	10	0, 141
200 - 2k	5, 5	0, 23
2k - 20k	3, 3	0, 44
20k - 1M	2, 5	2, 47
1M - 10M	2, 3	6, 90
10M - 100M	2, 3	21, 82
TOTAL		24.17

TABLE II. OPA621 Noise Performance vs Frequency.

NOISE SOURCE	VOLTAGE NOISE DENSITY nV/√Hz	EFFECTIVE VOLTAGE NOISE µVrms		
		5MHz	10MHz	100MHz
$\overline{u_{R_F}^2}$	4, 07	9, 1	12, 9	40, 7
$\overline{u_{R_I}^2}$	1, 29	2, 9	4, 1	12, 9
$\overline{u_{OP}^2}$	2, 42	5, 4	7, 7	24, 2
$\overline{i_{OP+}^2}$	0, 33	0, 7	1, 0	3, 3
$\overline{i_{OP-}^2}$	3, 30	7, 3	10, 4	33, 0
$\overline{i_S^2}$	1, 79	4, 0	5, 7	17, 9
TOTAL		13, 8	19, 6	61, 9

TABLE III. Receiver Noise Performance.

As already stated, dividing the equivalent noise at the output by the transimpedance resistor value produces the equivalent input current noise. The following equation is used to calculate the S/N ratio, and Table IV shows the S/N ratio vs frequency:

$$S/N = 20\log\left(\frac{I_P}{I_{RMS}}\right) \quad (8)$$

FREQUENCY (MHz)	CURRENT NOISE (nA)	SIGNAL-TO-NOISE RATIO (dB)
5	13, 8	57, 2
10	19, 6	57, 2
100	61, 9	44, 2

TABLE IV. Signal-to-Noise Ratio.

When low-noise, wide-band amplifiers are combined with very low-noise discrete FETs, the results are not only lower noise but also a higher S/N ratio and only slightly smaller bandwidth. As shown in Figures 11 and 12, the discrete J-FET J308 at the input of the final transimpedance amplifier version improves the S/N ratio by about 5dB at 100MHz. The FET in front of the OPA621 functions as a source follower, but it is connected to the OPA621 and feedback loop in such a way that it does not change the basic impedance structure. The photon current flows to the FET gate and generates a voltage change. The source follower transfers the voltage variation to the noninverting input at a lower impedance. In its negative feedback loop, the op amp also reacts by varying its output voltage, which causes a current to flow through the feedback network until the source voltage equals the voltage at the noninverting input.

The source follower provides no voltage gain but enough current gain that the noise from the OPA621 is negligible. Since the first gain stage in a composite amp is the primary noise-producing element, the main noise source of the circuit presented here is the input current noise at the FET gate, which is about 1pA/√Hz for the J308 at 100kHz.

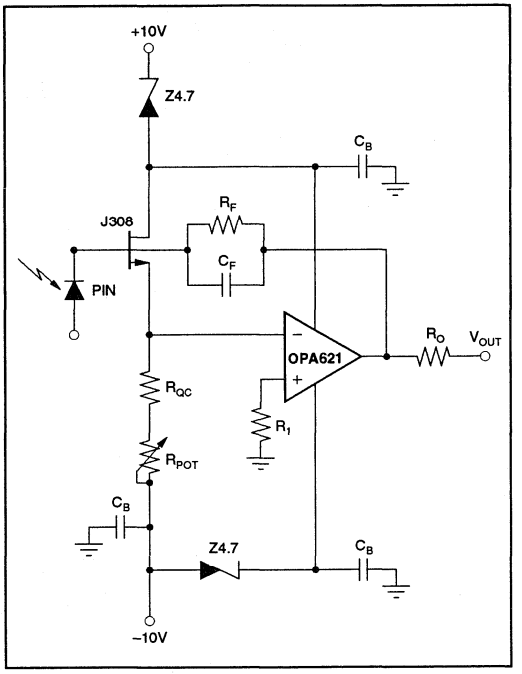


FIGURE 11. Receiver Circuit.

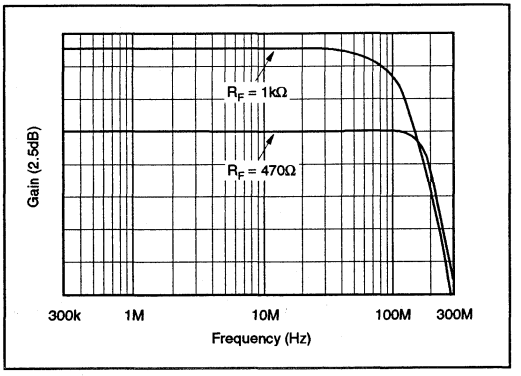


FIGURE 12. Receiver Bandwidth.

PARAMETER	VALUE	UNITS
Frequency	100	MHz
V_{NOISE}rms	36	µV
I_{NOISE}rms	36	nA
R_F	1	kΩ
S/N	48.9	dB

TABLE V. Summary of Noise-related Performance at 100MHz.

The resistor R_{QC} enables the user to adjust the FET bias point. To test the frequency response at the PIN-diode cathode, a generator provides a 10µA photo current, and an analyzer records the output vs frequency. The diode anode is connected to –15V in order to minimize the effective stray capacitance, which remains 5pF.

Two frequency response curves are shown in Figure 12. The top curve reflects the measurement using a 1000Ω transimpedance resistor; here the –3dB bandwidth is 110MHz. The bottom curve is for a 470Ω resistor, where the –3dB bandwidth is about 200MHz.

Table VI shows some test results for the fiber optic transmission system when the input signal is applied to the transmitter. The transmitter supplies the LED with a 35mA quiescent current and a ±25mA modulation current.

CONDITIONS	BW (MHz)	S/N (dB)	DG (%)	THD (%)
R_F = 470Ω w/o Preequalization	135	40.9	27	—
R_F = 1kΩ	100	44.2	27	—

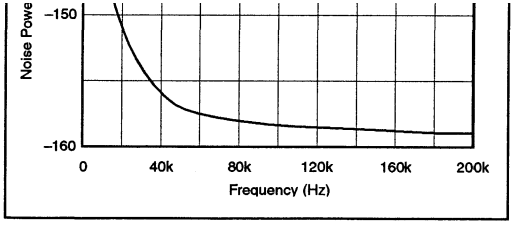


FIGURE 13. Noise Power vs Frequency.

AGC AMPLIFIER AND LINE DRIVER

Multiplication of analog signals has long been one of the most important nonlinear functions of analog circuit technology. Many signal sources, however, deliver weak, oscillating, and simultaneously wide-band signals. The PIN-diode current presented here is no exception, but it is equipped with an AGC amplifier to solve this problem. The AGC amplifier, in this case the OPA660, measures the output voltage, compares it to a reference voltage, and adjusts the multiplier control until the output has reached the set value.

The OPA660 is used in this configuration both as a two quadrant multiplier and as an amplifier. By varying its own gain, it keeps the output constant over a wide input voltage range. Figure 14 shows a simplified circuit diagram of the AGC configuration. The output signal of the transimpedance amplifier, which is 10mV for a 10µA input current and a 1kΩ R_F, is applied to the buffer input of the OPA660. It is configured as a differential amplifier with current output. The second input allows DC restoration of video signals, as will be shown later. The amplifier (OPA621) placed after the OPA660 converts the output current i of the multiplier into a voltage, while providing additional gain and drive capability. The peak detector and comparator compare the typical ±1.4V video output voltage with the +1.4V reference. The resulting difference in voltage controls the gate of the FET. The gate varies the FET drain current, which is also the OPA660 quiescent current, until the internal OPA660 transconductance has compensated the varying input voltage.

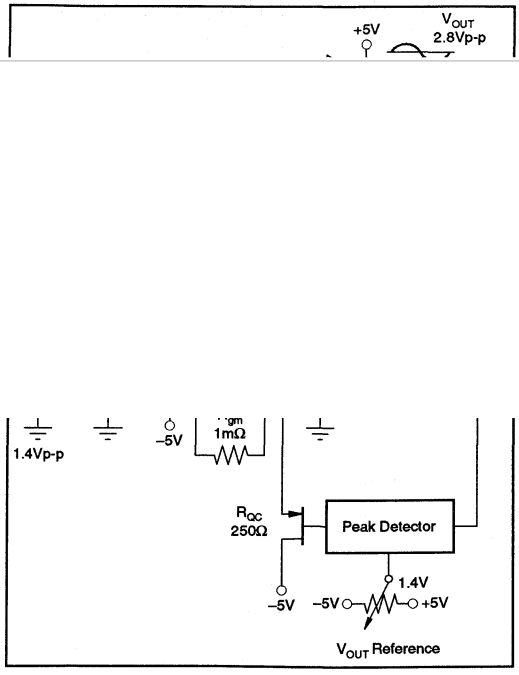


FIGURE 14. Automatic Gain-Controlled Amplifier.

Figure 15 shows the detailed AGC amplifier schematic. The output amplifier is split into an OPA621 and OPA623, reducing the gain requirement for each individual op amp in order to increase the achievable bandwidth. Unfortunately, it is not feasible to replace the voltage-feedback amplifier OPA621 with a wider bandwidth current-feedback op amp because the feedback resistance is 20kΩ. In current-feedback amplifiers, the size of the feedback network determines both the closed-loop and the open-loop gain. Thus in prac-

tice, the larger the resistor, the lower the bandwidth. The peak detector and comparator are made up of discrete components. For a more integrated solution, the differential amplifier can be replaced by an op amp.

Besides the automatic signal control, the circuit presented here also makes it possible to control and adjust the DC level of the output voltage. This feature is useful for video applications in which the blank level, or level at no luminance signal, is defined as 0V. The sync signals are defined from zero to –0.3V, and the luminance ranges from zero to +0.7V. To transmit a video signal over a coax cable, an amplifier amplifies this signal by 2. The whole procedure is called DC restoration or black level clamping. A video signal is a signal that appears periodically between sync pulses. The signal remains at black level for a short time after each horizontal signal pulse, which controls the line information. During this short time, a gated error amplifier compares the output level with the reference voltage (GND) to correct the output to GND. The OPA623 amplifies the signal from the preamp and drives the sync separation circuit LM1881. It provides the necessary clamp pulse shortly after the II sync. The buffer, BUF601, applies the clamp pulse II_C to the restoration circuit CA3080, which is switched on and generates the correction voltage that is then stored in C_4. The comparison stops when the clamp pulse returns to logic "low", but the capacitor keeps the output voltage at GND as a biasing point until the next clamp pulse is applied.

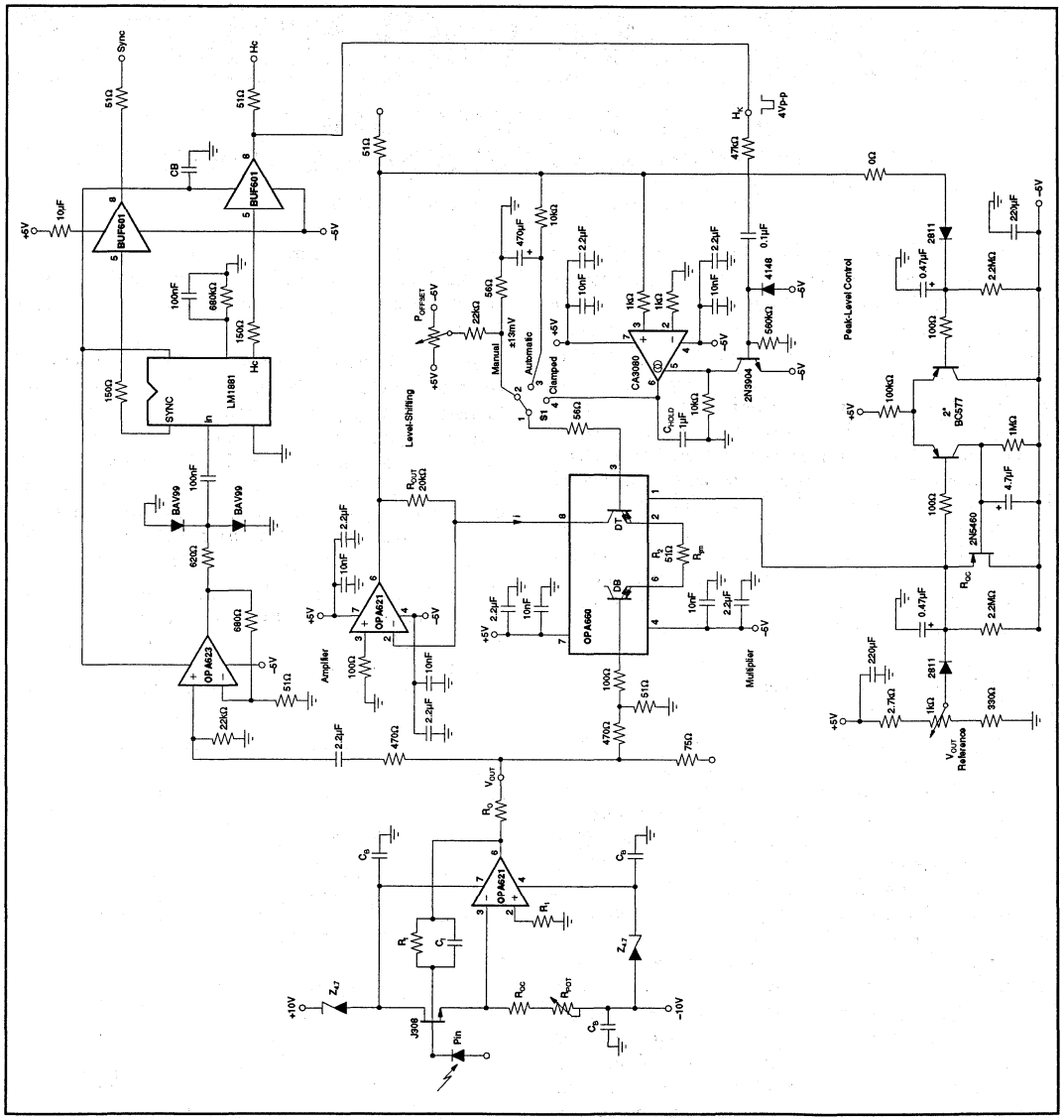


FIGURE 15. Circuit Schematic of the Transimpedance and AGC Amplifiers.

BURR-BROWN® APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

DRIVING VIDEO OUTPUT STAGES WITH MONOLITHIC INTEGRATED AMPLIFIERS

By Christian Henn, Burr-Brown International GmbH

Increasingly powerful computers and the rapidly expanding use of picture processing and CAD/CAM systems in almost all industry branches have combined to generate a greater and greater demand for higher resolution graphic monitors. Controlling the video output stages of these graphic monitors is a key to producing such high resolutions. Until recently, only highly complex, expensive systems have been available to drive hybrid video output stages. But using the monolithic amplifiers OPA623 and OPA2662 from Burr-Brown, new methods are possible that make complicated solutions a thing of the past. The OPA623 allows rise (t_{RISE}) and fall (t_{FALL}) times of 3ns and 2.3ns, respectively, at the output, while the OPA2662 is even more impressive at t_{RISE} = 2.4ns and t_{FALL} = 2.15ns. With this kind of performance, the OPA623 and OPA2662 can be used in graphic systems with resolutions of 1600 x 1200 pixel and more.

HIGH-RESOLUTION PICTURE PROCESSING SYSTEMS: AN OVERVIEW

The various standard resolutions range from the commonly used VGA standard with 640 x 400 pixels to the super VGA with 800 x 600 pixels to CAD/CAM and radar systems with over 1600 x 1200 pixels. But while radar and computer tomography systems generally use high-resolution 1600 x 1200 color graphic monitors, monochrome displays with 2k x 2k resolution and 500MHz bandwidth are now in development. To achieve such high resolutions, the monitors use horizontal deflection frequencies for electron rays between 64kHz and 96kHz, as well as data rates between 100Mbit/s and 250Mbit/s, which are read out from the video RAM card. Raising the vertical deflection frequency to more than 70Hz causes the horizontal frequency and data rate to increase while the resolution remains the same. Controlling the pixels by the video controller adds to the demands on the video amplifier, and significantly increases the power consumption during video signal processing. Instead of a continuous video signal, the video card produces pulse sequences that return to zero between every two pulses. The amplitude of each pulse is equal to the luminance of the respective color (R, G, B). An additive optical mixing process produces the correct color on the screen. For this reason, displaying the color white at the maximum amplitude is the toughest job for the video amplifier in graphic monitors.

Table I summarizes the various timing requirements necessary to produce the most commonly used graphic formats. The $T_{H\ ACTIVE}$ can be calculated by multiplying the horizontal cycle time by 0.8, and it includes time for the electron ray to return from the right side to the left side of the screen during the horizontal retrace time. When calculating t_{RISE} and t_{FALL}, it was assumed that each was one third of the pixel time. The –3dB bandwidth (f_{-3dB}) is dependent upon the rise time and can be calculated as $0.35/t_{RISE}$.

The video signal levels at the interface between the video card and monitor are standardized at +0.7Vp for the video signal and –0.3Vp for the synchronization pulse. A high-resolution cathode ray tube (CRT) functions with bias voltages between +65V and +75V and a modulation voltage of

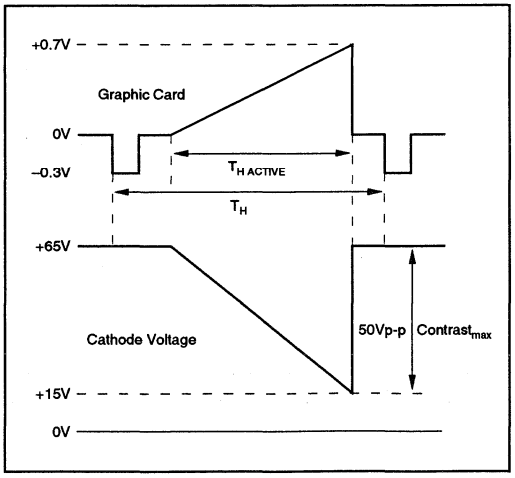


FIGURE 1. Pulse Sequences from a Signal Graphic Cathode.

SYSTEM STANDARDS	RESOLUTIONS H	V	f_H (Hz)	f_V (Hz)	t_H (µs)	t_{ACTIVE} (ns)	TIME/PIXEL (ns)	PIXEL/CLOCK FREQUENCY (Hz)	$t_{RISE/FALL}$ (ns)	–3dB BW (Hz)
VGA	640	400	31.5k	70	31.74	25.39	39.67	25M	13.22	26.47M
Super VGA	800	600	38k	70	26.31	21.04	26.30	38M	8.76	40M
CAD/CAM	1280	1024	64k	60	15.62	12.49	9.75	102M	3.25	107M
Work Station	1600	1200	76k	70	13.15	10.52	6.57	152M	2.19	160M

TABLE I. Timing Requirements.

up to 50Vp-p with high luminance densities between the cathode and ground. For sufficient contrast, the total gain between the input and cathode must be between 70 and 166, depending upon the contrast control method in use. The cathode is a capacitive load of about 8pF, which rises to at least 12pF when combined with stray capacitances from the supply lines, connectors, and required protection circuitry.

Gain	70 to 166
Output Amplitude	$50V_{MAX}$
t_{RISE}/t_{FALL} (40V, 12pF)	2ns
Driver Current	±300mAp-p
Slew Rate	25000V/µs
Linearity	1%

TABLE II. Video Output Stage Requirements for a 1600 x 1280 Graphic System.

VIDEO AMPLIFIER CONCEPT

Since the development of the first monitors, various types of amplifiers have been designed according to specific requirements and applications. The type of amplifier structure shown in Figure 2 has become the standard for high-grade monitors.

The amplifier at the front end of the circuit is equipped with a simple transconductance multiplier to control the signal. Since this type of multiplier has a small linear modulation range, it is necessary to reduce the signal in the amplifier from 0.7Vp to 0.3Vp. The following driver stage amplifies the signal 8 to 15 times and drives the output stages at approximately 4Vp-p. The output stage then amplifies the signal again to 50Vp-p max and provides the necessary driving power to charge the cathode and stray capacitances. At the back porch that occurs at the beginning of each line after the horizontal switch, the control circuit compares the cathode voltage to an adjustable bias and corrects any deviations from the bias. Depending on the type of amplifier structure, the bias point control drives either the input of the driver amplifier or the output stage. The entire video amplifier then reverses the video signal. A 0V signal at the input, which appears as a dark spot, is converted at the cathode to a voltage between +65V and +75V, depending upon the bias point of the cathode. A +0.7V signal, which corresponds to maximum luminance, is converted with maximum contrast control to a 50V modulation hub between the CRT bias point and ground. Figure 1 illustrates these conversions.

VIDEO OUTPUT STAGE

Until a few years ago, the standard circuit for video output stages was a cascode stage with or without a subsequent complementary emitter follower. The advantages of this circuit are that it is easy to design and avoids the Miller effect (harmful collector-base capacitances) in the amplifying transistor. Inductances in series to the collector resistor and RC parts parallel to the emitter resistor allow users to adjust the circuit as required by their particular application. The disadvantages of the cascode stage are its asymmetrical transient response and high power dissipation at short rise and fall times.

We conducted several experiments with various configurations to test the ability of the OPA623 and OPA2662 to control a discrete cascode stage. As shown in Figure 3, a few of these configurations failed because there are no discrete cascode transistors effective for this application. The integrated dual current source OPA2662 can produce a charge current of up to 300mA in the emitter of a transistor like the BFQ262 at rise times of about 2ns, but internal transistor and emitter resistances and any package stray capacitances limit and delay the current conversion from the emitter to the collector of the BFQ262.

Further tests were done using an output stage manufactured on a hybrid process, and these tests were successful. Figure 6 shows the schematic of the output stage, which is available from Philips under the part number CR3425. Using the test configuration shown in Figure 7, it was possible to check the performance of the hybrid circuit by itself. The pulse generator HP8130A drives the output stages via a terminated 50Ω line with rise and fall times of 0.7ns each and a signal amplitude of 4Vp. The output stage is supplied from 80V, and 60mA quiescent current flows when no signal is being applied. The rise and fall times measured at a 50V signal hub and 12pF load capacitance are impressively low at 2.15ns. Figure 8 shows the pulse responses at 10ns/div and 2ns/div.

AN ALTERNATIVE METHOD OF DRIVING THE OUTPUT STAGE

With the hybrid circuit CR3425, a cost-effective, high-performance circuit is now available for high-resolution graphic monitors that effectively controls the output of the video output stage. Now, however, the problem is controlling the input of the video output stage. What we need is a

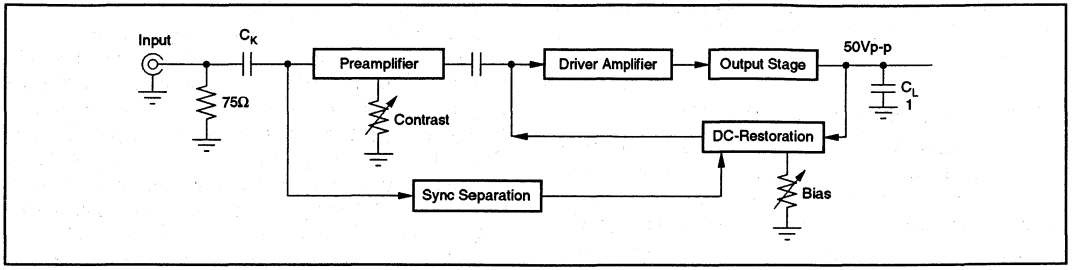


FIGURE 2. Video Output Stage Requirements for a 1600 x 1280 Graphic System.

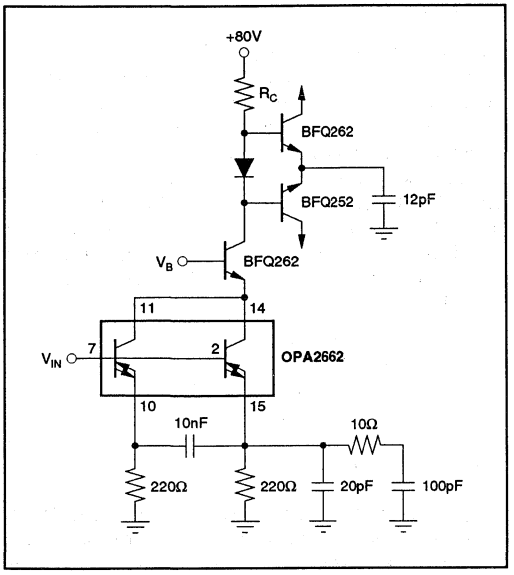


FIGURE 3. Video Output Stage.

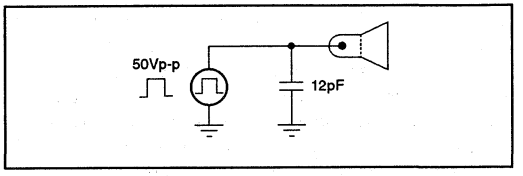


FIGURE 4. Cathode Voltage Control.

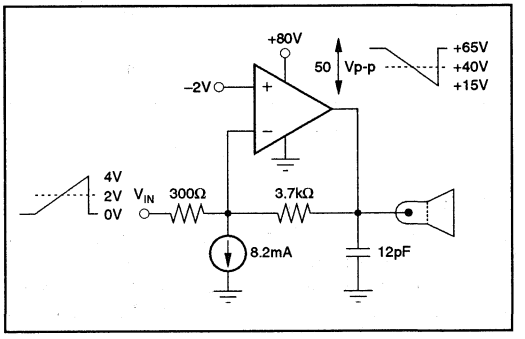


FIGURE 5. Basic Configuration of the Driver Circuit.

driver amplifier that takes the pulse after contrast control and amplifies it with no edge slopes, as well as controlling the complex input resistance in the output stage with a slew rate of over 1500V/µs for positive and negative signal transitions. The hybrid driver amplifiers currently on the market function only with NPN transistors in class A operation. Nonfeedback amplifiers are relatively low-cost but have high power consumption and, more importantly, can hardly produce the 1280 x 1024 resolution required for positive signal edges.

The Current-Feedback Amplifier OPA623 and the Dual Current Source OPA2662, two monolithic ICs manufactured on a complementary bipolar process, offer reasonably priced, effective alternatives. These new ICs differ both in performance and in manufacturing costs. They are not, however, limited to video output stage control. The problem of controlling an input or load resistance is a much more general dilemma present in a wide variety of applications. The real trick is to find amplifiers that can operate stably with complex loads, have low power consumption, and are capable of charging load capacitances with high currents in as little time as possible. In these categories as well, the OPA623 and OPA2662 prove themselves extremely viable options.

DRIVER AMPLIFIER USING THE OPA623

The Wide-Band Current-Feedback Amplifier, OPA623, is available in 8-pin DIL and SO packages and delivers up to ±70mA output current at a supply voltage of ±5V and low quiescent current of 4mA. Figure 9 shows the driver circuit using the OPA623. The OPA623 amplifies the video signal

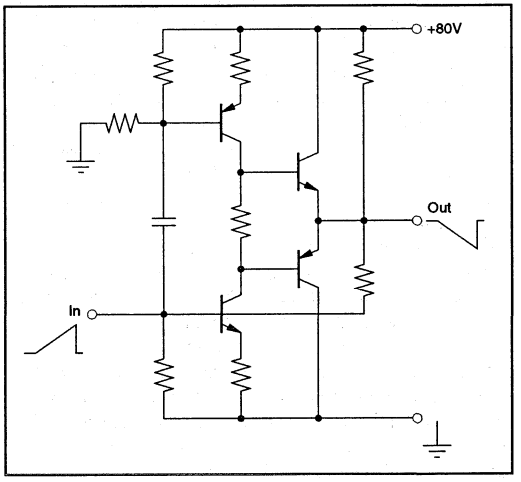


FIGURE 6. Internal Structure of the Video Output Stage CR3425.

from 0.8Vp to 4Vp and drives the complex input resistance of the CR3425 output stage. Figure 10 shows the pulse response at the OPA623 output, and Figure 11 that at the output of the video output stage. The rise and fall times of the OPA623 are 1.85ns and 1.95ns, respectively. Thus the OPA623 can drive complex loads of 24Ω + 287Ω || 50pF at an output voltage of 4Vp and slew rate of about 1700V/µs (ca. 4Vp • 0.8ns/1.9ns). Using the OPA623, the output of the video output stage CR3425 can charge the 12pF load capacitor with 40V in 3ns and discharge 40V in 2.3ns. In contrast

to direct control, control using the OPA623 results in an edge slope of 0.85ns for the rising edge and 0.15ns for the falling edge.

DRIVER AMPLIFIER USING THE OPA2662

The second test used the Dual Diamond Transistor OPA2662 to drive the video output stage. This new wide-band IC contains two voltage-controlled current sources (transconductance amplifiers) in a 16-pin package. Each current source delivers or pulls up to ±75mA at its high-impedance collector. The voltage at the high-impedance base appears in low-impedance form at the emitter and produces a current flow toward ground via the emitter resistor. This current is then reflected by a factor of 3 to the collector. As shown in Figure 12, it's easy to connect two current sources in parallel, which produces driving power of ±150mA. A compensation network connected to the emitters provides even more current during the charge phase. Figure 13 shows the excellent test results using this configuration. At the output of the CR3425, the design produces rise and fall times of 2.4ns and 2.15ns, respectively, with cathode voltage variation of 50Vp-p. This variation is the maxi-

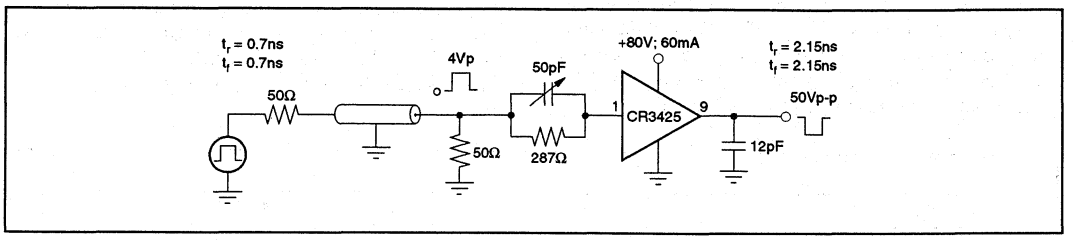


FIGURE 7. Driver Circuit Using a Pulse Generator.

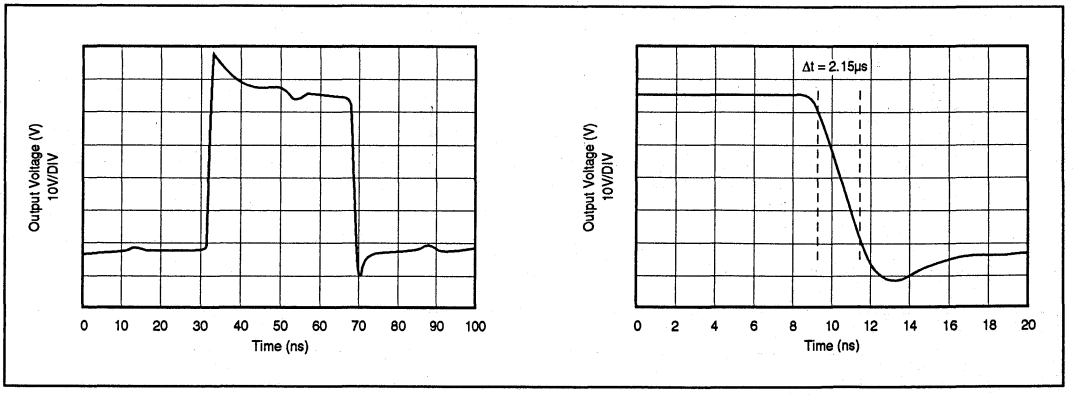


FIGURE 8. Test Circuit Response.

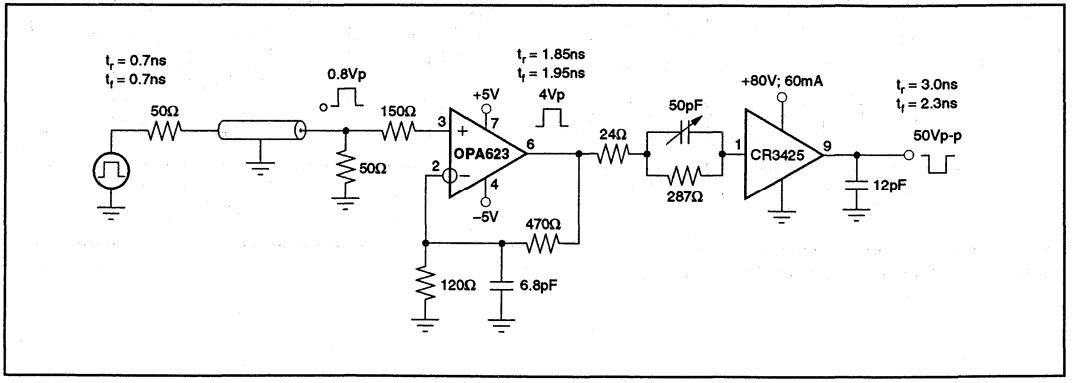


FIGURE 9. Driver Circuit Using the OPA623.

mum possible cathode modulation, during which most picture tubes are already in overdrive. Reducing the maximum output voltage lowers the rise and fall times to less than 2ns, making it possible to process video pulses of 6ns. The shorter the pulse, the more important it is to achieve sufficient cathode voltage, since high resolutions are accompanied by high horizontal deflection frequencies so that the turnaround time of the electron ray at the phosphor point becomes shorter and shorter. The rise time of a phosphor point is the time until it converts to the electron charge into a visible light (R, G, or B).

In comparison to direct control of the output stage by a generator, when controlled by the OPA2662, the rising edge has a small additional edge slope of 0.25ns and the falling edge is driven exactly as fast as with direct control. Considering that most signal generators are quite expensive, this comparison speaks quite well for the OPA2662.

CONCLUSION

Only in the last few years has it become possible to use integrated amplifiers in video signal processing with high-resolution monitors. New developments in circuit technology and IC manufacturing processes, as well as the rapidly increasing demand for low-cost displays, have combined to accelerate advances in video design. Today, integrated RBG video amplifiers are already available with a bandwidth of 100MHz. In addition to amplification and contrast control, these amplifiers offer additional functions such as clamping, blanking, and sync separation, and they can also drive the output stage.

Both driver circuit configurations shown here allow video output stage control that is less integrated but also more powerful, and the configurations achieve a level of performance previously possible only with complex, large, and

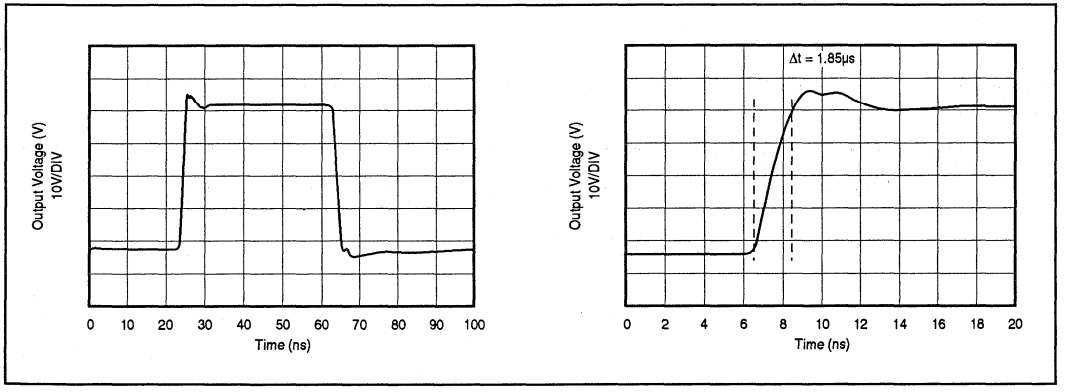


FIGURE 10. OPA623 Output.

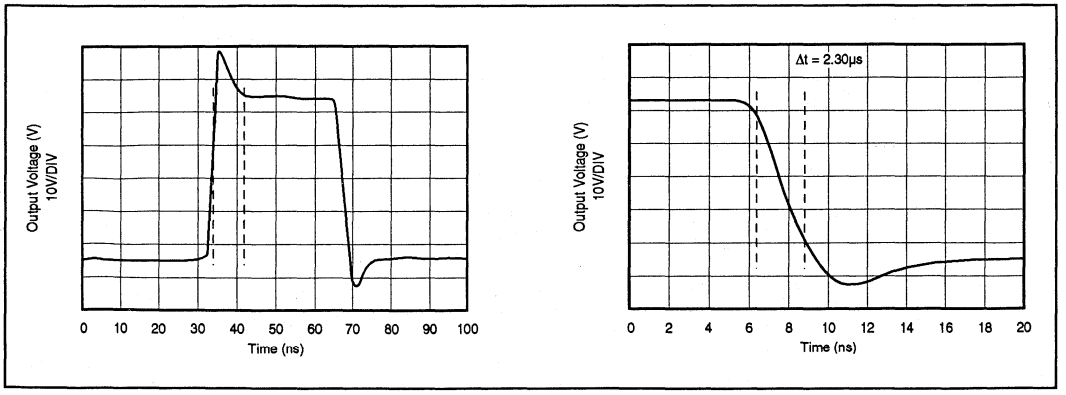


FIGURE 11. Response of the Test Circuit Shown in Figure 6.

expensive hybrid circuits. The lower cost, smaller driver circuit using the OPA623 can be used for 1600 x 1280 resolutions, while the OPA2662 can be used for applications requiring resolutions of up to 2k x 2k. It should be noted, however, that at 2k x 2k both the driver circuit and the video output stage operate at their performance limit. At frequencies over 100MHz, separation of the three color channels in different video amplifiers is the only effective way to keep the crosstalk between the channels to less than 30dB. Finally, a comparison of the two driver circuits demonstrates the superiority of a high-impedance current source over a low-impedance voltage source when controlling low-impedance, capacitive loads. Although the OPA623 with 350MHz appears at first glance a better choice than the OPA2662 with 200MHz, the current-source output and higher drive capability of the OPA2662 give it an edge in practice.

The next step will be to assemble both the monolithic integrated driver amplifier and the hybrid video output stage on the same substrate.

Both driver circuits are available from Burr-Brown as assembled demo boards so that you can test the configurations for yourself.

REFERENCES

OPA623 Product Data Sheet
Burr-Brown

OPA2662 Product Data Sheet
Burr-Brown

CR3425 Product Data Sheet
Philips

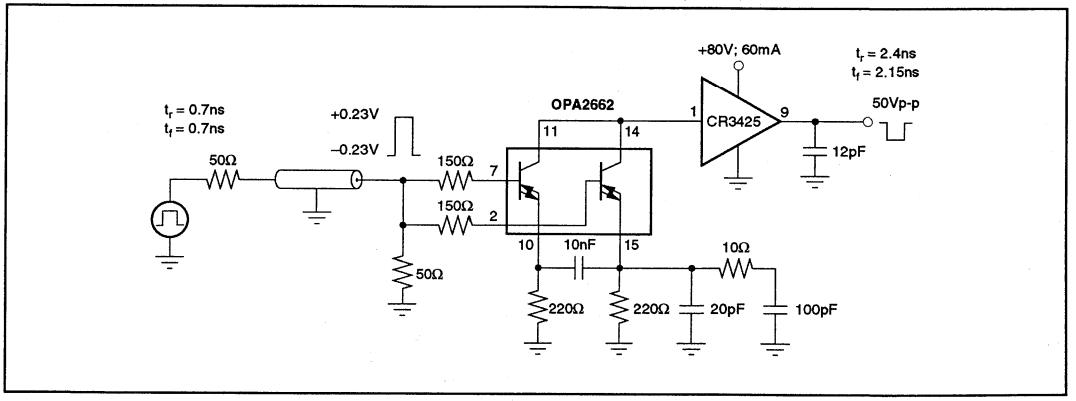


FIGURE 12. Driver Circuit Using the OPA2662.

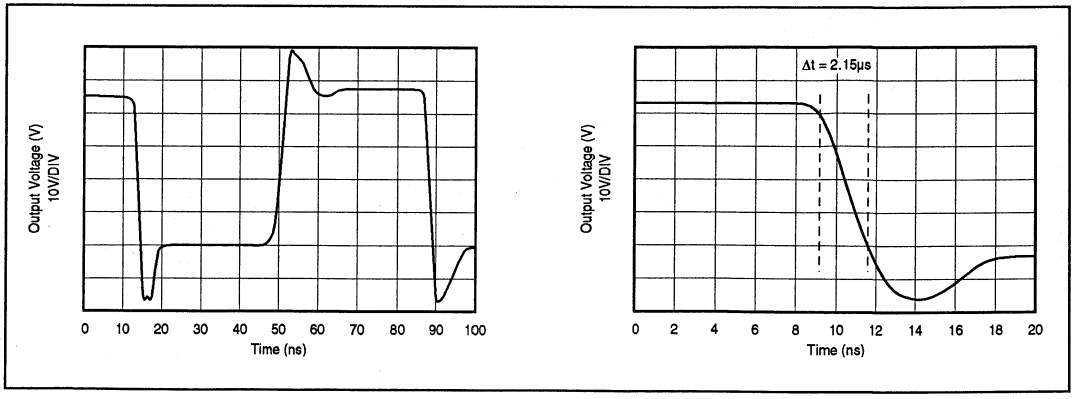


FIGURE 13. Test Circuit Response Curves.

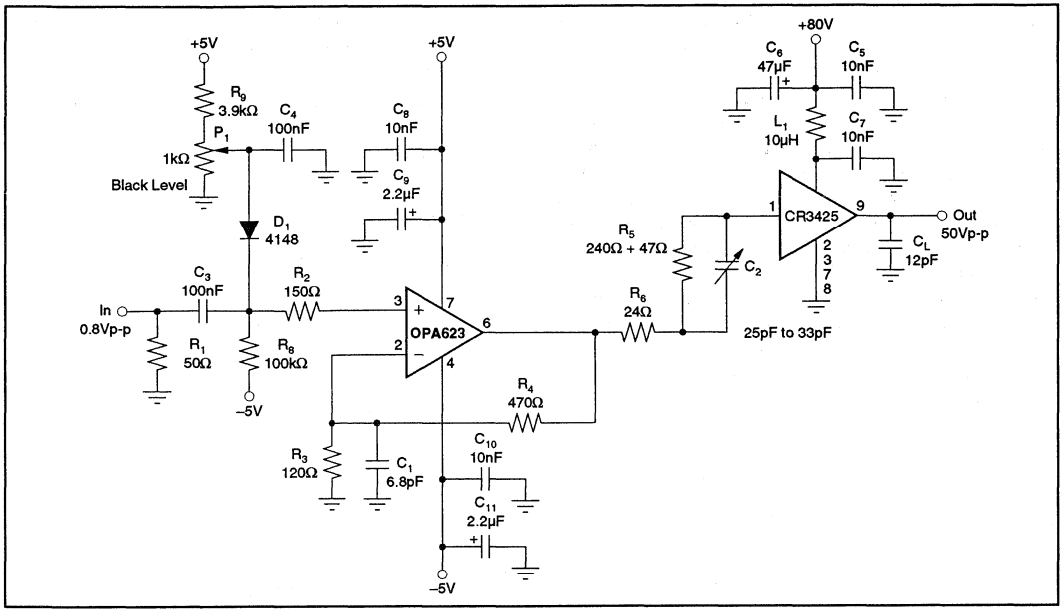
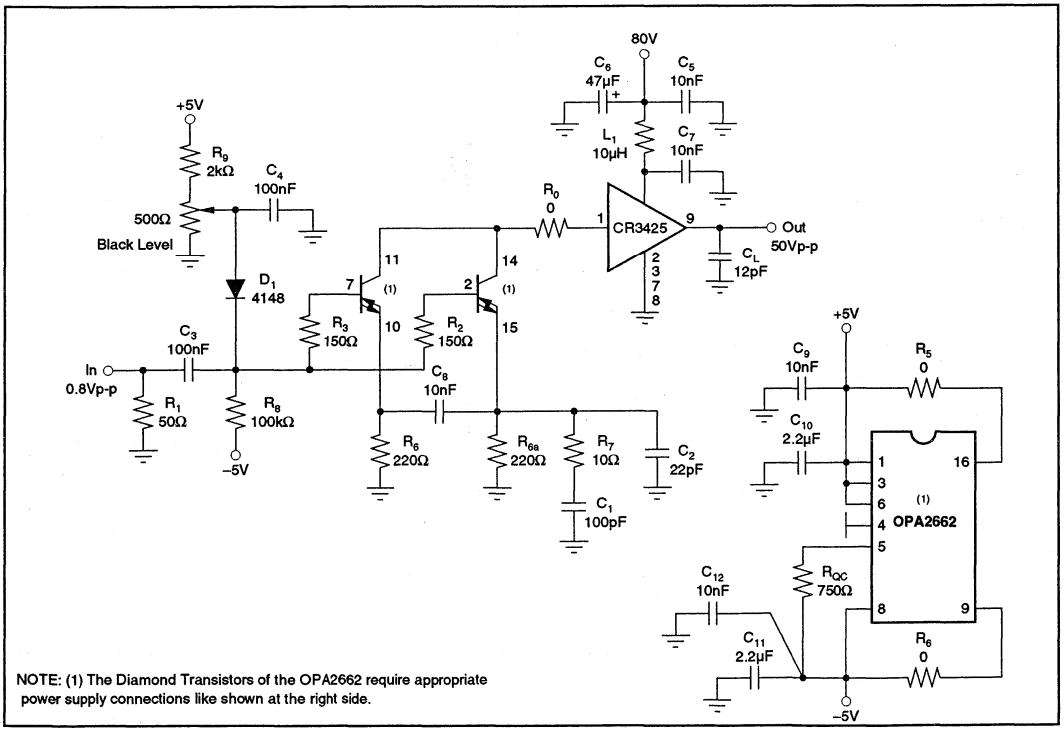


FIGURE 14. Driver Circuit 1.



NOTE: (1) The Diamond Transistors of the OPA2662 require appropriate power supply connections like shown at the right side.

FIGURE 15. Driver Circuit 2.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

BURR-BROWN® APPLICATION BULLETIN

Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

SWOP AMPS SIMPLIFY RF SIGNAL PROCESSING

When designing high performance systems for RF and video applications requiring amplifiers, multiplexers, or programmable gain amplifiers, finding the right components to do the job is not simple. A pair of SWOP amps from Burr-Brown, the OPA675 and OPA676, open the door to high speed without the headaches. These devices are true operational amplifiers with a built-in switchable front end, hence the name SWOP amp, for SWitchable input OP amp. The resulting integrated circuit functions as a fast settling wideband op amp with a DPDT switch on the two input pins. Using a SWOP amp makes it easy to switch from one channel to another in nanoseconds.

Figure 1 shows the OPA676 multiplexing two input signals into a single output. The gain for each channel is set by external feedback resistors according to standard op amp design techniques. The inverting input pins for both input stages are connected to the same feedback network, guaranteeing that the gains will be identical for both channels without requiring precision matched resistors.

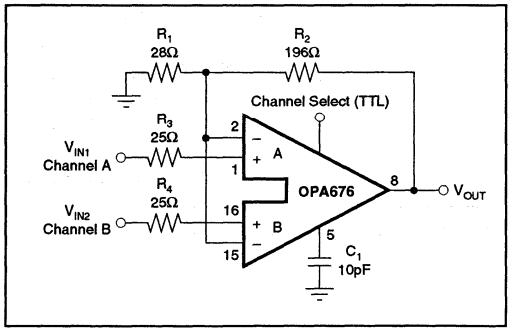


FIGURE 1. Two-Input Multiplexer with a Gain of +8V/V for Each Channel. Gain is identical for each channel without precision resistors. Bandwidth is greater than 100MHz.

Either channel may be configured as inverting or noninverting. If different gains are desired for the two channels, separate feedback networks may be used as shown in Figure 2. Note that the compensation node is common to both channels. The capacitor must be large enough to make the channel with the lowest gain stable. For this reason, channel B in Figure 2 has R_7 added across the inputs to make the noise gain equal to +10V/V, although the signal gain is +2V/V. This allows the SWOP amp to be compensated with 6.5pF for a gain of +10V/V, instead of the 35pF that would be required for a gain of +2V/V. The noise gain calculation is:

$$\text{Noise Gain}_{\text{CHANNEL B}} = 1 + R_6/(R_5 \parallel R_7)$$

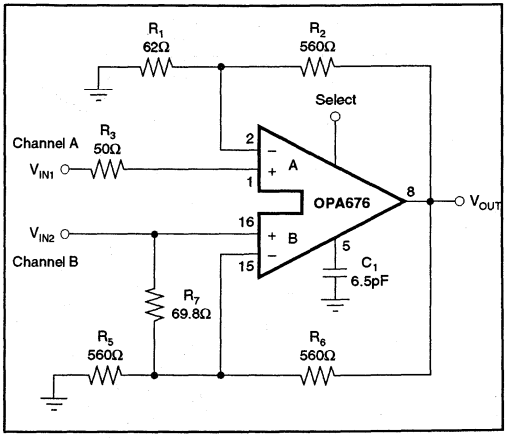


FIGURE 2. SWOP amp with a Gain of +10V/V for Channel A. Gain of +2V/V for channel B. Connecting both inputs together yields a programmable gain amplifier.

By selecting different gains for each channel and connecting the inputs together, a programmable gain amplifier is realized. The selectable input amplifier can also function as a gated amplifier, for noise blanking with RF signals, or a return to zero deglitcher for digital-to-analog converters. Filtering may be added to any of the circuits shown here, using standard op amp filter designs.

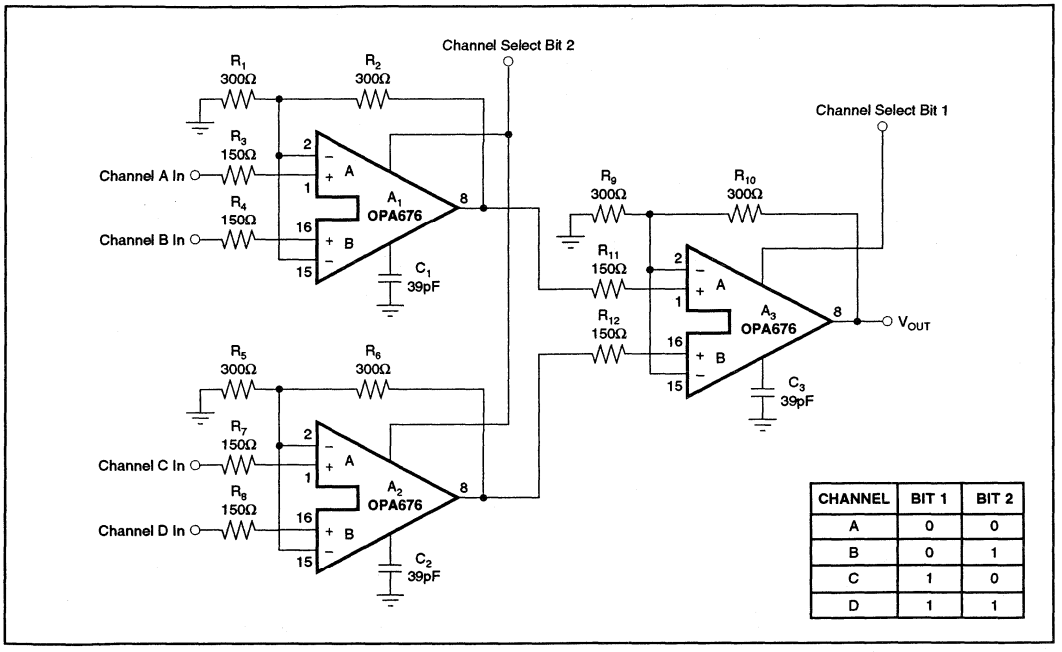
Figure 3 shows a four channel MUX made with three SWOP amps. The circuit for each amplifier is shown in Figure 1 with SWOP amps A_1 and A_2 used to MUX the four channels into two.

A_3 performs the final multiplexing down to one output channel. The circuit uses two bits for channel select, as shown in the table in Figure 3. The second bit selects

channel A or B on amplifier A_1 and channel C or D on amplifier A_2. The first bit selects side A or B on amplifier A_3, which selects the output of amplifier A_1 or amplifier A_2, respectively.

Using regular operational amplifier design techniques, any of the four channels may be configured for any inverting or noninverting gain. Note that the SWOP amp is optimized for gains greater than 2. Filtering can also be added to one or more channels. When selecting the compensation capacitor for the three amplifiers, several things should be considered for optimum performance. Split up the gain for each channel evenly between the first bank of SWOP amps (A_1 and A_2) and A_3. This allows all the amplifiers to be compensated for maximum bandwidth. For a wide range of gains, try to group high gains on A_1 and low gains on A_2. This allows A_1 to be compensated lightly for the high gains, maximizing bandwidth.

Another technique for optimizing the bandwidth for different gains is to make a low-gain channel by placing the first SWOP amp in a gain of 8 to 12 and preceding it with an attenuator. This will degrade SNR, since the input signal is attenuated before it is added to the first SWOP amp's noise. This is usually not a problem because the SWOP amp exhibits only 2.3nV/√Hz input noise.



CHANNEL	BIT 1	BIT 2
A	0	0
B	0	1
C	1	0
D	1	1

FIGURE 3. A Fast, Four-input Multiplexer Using Three SWOP amps. $V_{OUT} = 4 \cdot V_{IN}$ for the selected channel. Bandwidth is 70MHz.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

BURR-BROWN® APPLICATION BULLETIN

Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

OPERATIONAL AMPLIFIER MACROMODELS: A COMPARISON

By Bonnie Baker (602) 746-7468

All major competitors in the operational amplifier markets are providing their customers Spice-based macromodels. These models give the designer a tool to do initial characterization and a limited amount of system troubleshooting. In the interest of faster simulation times and lower CPU memory requirements, macro topologies have been developed to simulate a majority of the op amp's performance characteristics. Several different approaches to creating macromodels have been used, each producing a macro with its own set of strengths and weaknesses. Circuit simulations have become increasingly important to the systems level designer. By using macros, the designer can quickly determine gross limitations of their design and correct potential problems in the circuit quickly at the computer terminal. Although it is not recommended that circuit simulation replace the bread board, many costly design problems can be quickly identified during the simulation cycle. By using a macromodel as a simulation tool, the designer may be able to shorten the design cycle of their circuit. This, of course, assumes that the model's level of accuracy is adequate for the design's constraints and trade offs. If the systems designer is aware of the capabilities and limitations of the macro that has been selected for the simulation phase, the entire design cycle can be significantly reduced. Many of the macro's limitations can also be overcome with easily implemented enhancements to the basic macromodel architecture, depending on the specific application requirements. A good selection of the correct model with appropriate enhancements enables the designer to use the op amp macromodel as an effective tool in system level circuit design.

Historically, circuit simulation tools, such as SPICE[1], were developed for the integrated circuit designer. SPICE uses detailed mathematical formulas, which emulate the behavior of actual devices. The IC designer uses simulation tools, such as SPICE, extensively during the circuit design cycle. The level of sophistication that the IC circuit designer requires is that every element is simulated as closely to actual performance as possible. As a consequence, the majority of elements in the simulated circuit are non-linear elements, such as bipolar transistors, field-effect transistors, etc. Because of the complex behavior of these non-linear elements in the Spice simulation environment, these elements require more simulation time and computer memory. With increased integrated circuit complexity, performance and size, simulation time and computer memory have become critical simulation constraints for the software and systems used by the IC designer.

This limitation has prevented the systems level designer from taking full advantage of the same simulation tools. As a result, macros have gained popularity as an alternative tool for circuit simulation at the systems level. Op amp macros are designed to model specific, predetermined amplifier characteristics. When Spice is used as the preferred software, the op amp macro is typically developed with one of two basic design approaches.

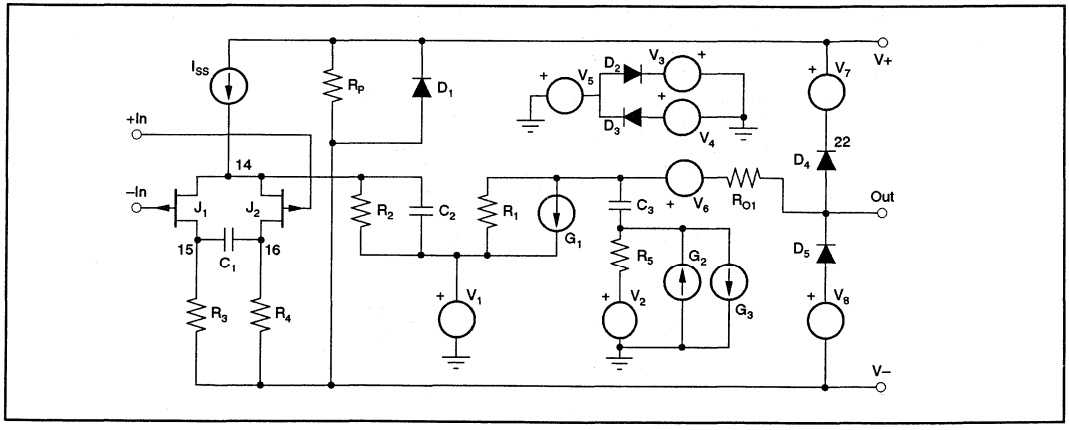


FIGURE 1. Boyle Macromodel Used to Simulate Operational Amplifiers.

MACROMODEL DESIGN APPROACHES

The first basic macromodel design approach involves reducing the complexity of the circuit. For example, the input stage of an op amp can be reduced to a differential pair with a resistive load, biased with a current source. The actual op amp could have a cascoded differential input with active load and the current source biasing the input stage would be built using a transistor that would have the non-linearities associated with early voltage and collector resistance, etc. Throughout the macromodel circuit, transistors that are deemed non-critical are replaced with linear elements, such as current sources, resistors, etc. The reduction in complexity reduces the number of nodes in the circuit as well as the number of non-linear devices, both of which will reduce simulation time. To reduce simulation time even further, the transistors are as near to ideal as possible. This is done by reducing the number of transistor model parameters. The obvious benefit of this macromodel design approach is a reduction in simulation time; however, op amp performance is compromised to some extent. For example, the input stage of the model described does not model the common-mode input range of the amplifier properly.

A second method that is used in macromodelling is the build method. When this method is used, the designer of the macro characterizes the performance of the op amp and then builds the macro out of ideal linear elements, such as resistors, inductors, capacitors, dependent sources and independent sources. A good example of this topology would be the op amp hybrid pi-model where the input stage of the amplifier is a resistor. The voltage across that resistor is sensed by the gain stage, etc. The simulation time of this type of model is significantly faster than the first macromodel design method; however, the op amp performance is compromised to a great extent with this approach.

THE BOYLE OP AMP MACROMODEL

The Boyle Op Amp Macromodel[2] was designed using the simplification method to design the input stage and the build method for the remainder of the macro design. As shown in

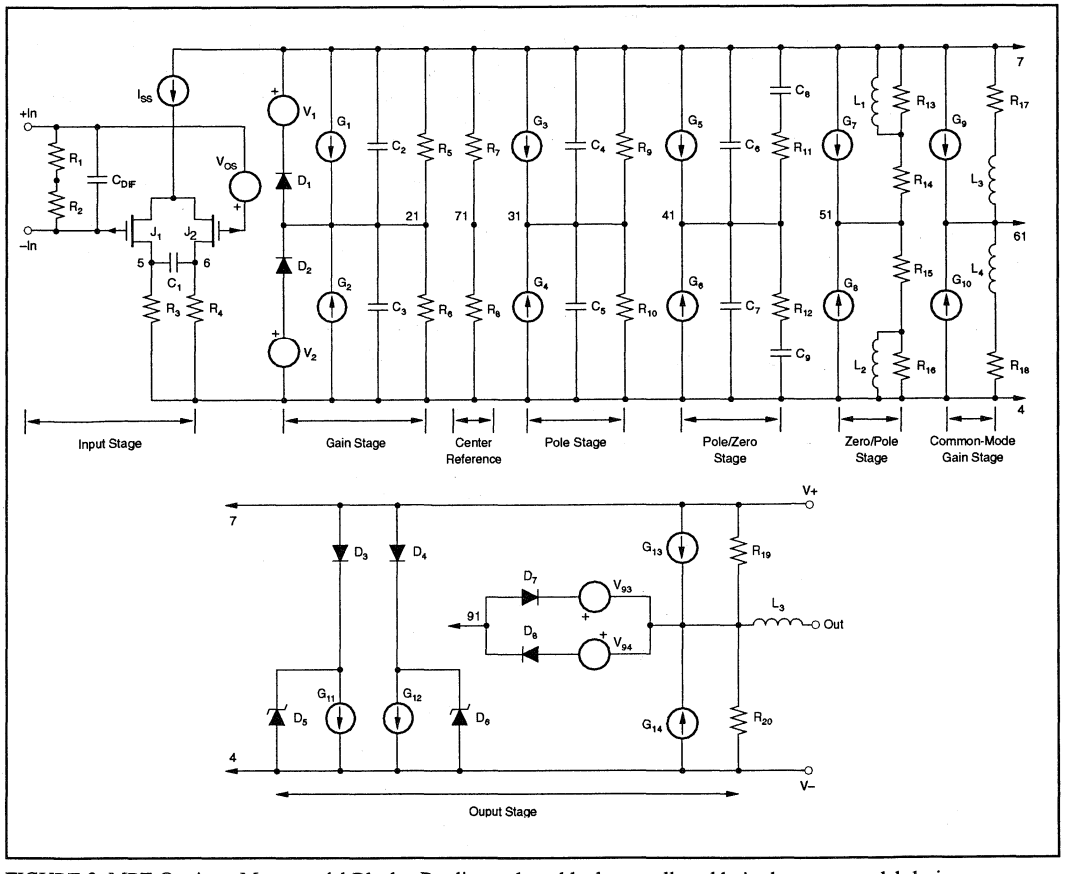


FIGURE 2. MPZ Op Amp Macromodel Blocks. Duplicate phase blocks are allowable in the macromodel design.

Figure 1, the only transistors in the Boyle model are used for the input differential pair of the op amp. All other elements are linear devices with the exception of a few diodes that are used as clamps. The ac parameters that this model topology simulates are slew rate, unity gain frequency, gain/phase for a one or two pole amplifier and a simplified ac output resistance. DC characteristics modelled are quiescent current, short circuit output current, output voltage swing maximums and minimums, input bias current, common-mode rejection ratio, and dc output resistance. The Boyle macromodel performance characteristics listed above suffice for many general applications. However, temperature performance, common-mode input range, offset voltage, offset current, input protection, power supply rejection, noise, THD, input impedance, good ac output resistance, and change in supply current versus supply voltage are a few of the more important parameters that are not modelled with the Boyle macro topology. Several op amp vendors have chosen to design their macros around the Boyle topology. Of the companies using the Boyle model that were researched, all added enhancements to the Boyle model to include a few more operational amplifier performance features.

THE MULTIPLE POLE/ZERO MACROMODEL

Another popular topology using both macromodelling methods is shown in Figure 2. The model shown in Figure 2 and the Boyle model (Figure 1) have identical input stages, but all of the remaining stages are different. This topology evolved from several sources[3,4] and is named after the midsection of the model, multiple pole/zero or MPZ. The midsection of this model can be expanded to include additional poles, pole-zero, or zero-pole stages. The MPZ macro has the same dc performance characteristics as the Boyle model as well as input offset bias current, input offset voltage and input differential impedance. The ac parameters that this model topology simulates are slew rate, unity gain frequency, gain/phase for a multiple pole/zero amplifier, CMRR versus frequency, and a simplified ac output resistance. In addition, the MPZ macro models change in quiescent current versus change in supply voltage, has no ground reference, and splits the output current between the supplies instead of sinking and sourcing from ground. A few of the MPZ limitations are a lack of temperature performance, poor modelling of common-mode input range, no input protection circuitry, no power supply rejection, no noise, no THD, and the ac output resistance is modelled with a one zero system.

THE BOYLE MACROMODEL VERSUS THE MPZ MACROMODEL

When comparing op amp macro performance, there are two simulation characteristics that are critical to the systems designer. The macro must model the electrical performance of the op amp in the designer's application of interest, and secondly, the macro must perform the simulation in a reasonable amount of time using a reasonable amount of computer memory.

When comparing the electrical performance of the Boyle model versus the MPZ model, the MPZ model provides several additional performance characteristics that the Boyle does not. For instance, the MPZ model models the same DC parameters that the Boyle model does and additionally input offset voltage and input offset bias current. The MPZ macro lacks a reference to ground which is sometimes convenient in level shift circuits where the Boyle model has several ground references in the circuit. Additionally, the MPZ macro draws output current from the supplies' nodes instead of the ground node. This is useful when power supply requirements are evaluated. The real power of the MPZ macro, however, is in the ac domain. If an op amp has more than two poles and/or additional pole/zero pairs in its transfer function, the Boyle model is unable to do an adequate job simulating the op amp.

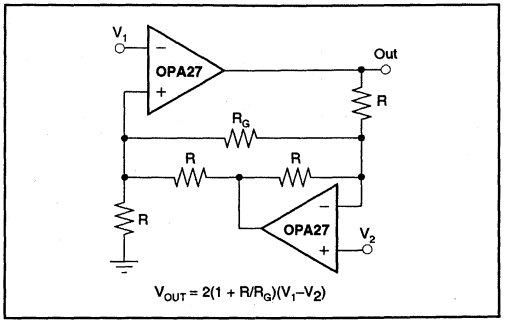


FIGURE 3. An Instrumentation Amplifier Using the Industry Standard OPA27.

To demonstrate this, the application in Figure 3 was chosen. A test to determine the ac accuracy of an op amp macromodel that is frequently recommended is to compare the simulated unity-gain transient response of the op amp to the actual performance of the device at the bench. Although this is a good place to start when performing the macromodel ac performance verification, most macros are optimized to have the correct gain/phase at the zero crossing of the transfer function (see Figures 4 and 5). When the application demands that the op amp macromodel performs with various configurations, the real power of the MPZ macromodel topology is easily demonstrated. The OPA27, a generic amplifier, is used to demonstrate. The simulated results of Figure 3 are shown in Figure 6. In Figure 6, the excessive phase of the two op amp instrumentation amplifier is modelled successfully by the MPZ macro (19.2% overshoot) and unsuccessfully by the Boyle model (9.3% overshoot). The scope photo in Figure 7 verifies the MPZ as being the more accurate macro for this application. On the other hand, the Boyle macro outperforms the MPZ macro in better simulation time and use of computer memory. When simulating one op amp, this is not a critical issue: however, in multiple amplifier applications the MPZ macro becomes CPU hungry. Assuming no convergence problems exist in the macros, the operating-point calculation is largely a function of

the number of circuit elements specified in the net list. With increased op amp complexity, the MPZ macro quickly begins to consume more simulation time. Similarly, the overhead run time of the ac analysis increases with each additional element. The transient analysis is much more difficult to quantify, because of numerous factors that come into play. The primary players are the number of transient iterations and the accuracy of the result needed for each calculation. In many instances, the MPZ macro will require that the programmer change the default values of the two variables in the .OPTIONS statement of Spice by increasing the number of iterations from 10 to 40 (ITL4) and changing the relative tol from 0.001 to 0.01 (RELTOL). If the designer can afford to sacrifice accurate ac performance from the macromodel, the Boyle model is the better choice.

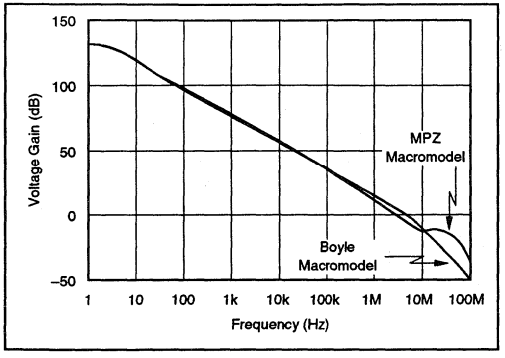


FIGURE 4. Spice Gain Plots of the OPA27 Boyle and MPZ Macromodels.

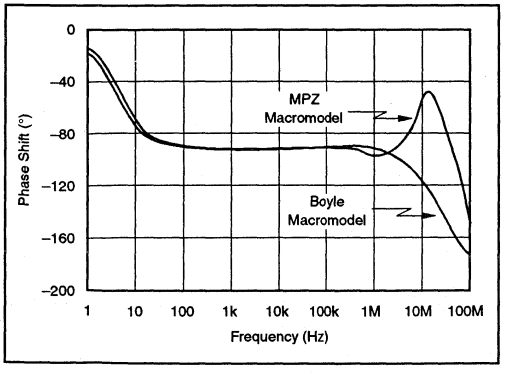


FIGURE 5. Spice Phase Plots of the OPA27 Boyle and MPZ Macromodels.

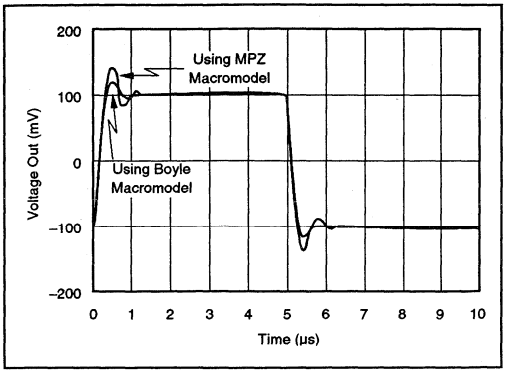


FIGURE 6. Spice Simulation of the Small Signal Transient Response of the Instrumentation Amplifier Shown in Figure 3.

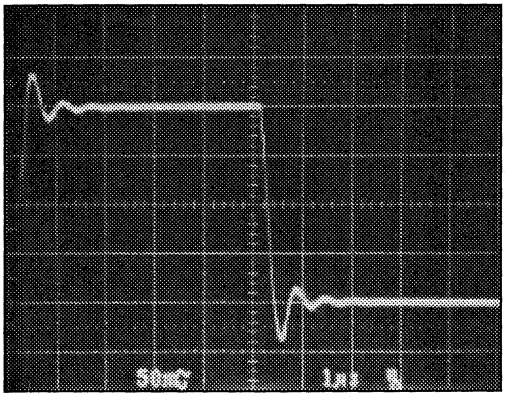


FIGURE 7. Scope Photo of the Small Signal Transient Response of the Instrumentation Amplifier Shown in Figure 3.

REFERENCES

(1) Antognetti, Massobrio, *Semiconductor Device Modeling with Spice*, McGraw-Hill, 1988.

(2) Boyle, Cohn, Pederson, et al, "Macromodeling of Integrated Circuit Operational Amplifiers," *IEEE Journal of Solid State Circuits*, Vol. SC-9, No. 6, December, 1974.

(3) Tabor, Siegel, "Macromodels Aids in Use of Current-Mode Feedback Amps," *Electronic Products*, April, 1992

(4) Alexander, Bowers, "Designer's Guide to Spice-Compatible Op-Amp Macromodels - Part 1," *Electronic Design News*, Volume 35, No. 4, February 15, 1990.

BURR-BROWN®
APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

POWER AMPLIFIER STRESS AND POWER HANDLING LIMITATIONS

By Bruce Trump (602) 746-7347

To achieve reliable power amplifier designs you must consider the stress on the amplifier compared to its power handling limitations. Power handling limits are specified by the Safe Operating Area (SOA) curves of the power amp. Stress on the amplifier depends on amplifier load and signal conditions which can be evaluated with straightforward techniques.

Consider the simplified power op amp shown in Figure 1. Output transistors Q_1 and Q_2 provide positive and negative output current to the load. I_{OUT} is shown flowing out of the amplifier, so Q_1 is supplying the output current. For positive output current, Q_2 is "off" and can be ignored.

The stress on Q_1 under load is related to the output current and the voltage across Q_1 (its collector-to-emitter voltage, V_{CE}). The product of these quantities, $I_{OUT} \bullet V_{CE}$, is the power dissipation of Q_1. This power dissipation is one important consideration, but the "safe operating area" provides a more complete description of the amplifier's limits.

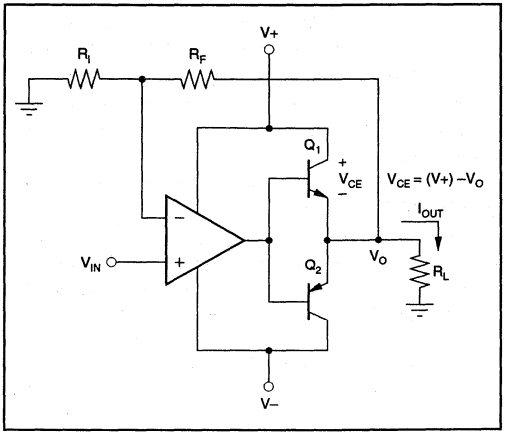


FIGURE 1. Simplified Power Op Amp Circuit.

SAFE OPERATING AREA

The power handling ability of a power transistor is characterized by its Safe Operating Area (SOA), Figure 2. The SOA curve shows permissible voltage, (V_{CE}) and current, (I_{OUT}). The maximum safe current is a function of V_{CE}. The characteristic shape of this curve has four distinct regions.

At low V_{CE}, maximum output current can be safely delivered to the load. Exceeding the maximum current in this region can overstress wire bonds or metallization on the die and destroy the device.

As V_{CE} is increased, the power dissipation of the transistor increases until self-heating raises the junction temperature to its maximum safe value. All points along this thermally limited region (dotted lines) produce the same power dissipation. $V_{CE} \bullet I_O$ is a constant 120W (at 25°C) in Figure 2. All points on this region of the curve produce the same maximum junction temperature. Exceeding the safe output current in this region may damage the transistor junction.

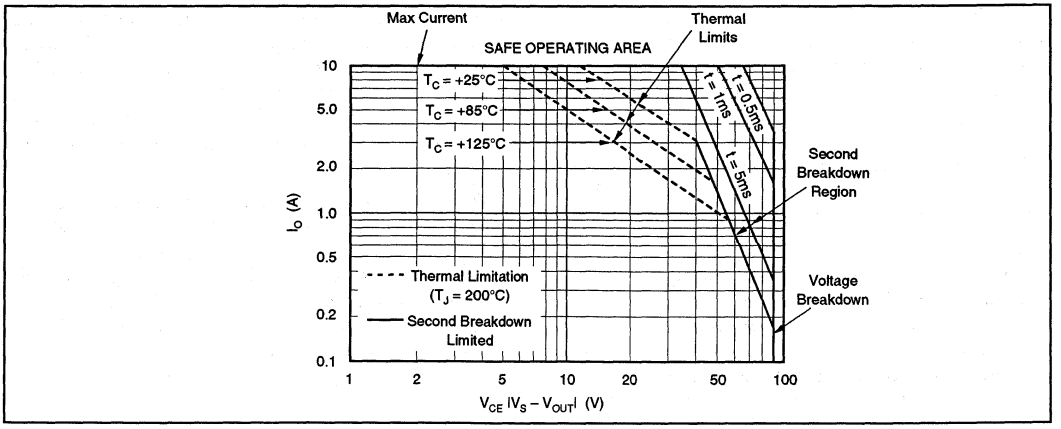


FIGURE 2. Safe Operating Area (SOA)— OPA502. (Figure 2 in PDS-1166)

As V_{CE} is further increased, beyond the thermally limited region, the safe output current decreases more rapidly. This so-called *second breakdown* region is a characteristic of bipolar output transistors. It is caused by the tendency of bipolar transistors to produce "hot spots"—points on the transistor where current flow concentrates at high V_{CE}. Exceeding the safe output current in the second breakdown region can produce a localized thermal runaway, destroying the transistor.

The final limit is the breakdown voltage of the transistor. This maximum power supply voltage cannot be exceeded.

Often, an SOA curve provides information showing how the safe output current varies with case temperature. This accounts for the affect of case temperature on junction temperature. Additional lines may show the maximum safe current for pulses of various durations according to the thermal time constants of a device.

The SOA curve should be interpreted as an absolute maximum rating. Operation at any point on the thermal limit portion of the curve produces the maximum allowable junction temperature—a condition not advised for long-term operation. Although operation on the second-breakdown portion of the curve produces lower temperature, this line is still an absolute maximum. Operation below this limit will provide better reliability (i.e.—better MTTF).

HEAT SINKING

In addition to assuring that an application does not exceed the safe operating area of the power amplifier, you must also assure that the amplifier does not overheat. To provide an adequate heat sink, you must determine the maximum power dissipation. The following discussions detail methods and considerations that affect SOA requirements and power dissipation and heat sink requirements.

SHORT-CIRCUITS

Some amplifier applications must be designed to survive a short-circuit to ground. This forces the full power supply voltage (either V+ or V–) across the conducting output transistor. The amplifier will immediately go into current limit. To survive this condition a power op amp with adjustable current limit must be set to limit at a safe level.

Example 1

What is the maximum current limit value which would protect against short-circuit to ground when OPA502 (Figure 2) power supplies are ±40V?

Answer—

If the case temperature could be held to 25°C, the current limit could be set to 3A, maximum. This would be unlikely, however, since the amplifier would dissipate 120W during short-circuit. It would require an "infinite" or ideal heat sink to maintain the case temperature at 25°C in normal room ambient conditions.

If the case temperature were held to 85°C, a 2A current limit would be safe. Power dissipation would be 80W, requiring a heat sink of 0.75°C/W—a large heat sink. (See Application Bulletin AB-038 for heat sink calculations.)

If the op amp must survive a short-circuit to one of the power supplies, for instance, the maximum V_{CE} would be the total of both supplies—a very demanding case.

Not all applications must (or can be) designed for short-circuit protection. It is a severe condition for a power amplifier. Additional measures such as fuses or circuitry to sense a fault condition can limit the time the amplifier must endure a short-circuit. This can greatly reduce the heat sink requirement.

An additional feature of the OPA502 and OPA512 power amplifiers, the optional fold-over circuit, can be connected on the current limit circuit. This can be set to reduce the current limit value when V_{CE} is large—exactly the condition that exists with a short-circuit. While useful in some applications, the foldover limiter can produce unusual behavior—especially with reactive loads. See the OPA502 data sheet for details.

RESISTIVE LOADS—DC OPERATION

Consider a power amplifier driving a resistive load. It is tempting to check for safe operation only at maximum output voltage and current. But this condition is not usually the most stressful.

At maximum output voltage, the voltage across the conducting transistor, V_{CE}, is at a minimum and the power dissipation is low. In fact, if the amplifier output could swing all the way to the power supply rail, the current output would be high, but the amplifier power dissipation would be zero because V_{CE} would be zero.

Figure 3 plots power from the power supply, load power, and amplifier power dissipation as a function of output voltage delivered to a resistive load. The power delivered to the load increases with the square of the output voltage ($P = I^2R$), while the power from the power supply increases linearly. The amplifier dissipation (equal to the difference of the first two curves) follows a parabola. If the amplifier output could swing all the way to the power supply rail (dotted portion of lines), all the power from the supply would be delivered to the load and the amplifier dissipation would be zero.

Peak amplifier dissipation occurs at an output voltage of (V+)/2, or 50% output. At this point, V_{CE} is (V+)/2 and I_O is $(V+)/(2R_L)$. The amplifier dissipation at this worst-case point is the product of V_{CE} and I_O, or $(V+)^2/(4R_L)$. Check this condition to assure that it is within the SOA of the amplifier. Also be sure that you have sufficient heat sinking for the calculated power dissipation to prevent overheating.

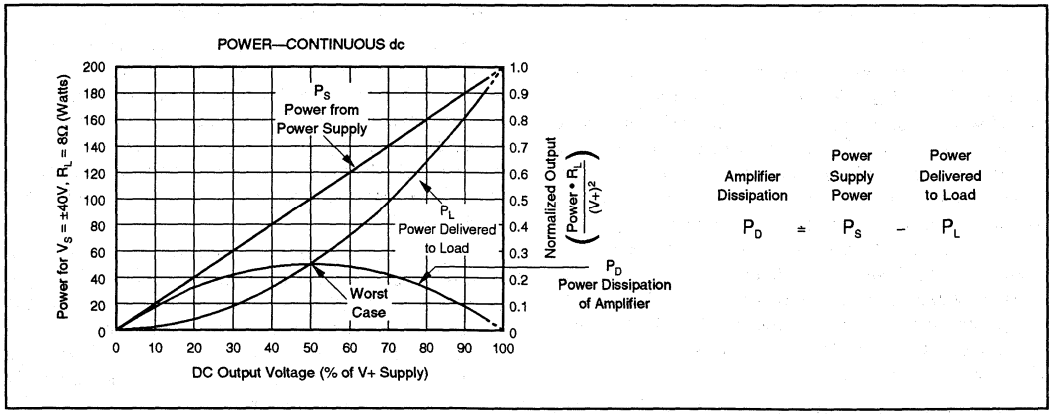


FIGURE 3. DC Power Dissipation, Resistive Load.

Example 2

An unbalanced power supply is often used with power amplifiers to allow a large unipolar output voltage. A +70V/–5V power supply is used with the OPA502 to drive a 30Ω load connected to ground. What is the worst case power dissipation and SOA requirement?

Answer—

The worst case occurs at half output, where V_O = 35V, and V_{CE} = 35V. The output current at this point would be 35V/30Ω = 1.17A which is within the SOA. Power dissipation would be 35V • 1.17A = 41W.

Other points to consider: The maximum output voltage would be approximately 65V, and 65V/30Ω = 2.17A. At this point, V_{CE} = 5V, a safe value on the SOA.

If the current limit were set to accommodate the full output of 2.17A, it would not be safe for short-circuits to ground. With a short-circuit to ground, V_{CE} = 70V where the maximum safe current is 0.4A.

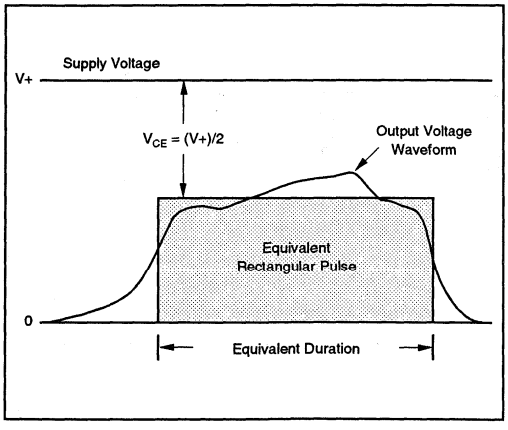


FIGURE 4. Pulsed Loads.

PULSED OPERATION

Some applications must handle pulses of current or varying current waveforms with a low duty-cycle. The SOA plot sometimes shows an ability to supply larger currents for short duration pulses. In Figure 2, the SOA limits are labeled for 5ms, 1ms and 0.5ms pulses. The duty-cycle must be low (approximately 5% or less), so that heating in the output transistor is given time to dissipate.

Unusual current waveforms can be estimated with an approximation to a rectangular pulse as shown in Figure 4. With a resistive load, the most stressful condition is when the output voltage is approximately half the supply voltage as shown. For other types of loads, evaluate any condition that produces significant load current and high V_{CE}. Applications which pulse currents beyond the dc SOA of the amplifier should be evaluated very carefully since they are pushing the limits of the device. Good reliability is achieved by taking a conservative approach to SOA limits.

AC SIGNALS

Imagine a time-varying signal that rapidly transverses the curves in Figure 3. The point of maximum dissipation is passed only briefly. If the signal changes rapidly enough (above 50Hz), the thermal time constant of the device causes the junction temperature to be determined by the *average* power dissipation. So, ac applications are generally less demanding than dc applications of the same peak voltage and current requirements.

If the signal is bipolar, such as a sine wave centered around zero, each output transistor "rests" for a half-cycle. The total amplifier dissipation is shared between the two output transistors, lowering the effective thermal resistance of the package.

If the instantaneous peak dissipation point is within the SOA of the amplifier, the primary concern is providing a sufficient heat sink to prevent overheating. Since this peak

condition is passed only briefly during an ac cycle, ac applications operate reliably, closer to the SOA limit.

Figure 5 shows the power curves for a power amplifier with ±40V supplies and an 8Ω resistive load. Again, powers are plotted with respect to the percentage of maximum voltage output. As with dc, the power delivered from the power supply increases linearly with output voltage and the power delivered to the load increases with the square of the output voltage. The power dissipated by the amplifier, P_D, is the difference of the first two curves. The shape of the P_D curve is similar to the dc signal case, but does not approach zero at 100% output voltage. This is because at full ac output voltage, the output is rapidly transversing the whole curve (0 to 100%) of Figure 4. Figure 5 shows the average dissipation of this dynamic condition.

Amplifier dissipation reaches a maximum when the peaks of the ac output waveform are approximately 63% of the power supply voltage. For this sine wave amplitude, the instantaneous output voltage hovers near the crucial half-supply-voltage value for a large portion of the ac cycle.

The normalized values read from the right side of the curve in Figure 5 can be scaled to any supply voltage and load resistance. To find your amplifier dissipation at a given signal level, multiply the reading taken from the right-side scale by $(V+)^2/R_L$.

AC applications rarely must endure continuous operation at the maximum dissipation point of Figure 5. An audio amplifier, for instance, with voice or music typically dissipates much less than this worst-case value, regardless of the signal amplitude. Yet, since a continuous sine wave signal of any amplitude is conceivable, this worst-case condition is a useful benchmark. Depending on the application, you might want to design for this condition.

REACTIVE LOADS—AC SIGNALS

Figure 6 shows the relationship of voltage and current in purely inductive load. The current lags the load voltage by 90°. At peak current, the load voltage is zero. This means that the amplifier must deliver peak current with the full V+ across the conducting transistor (V– for negative half-cycle peak current). The situation is equally severe for a capacitive load. Check for this condition of voltage and current on the SOA curve.

Once again, consider the curve in Figure 5. Power amplifier dissipation is equal to the power from the power supply minus the power delivered to the load. The power from the power supply, P_S, is the same whether the load impedance is resistive or reactive. But if the load is completely reactive (inductive or capacitive), the power delivered to the load is zero. So the power dissipated by the amplifier is equal to the power from the power supply. At full output this is approximately three times the worst-case amplifier dissipation with a resistive load!

A reactive load is a very demanding case, requiring a large heat sink compared to a resistive load. Fortunately, purely reactive loads are rare. An ac motor, for instance, could not be purely inductive, or it would be incapable of performing any mechanical work.

FINDING POWER DISSIPATION

Unusual loads and signals can be challenging to evaluate. Use the principle that amplifier power dissipation is equal to the power from the supplies minus the load power.

Power delivered from the power supplies can be measured as shown in Figure 7. The power from each supply is equal to the average current times its voltage. If the output waveform is asymmetrical, measure and calculate the positive

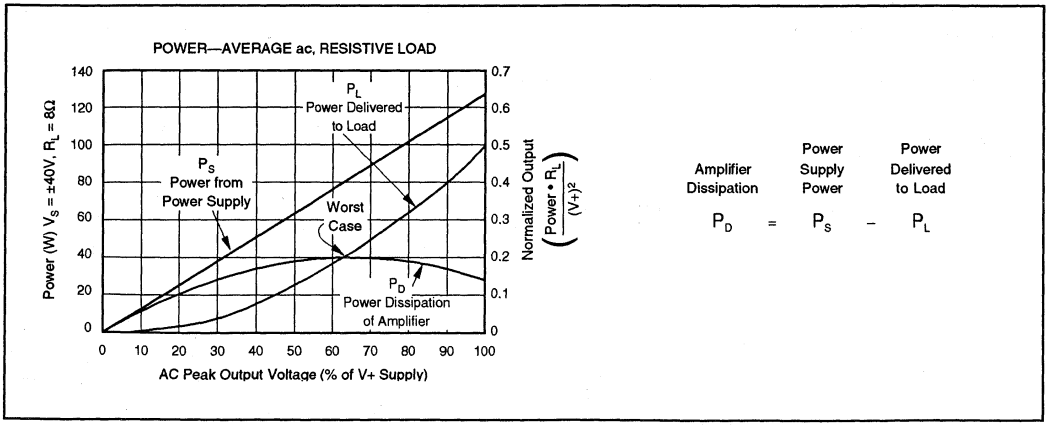


FIGURE 5. AC Power Dissipation, Resistive Load.

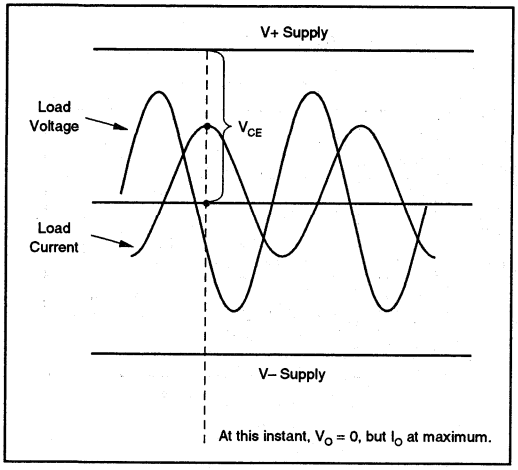


FIGURE 6. Voltage and Current Waveforms for Inductive Load.

and negative supplies separately and add the powers. If the waveform is symmetrical, you can measure one and multiply by two. Use an average-responding meter to measure the current. A simple D'Arsonval type meter movement with a current shunt works well. Do not use an rms-responding meter.

For sinusoids, finding the load power is easy—

$$P_{LOAD} = (I_O \text{ rms}) \bullet (V_O \text{ rms}) \bullet \cos(\theta)$$

Where θ is the phase angle between load voltage and current. (See Figure 8 for measurement methods.)

For complex waveforms, the load power is more difficult to measure. You may know something about your load which allows you to determine load power. If not, you can build a circuit that measures load power using a multiplier IC to continuously multiply load voltage and current. The average dc output of the multiplier is proportional to the average load power. See the MPY100 data sheet for a circuit to measure power with a multiplier.

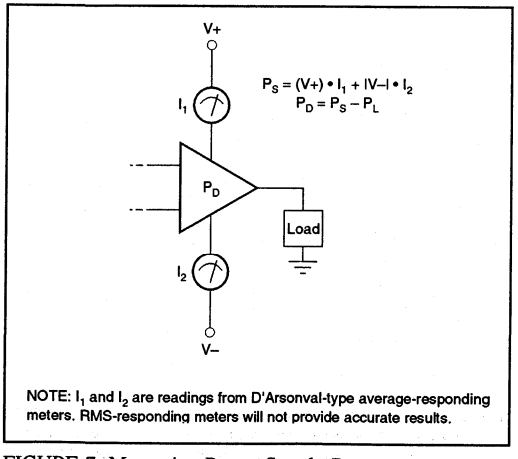


FIGURE 7. Measuring Power Supply Power.

UNUSUAL LOADS

Usually an op amp sources current to the load (Q_1 conducting, Figure 1), when the output voltage is positive. But depending on the type of load and the voltage to which it is referenced, an op amp might have to sink current (Q_2 conducting) with positive output voltage. Or, it could be required to source current with negative output voltage. In these cases, the voltage across the conducting transistor is larger than V+ or V–.

An example of this situation is a power op amp connected as a current source. The output of a current source might be connected to any voltage potential within its compliance range. Sourcing high current to a negative potential node would produce high dissipation and require good SOA.

MOTOR LOADS

Motor loads can be tricky to evaluate. They are like a reactive load since stored energy (mechanical) can be delivered back to the amplifier. Motor and load inertia can cause the amplifier to dissipate very high power when speed is changed.

Electro-mechanical systems can be modeled with electric circuits. This is a science in itself—beyond the scope of this discussion.

You can, however, measure the V-I demand of a motor (or any other load) under actual load conditions. Figure 8 shows a current sense resistor placed in series with the load. With load voltage and current displayed on separate oscilloscope traces, you can find the conditions of maximum stress. Be sure to consider the voltage across the conducting transistor, (V_{CE}), not the amplifier output voltage. The most stressful conditions may occur with moderate current, but low load voltage.

An X-Y type display of voltage and current (Figure 8B) may also help identify troublesome conditions. More demanding combinations of voltage and current are those that deviate from a straight-line resistive load.

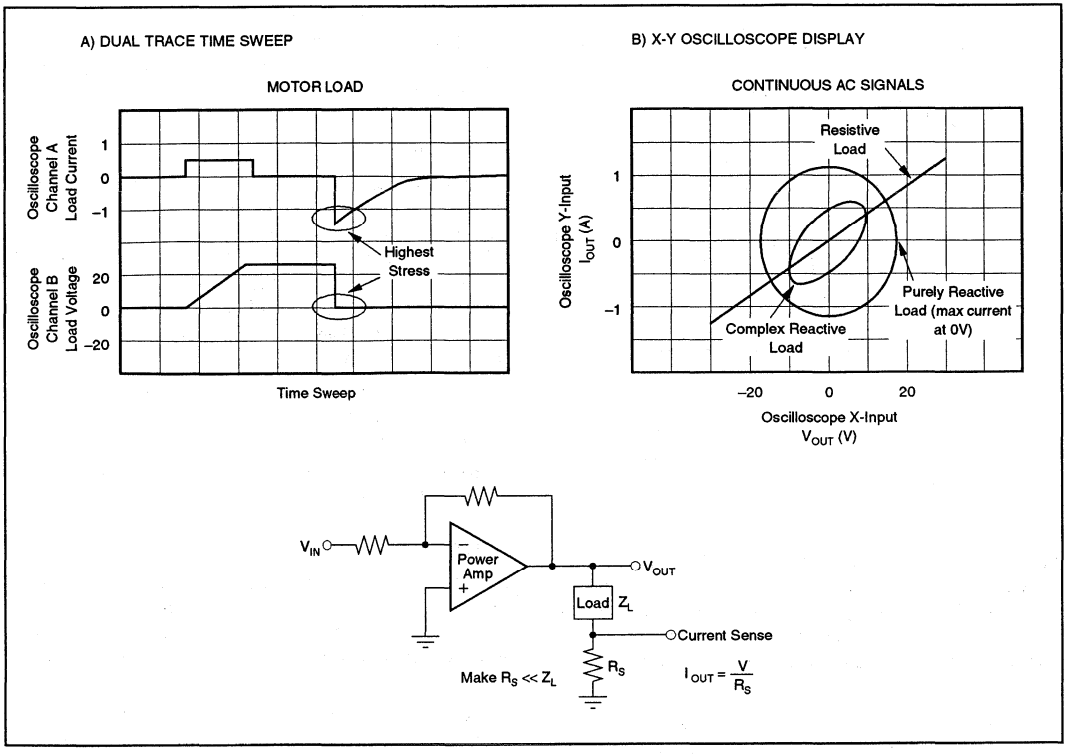


FIGURE 8. Voltage/Current Waveforms, Unusual Loads.

BURR-BROWN® APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

MOUNTING CONSIDERATIONS FOR TO-3 PACKAGES

By Hubert Biagi (602) 746-7422

Proper mounting of TO-3 packages is required to assure rated performance and reliability. Although the procedures are simple, ignoring them can result in poor performance and catastrophic failure of the device.

PACKAGE HANDLING

The TO-3 package is a rugged hermetic package, but it can be damaged with improper handling. Excessive bending or twisting of the package pins can crack the glass seal around the pin and result in loss of hermeticity. If pin straightening is required, clamp the pin against the package base using needle-nose pliers. This will strain-relieve the pin during the straightening operation.

Another potential problem is cracking the internal circuit substrate from bending of the package base. This can be caused by mounting the package onto a non-flat surface, improper use of a compressible thermal pad, or over-tightening the mounting fasteners.

TO-3 SOCKET

The Burr-Brown 0804MC TO-3 socket is designed to meet the requirements of high current, high power products such as the OPA512, OPA541, and OPA2541. The socket has a rugged contact design which assures positive and reliable contact even when using thermal grease and pre-tinned pins. The closed-ended contacts will accept the full pin length of the TO-3 and guard against solder and flux contamination. The socket body has a center hole which allows for direct measurement of TO-3 case temperature.

FASTENERS

The fastener hardware used to mount the TO-3 package is very important. Table I describes the proper hardware combination. Sources for fastener hardware are listed at the end of this bulletin. The preferred fastener material is stainless steel. Plated steel is a good alternative. Brass or plastic fasteners are not recommended.

The mounting holes of the TO-3 package are designed to accept 6-32 machine screws; no other size should be used (see exploded views in Figure 1A and 1B). The pan-head is the best head style. It has a low profile and large bearing face to properly cover the mounting hole, but its not so large as to ride up onto the lip of the welded cover.

In order to maintain proper mounting pressure, the Belleville spring washer (also known as a conical compression washer), is recommended. Split ring and star lock washers are not recommended. They typically bottom out at less than 50 pounds, whereas 150-300 pounds of pressure is needed to

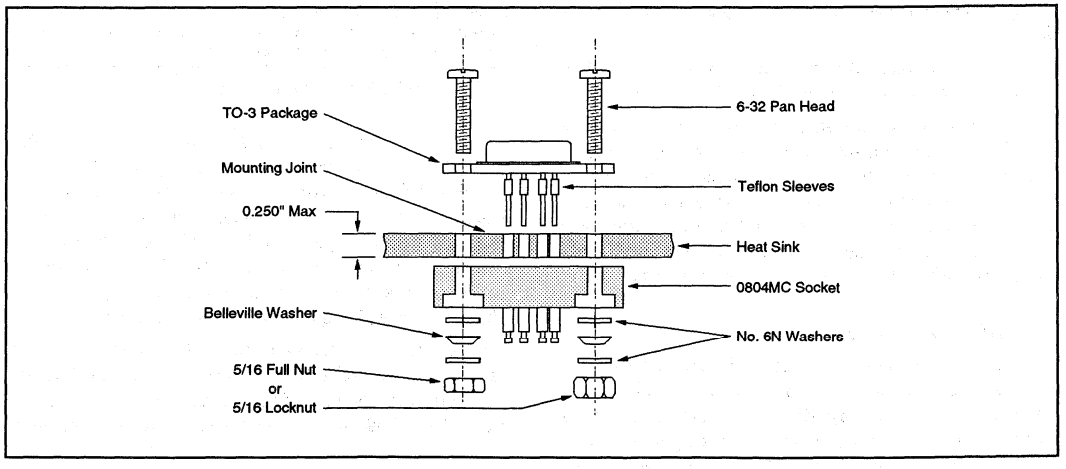


FIGURE 1A. High Power Application Using 0804MC Socket.

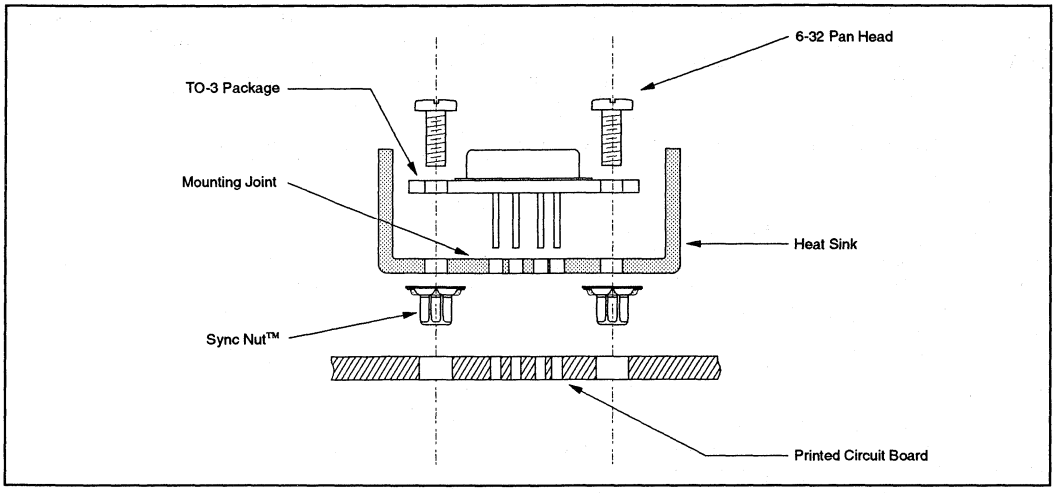


FIGURE 1B. Low Power Application Using Printed Circuit Board.

achieve low thermal resistance[1]. The Belleville washer does not bottom out and therefore can absorb the thermal expansion of the package[2] or any slight compression of the socket material that may occur over time. An excellent variation of the conical washer is called the Sync Nut™ and is available from EG&G Wakefield. It includes a spring washer as part of the nut.

The Belleville washer should be installed on the board or heat sink side of the fastener, *not* on top of the package flange. Install the large face of the Belleville washer toward the mounting surface. When tightening against a board or 0804MC socket, install an additional No.6N (narrow) flat washer against the relatively soft material to insure that the Belleville washer functions correctly. Tighten the fasteners slowly, and alternate between them until both are tighten to the specification.

The recommended tightening torque is 6 inch-lbs., with an acceptable range of 4 - 7 inch-lbs. (0.45 - 0.79 N-m).

Avoid contaminating the fastener threads with thermal grease since it can change the torque readings. Over-tightening the fasteners can damage the package or internal substrate, under-tightening can lead to poor thermal performance. Re-torquing may be required after environmental screening operations such as burn-in. For permanent installation, an all-metal locknut is preferred. Don't use locknuts with plastic inserts.

TO-3 HOLE PATTERN

A good mounting joint between the TO-3 package and the heat sink requires a properly machined mounting hole pattern. Never drill out a single (large diameter) clearance hole for the package pins. Drill individual holes for each pin. Follow the TO-3 hole pattern illustrated in Figure 2. For best thermal performance, use a minimum hole size of 0.073 inch (#49 drill). Smaller holes could interfere with the glass seal around each pin.

	BEST	ACCEPTABLE	NOT RECOMMENDED
Material	Stainless Steel	Plated Steel	Brass, Plastic
Fastener Head	Pan	Round, Hex	Binding, Flat, Oval, Truss, Fillister, Socket, Hex Washer
Washers	No.6 Belleville[1] + No.6N Flat	No.6N Flat	
Nut	5/16" Full, Sync Nut™	1/4" Hex Threaded, 1/4" Full	
Locking Device	5/16" Locknut[2]	Split Ring[3]	Star Washer

NOTES: (1) Recommended No.6 Belleville washer is available from ASMCO (part number 24087; diameter 0.312"; rated 78lbs initial force). (2) For high power use all metal type, elastic inserts not recommended. (3) Not recommended for high power or temp cycling conditions.

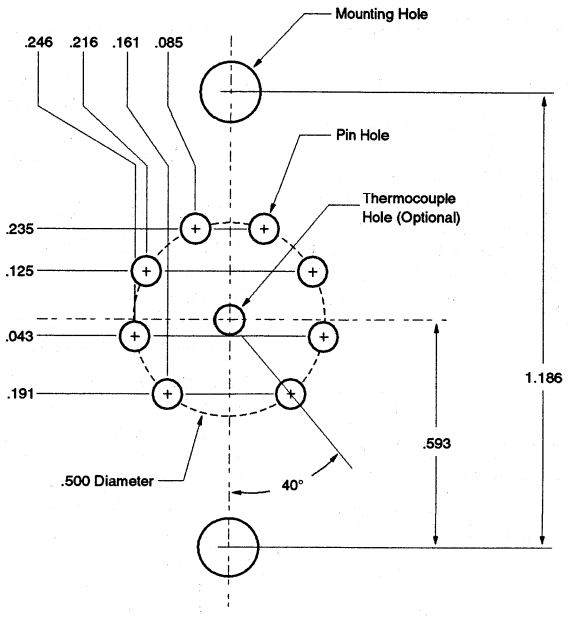
TABLE I. 6-32 Fastener Hardware.

To avoid shorting the pins to the heat sink, use #18 Teflon tubing to sleeve all pins. Make sure the sleeve length is slightly less than the thickness of the heat sink. Most pre-drilled heat sinks use larger 3/32 (0.094") holes for the pins, and sleeving is not required so long as a socket or PC board pattern is used. You may still want to sleeve at least two opposite pins to help center the package. When wiring directly to the pins, all pins should be sleeved, regardless of the hole size used.

A word of caution concerning anodized heat sinks. Unless you know what type of anodizing was used, do not trust the anodizing to provide electrical insulation. Refer to the section called "Heat Sink Surface Treatment" for more information.

MOUNTING SURFACE PREPARATIONS

In general, the heat sink mounting area should have a flatness and finish comparable to that of the TO-3 package. When



HOLE TYPE	NUMBER REQUIRED	HOLE SIZE MIN / MAX		RECOMMENDED DRILL SIZE
Mounting	2	.147"	.157"	24
Pin	8	.073	.094	46
Thermocouple	Optional	.067	.070	51

FIGURE 2. TO-3 Hole Pattern.

using thinner, low power heat sinks, it is sufficient that the mounting area appears flat against a straight edge. When mounting on thicker material, surface flatness is important not only for thermal performance, but to avoid distorting and stressing the package base when it is tightened down.

HEAT SINK SURFACE FLATNESS AND FINISH

JEDEC recommends a surface flatness of 0.004 inch/inch max. The standard flatness tolerance for most extruded heat sinks is 0.004 inch/inch, maximum, which results in typical values closer to 0.002 inch/inch. Surface finish is normally specified around 60 micro-inches (rms). Testing has shown that this is acceptable for most high power applications[3]. It is a good practice to polish the mounting area with No. 000 steel wool, followed by an acetone or alcohol rinse, immediately prior to assembly.

For best thermal performance, the mounting area of the heat sink can be spot faced. This removes oxidation or anodization and improves the surface flatness and finish. When using thermal pads instead of thermal grease, a surface flatness of 0.001 inch/inch is recommended. When mounting the TO-3 package to panels, brackets, or other structural members of the system, spot facing may be required to insure the proper flatness and finish.

HEAT SINK SURFACE TREATMENT

The typical surface treatment for aluminum heat sinks is black anodized[4] per MIL-A-8625, Type II. This surface treatment prevents corrosion and maximizes thermal performance. Do not trust this surface treatment to provide electrical insulation. For electrical insulation, always specify hard anodized, 0.001 inch thick, per MIL-A-8625, Type III. This *file hard* surface treatment resists scratches and punctures, and is typically rated for 200VDC electrical insulation for a 0.001 inch thick treatment.

HEAT SINK THRU-HOLES

Be wary of heat sinks with punched, rather than drilled, thru-holes. If not properly done, the area around each punched hole can be depressed into a crater with a raised lip or mound on the opposite side. This irregular surface can significantly degrade thermal performance.

For high power, extruded heat sinks, the general practice is to drill the hole pattern. All holes should be de-burred. The holes for the TO-3 pins should not be chamfered too deeply, as this will reduce the contact area of the mounting joint. Unless special precautions are taken, threading the TO-3 mounting holes is not recommended. The threading process can also leave a raised mound around each hole. Threading the mount-

ing holes also eliminates the possibility of using Belleville washers and locknuts for proper control of mounting pressure.

MOUNTING THERMAL RESISTANCE

Even if all of the proper mounting preparations are followed, the thermal resistance at the mounting joint will consist largely of small air gaps. Only a small percentage of the mounting area will actually have metal-to-metal contact. To minimize the thermal resistance, these gaps must be filled with a stable, thermally conductive material. Table II describes the common thermal fillers available and the performance that can be expected. Note that the tightening torque of the mounting fasteners also affects thermal performance[5].

DESCRIPTION	θ_{CH} (°C/W)	APPLICATION	HEAT SINK FLATNESS REQUIREMENTS
Bare Joint	0.5 - 1.0	Low power only	Very sensitive to variations in flatness and finish
Thermal Grease	0.1 - 0.2	High Power	Not sensitive, standard .004 inch/inch (max) ok
Aluminum Foil[1] (pre-coated with alumina filled silicone)	0.2 - 0.4	High Power	For lowest θ_{CH}, .001inch/inch (typ) recommended
Aluminum Foil[2] (pre-coated with thermal grease)	0.2 - 0.4	High Power	For lowest θ_{CH}, .001inch/inch (typ) recommended
Kapton[3] (pre-coated with thermal grease)	0.3 - 0.5	Electrical Insulation	For lowest θ_{CH}, .001inch/inch (typ) recommended
Silicon Rubber (compressible)	0.4 - 1.0	Electrical Insulation	See Text
Mica (bare)	1.0 - 1.5	Electrical Insulation	Not recommended Mica is brittle and prone to crack
Mica (with thermal grease)	0.3 - 0.4		
NOTE: (1) Available from BERGQUIST, part number QII-88 (with .094 inch holes). (2) Available from Power Devices, part number AL-155-10C. (3) Available from Crayotherm, part number TO-3-8 CR2-MT. See Appendix for manufacturers listings.			

TABLE II. Thermal Interface Options For TO-3 Packages.

Understanding the thermal model of the system will enable you to make the best mounting compromises. Consider the simplified thermal model in Figure 3. The mounting thermal resistance is represented as θ_{CH} (case-to-heat sink). The overall thermal resistance is represented by θ_{JA} (junction-to-ambient). For low power applications, θ_{JA} can be as high 30°C/W. In this case, the mounting thermal resistance is not a significant portion of the overall thermal resistance. For high power applications, θ_{JA} can be as low as 1°C/W. Then it is critical to obtain a low θ_{CH}. For example, at a power dissipation of 50W, an additional 0.5°C/W mounting thermal resistance will increase the junction temperature by 25°C.

BARE MOUNTING

For no-load or low power applications, you can mount the TO-3 package bare against the heat sink. For high power applications, this is not recommended, even if the extra thermal resistance is acceptable. This is because the thermal resistance of a bare joint can vary greatly depending on the surface flatness and finish of the heat sink.

THERMAL GREASE

For the lowest θ_{CH}, thermal grease should be used in conjunction with a properly machined and finished mounting surface. This combination will result in a θ_{CH} of about 0.1°C/W. Using the proper fastener hardware is critical for maintaining this low thermal resistance over time and temperature.

There are many suppliers of thermal grease (also known as heat sink compound). Thermal grease is a formulation of fine zinc oxide or other thermally conductive, electrically insulating, particles in a silicone oil or other synthetic based fluid. The shelf life for most thermal greases is indefinite when kept sealed in its container, but over time, the oil may separate out. Mixing the components back together before use will restore the thermal properties.

Thermal grease should not be applied in excess, the objective is to fill the air gaps, not decrease the amount of metal-to-metal contact. Slight rotation of the TO-3 package against the heat sink will promote even spreading. With the correct amount applied and the fasteners properly torqued, a very small bead of thermal grease should appear around the perimeter of the TO-3 package. Although the grease may dry up over time, this does not degrade the thermal resistance provided the mounting joint remains tight.

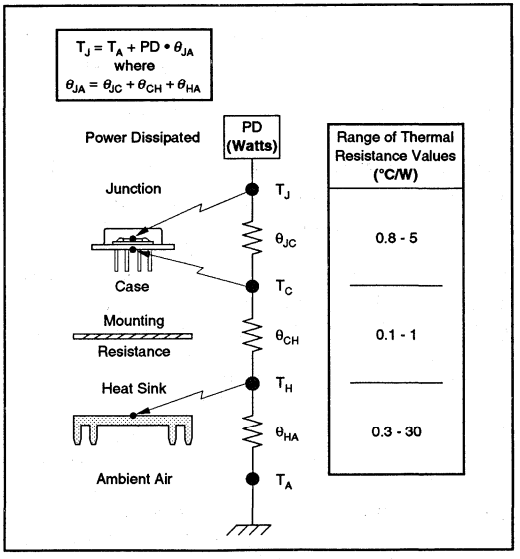


FIGURE 3. Simplified Thermal Model.

THERMAL PADS

Thermally conductive pads offer a cleaner, simpler method for improving the thermal interface. The lowest θ_{CH} attainable using a thermal pad is about 0.2°C/W, which is almost as good as thermal grease. However, one should approach with caution the multitude of different materials, designs, and applications for thermal pads.

Basically there are two types of thermal pads, electrically insulating and electrically conductive. Electrically insulating pads are designed to be used with discrete transistor TO-3s, which do not have an electrically isolated package. In general, they do not provide a low enough θ_{CH} for high power use because a dielectric layer must be sandwiched into the pad. Hybrid TO-3s with isolated headers do not require electrically isolated pads. They can use electrically conductive pads. Without the need for a dielectric layer, a very low θ_{CH} can be achieved, almost as good as thermal grease.

While they do a good job of filling small air gaps, all thermal pads suffer the same problem when used against heat sinks with standard flatness tolerances of 0.004 inch/inch. They do not flow to conform with the surfaces as does thermal grease. Therefore, it is recommended that whenever thermal pads are to be used, the mounting area should be spot faced to a typical surface flatness of 0.001 inch/inch. Silicon rubber pads are also sensitive to surface flatness[6]. Approach these with caution. Most do not improve thermal performance over a bare joint. The compressibility of these rubber pads can cause the package header to flex and possibly crack the internal substrate. They can also settle over time and temperature, resulting in loose fasteners and low mounting pressure.

SUGGESTED MOUNTING SCHEMES

The mounting schemes presented here address the more common operating conditions for TO-3 power products (see Figure 4). These conditions include high power operation, low power operation, and functional testing under unloaded, quiescent conditions. The options are for the 0804MC socket, individual cage jacks, and direct PC board soldering. Table III describes the recommended cage jacks.

MANUFACTURER	PART NUMBER	DRILL SIZE INCHES (NUM)	COMMENTS
Cambion	450-3716-01-03	.076 48	Knock-out bottom permits wave soldering.
Concord	09-9047-1-03	.104 37	Heavy duty, open ended.
SPC Technology	MC76	.089 43	PC board press fit.
Mil-Max	0325-0-15-01-34-27-10-0	.089 43	Closed end, accepts full pin length.
(See Appendix for manufacturers listings)			

TABLE III. Recommended Cage Jacks.

FUNCTIONAL TESTING AND NO-LOAD CHARACTERIZATION

For functional testing and no-load characterization at room temperature, heat sinking may not be required. These mounting schemes are the least critical and easiest to fabricate. When using the 0804MC socket, the socket can be mounted directly to the test box or PC board by drilling a single clearance hole for all eight socket contacts. The hole should be (0.63 - 0.75) inches in diameter. Be careful not to short the copper cladding or metal box to any of the contacts. The socket body should be mounted using flat head machine screws. For electrical insulation, nylon flat head machine screws may be used instead. When using cage jacks, follow the TO-3 hole pattern illustrated in Figure 2. Use close ended cage jacks whenever possible to avoid solder contamination.

LOW POWER OPERATION

The mounting schemes for low power applications are an extension of those used for functional testing and no-load characterization. The difference is that a small heat sink is must be attached to the TO-3 package. The overall thermal resistance (θ_{JA}) for low power applications can be relatively high, from 5 - 30°C/W. Therefore, θ_{CH} is not as critical as for high power operation. In most instances, the TO-3 package can be mounted bare.

Low power heat sinks are usually stamped rather than extruded, and some even press fit around the TO-3 cover. They are called "low power" or "standard" heat sinks (versus "high power" or "extruded" heat sinks used for high power operation). The thermal resistance of these types of heat sink range from 3 - 20°C/W, depending on their size, weight, and design.

Low power mounting schemes are commonly used on PC board applications. For these applications, heat sink manufacturers have developed many custom accessories such as wave solderable fasteners and thermally conductive pads. These must be approached with caution. It is important to follow the specific recommendations of this bulletin. Thermal pads are discussed in the section called "Thermal Mounting Resistance".

The recommended fastener for PC board applications is the Sync Nut™. This fastener allows the TO-3/heat sink combination to be wave soldered directly to the board. Re-torquing should be performed after any wave solder. For low power applications that do not involve temperature cycling, split ring lock washers may be safely used.

HIGH POWER OPERATION

Mounting schemes for high power operation involve the use of larger, heavier heat sinks, that are machined rather than stamped. Their size and weight usually requires that they be integrated into the system layout, rather than simply attached to the TO-3 package. In general, they are cut to length from extruded sections, thus are often called "extruded" heat sinks.

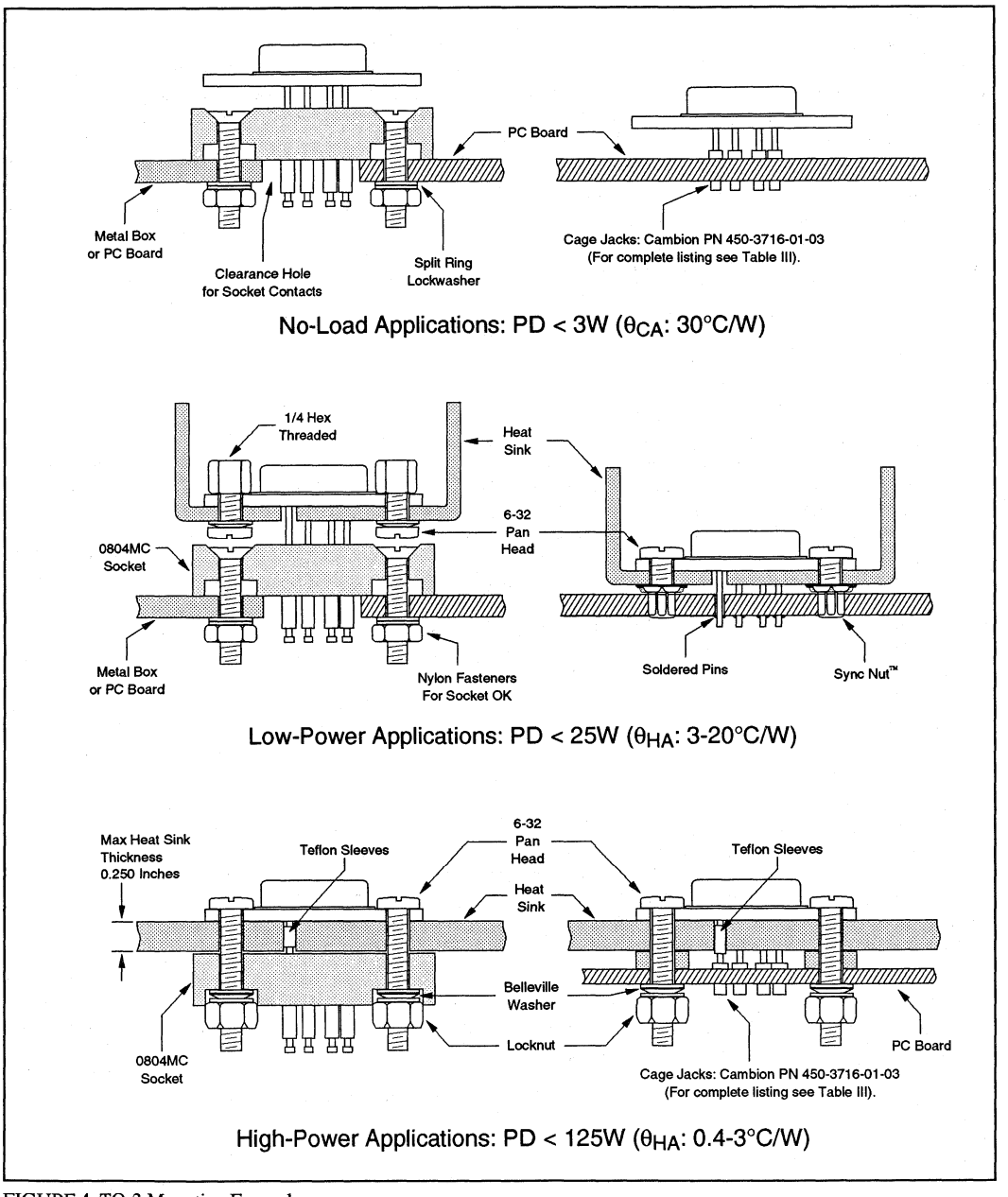


FIGURE 4. TO-3 Mounting Examples.

The thermal resistance of these types of heat sink range from 0.4 - 3°C/W for operation in still air. With forced air, θ_{HA} can be reduced by one-half to two-thirds.

For high power applications, the overall thermal resistance (θ_{JA}) can be as low as 1°C/W. Under these conditions, obtaining a low θ_{CH} is critical. To insure a good mounting joint, use the recommended fastener hardware and surface preparations as described in the previous sections of this application bulletin.

THERMAL MEASUREMENT AND EVALUATION

It is always a good idea to check the TO-3 mounting scheme by measuring the package case temperature (T_C) under actual operating conditions. The semiconductor junction temperature (T_J) can then be calculated from the case temperature, as indicated in Figure 3 :

$$T_J = T_C + PD \bullet \theta_{JC}$$

where PD is the total power dissipation (including quiescent power) and θ_{JC} is the junction-to-case thermal resistance (given in the product data sheet). The calculated junction temperature should be less than the maximum allowable temperature indicated by the product data sheet (typically 150°C).

The true case temperature is located directly below the substrate and centered within the package pins (see Figure 5). This location, called the case backside, will also give the most repeatable measurements. To directly access the case backside, drill the heat sink with the optional thermocouple hole(7) as illustrated in Figure 2. The recommended thermocouple is an Omega fast-response probe (part no. SDX-SET-RT-K-SMP). Allow enough time for the system to reached thermal equilibrium. A touch of thermal grease on the probe tip will ensure good thermal contact.

The package case temperature can also be estimated by fitting a spade-lug type thermocouple under the head of the mounting fastener. This will give the temperature at the mounting flange of the package rather than the case backside. The case backside will actually be hotter than the mounting flange. The difference can be as large as 10°C, depending on the power dissipation, mounting thermal resistance, etc. For high power applications, it is recommended that the case backside temperature be measured directly, at least for the prototype setup.

References:

(1) Thermalloy catalog #90-HS-11 (page 13), Figures 6 and 8.

(2) EG&G Wakefield catalog, printed 4/90 (page 103), "115, 116, 117, & 118 Series SyncNut".

(3) Thermalloy catalog #90-HS-11 (page 12), "Test Results".

(4) Thermalloy catalog #90-HS-11 (page 9), "Available Finishes".

(5) Thermalloy catalog #90-HS-11 (page 13), Figures 6 and 8.

(6) Thermalloy catalog #90-HS-11 (page 106), "Test Method Comparison — TO-3 Silicon Rubber Insulators".

(7) The optional thermocouple hole will not increase the mounting thermal resistance significantly. The difference cannot be measured experimentally. Computer simulations indicate an increase of less than 0.02°C/W.

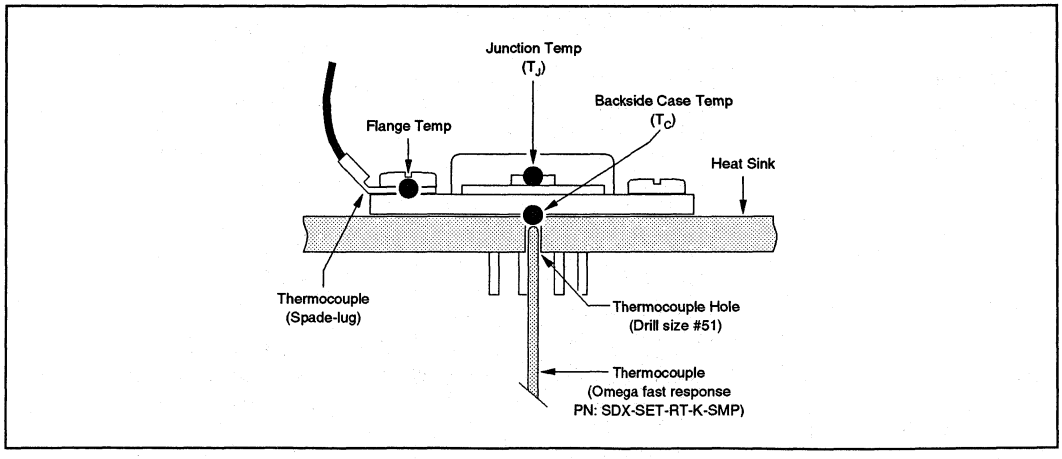


FIGURE 5. Package Case Thermal Measurement.

APPENDIX

MANUFACTURER	TO-3 SOCKET	GAGE JACKS	THERMAL GREASE	THERMAL PADS	HEAT SINKS	TEFLON TUBING	FASTENER HARDWARE	TEMP MEAS	ASM TOOLS
BURR-BROWN	0804MC								
CTI	X								
CONCORD		X							
Cambion		X							
Mill-Max		X							
NEWARK		X			X		X		
Thermalloy			X		X				
AAVID Engineering			X		X				
EG&G Wakefield			X		X		X		
BERGQUIST				X					
Power Devices				X					
Crayotherm				X					
Alpha Wire						X			
SPC Technology						X			
McMASTER-CARR							X		X
ASMCO							X		
OMEGA								X	

TABLE IV. Sources of TO-3 Mounting Hardware.

Alpha Wire Corp.
711 Lidgerwood Ave.
Elizabeth, NJ 07207-0711
(908) 925-8000

ASMCO
19 Baltimore St.
Nutley, NJ 07110
(201) 661-2600

AAVID Engineering, Inc.
One Kool Path
P.O. Box 4000
Laconia, NH 03247
(603) 528-3400

BERGQUIST
5300 Edina Industrial Blvd.
Minneapolis, MN 55435
(612) 835-2322

Cambion Division
MIDLAND ROSS
One Alewife Place
Cambridge, MA 02140
617) 491-5400

CONCORD
30 Great Jones St.
New York, NY 10012
(212) 777-6571

Crayotherm Corp.
1185 N. Van Home Way
Anaheim, CA 92806
(714) 630-2696

CTI Technologies, Inc.
7855 E. Evans Road, Suite A
Scottsdale, AZ 85260-3411
(602) 998-1484

EG&G Wakefield
60 Audubon Road
Wakefield, MA 01880
(617) 245-5900

McMASTER-CARR
P.O. Box 54960
Los Angeles, CA 90054-0960
(213) 692-5911

Mill-Max Mfg. Corp.
P.O. Box 300
190 Pine Hollow Road
Oyster Bay, NY 11771-0300
(516) 922-6000

NEWARK Electronics
4801 N. Ravenswood Ave.
Chicago, IL 60640-4496
(312) 784-5100

OMEGA
One Omega Drive
P.O. Box 4047
Stamford, CT 06907
(203) 359-1660

Power Devices
27071 Cabot Road, Bldg. 114
Laguna Hills CA 92653
(714) 582-6712

SPC Technology
4801 N. Ravenswood Ave.
Chicago, IL 60640
(312) 907-5181

Thermalloy, Inc.
2021 W. Valley View Lane
P.O. Box 810839
Dallas, TX 75381-0839
(214) 243-4321

BURR-BROWN® APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

HEAT SINKING — TO-3 THERMAL MODEL

Hubert Biagi (602) 746-7422

A critical issue with all semiconductor devices is junction temperature (T_J). T_J must be kept below its maximum rated value, typically 150°C. The lower the junction temperature the better.

The thermal circuit shown below allows temperature to be estimated with simple calculations. The temperature rise across each interface is equal to the total power dissipated in the device times the thermal resistance (PD • θ). An estimate of the junction temperature can be calculated using the following formula:

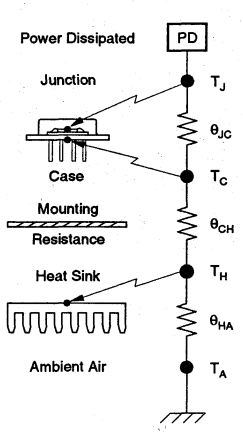
$$T_J = T_A + PD \bullet \theta_{JA}$$

Where,

$$\theta_{JA} = \theta_{JC} + \theta_{CH} + \theta_{HA}$$

T_A (°C) = Temperature of Ambient Air
T_J (°C) = Temperature of the Semiconductor Junction
PD (Watts) = Power Dissipated in Semiconductor
θ_{JC} (°C/Watt) = Thermal Resistance (Junction to Case)
θ_{CH} (°C/Watt) = Thermal Resistance (Case to Heat Sink)
θ_{HA} (°C/Watt) = Thermal Resistance (Heat Sink to Air)
θ_{JA} (°C/Watt) = Thermal Resistance (Junction to Air)

The following example shows typical values for a TO-3 package mounted in two different ways — one for high power applications, the other for low power applications. The value for θ_{JC} of 0.8°C/W is for the OPA512 operating under AC signal conditions. For DC signal conditions, θ_{JC} is about 1.4°C/W.



UNITS	HIGH POWER APPLICATION		LOW POWER APPLICATION	
Watts	100W	10W	10W	1W
°C	145°C	37°C *	158°C *	39°C
°C/Watt	0.8	0.8	0.8	0.8
°C	65°C	29°C	150°C	38°C
°C/Watt	0.1	0.1	0.5	0.5
°C	55°C	28°C	145°C	37°C
°C/Watt	0.3	0.3	12	12
°C	25°C	25°C	25°C	25°C

* Note, the difference in junction temperature that thermal resistance can make even when operating at the same power level.

Calculations begin at the bottom of the chart and assume 25°C ambient temperature in these examples. Each component of thermal resistance produces a temperature rise equal to the product of power dissipated and thermal resistance. The temperature of the junction is equal to the product of power dissipated and the total thermal resistance (PD • θ_{JA}).

Thermal resistances can vary significantly with particular models and mounting. While θ values can be obtained from specifications, calculated temperatures should be confirmed by measurements made at the bottom of the case.

BURR-BROWN® APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

THE MPC100 ANALOG MULTIPLEXER IMPROVES RF SIGNAL DISTRIBUTION

By Christian Henn

When designing high-performance systems for RF and video applications requiring amplifiers, multiplexers, DC restoration circuits, switched and continuous multipliers, or programmable gain amplifiers, finding the right component to do the job is not easy. The new 4 to 1 video multiplexer MPC100 opens the door to high-speed signal distribution without the headaches. This component contains four wideband open-loop amplifiers connected together internally at the output with a bandwidth of 180MHz at 1.4Vp-p signal swing. When the user selects one channel by applying a digital "1" to the corresponding SEL input (see Figure 1), the component acts as a buffer amplifier with a high input impedance of 0.88MΩ||1pF and a low output impedance of 11Ω.

The MPC100 can be used to design a bus-controlled distribution field, as shown in Figure 3. In this application, a driver device, which is controlled by a memory and a parallel-to-serial converter, shifts the information about the field state into the output latches, U_1, U_2, and U_3. When the strobe line is triggered the new latch information is stored in the output latches, which controls whether the buffers of the MPC100 (U4-U9) are in an "on" or "off" state. The MPC100 operates with a fast make-before-break switching action to keep the output switching transients small and short. As shown in Figure 2, the switching time from one channel to the next is less than 0.5µs, and the signal envelope during transition rises and falls symmetrically and shows practically no overshoot or DC settling effects. A transmission

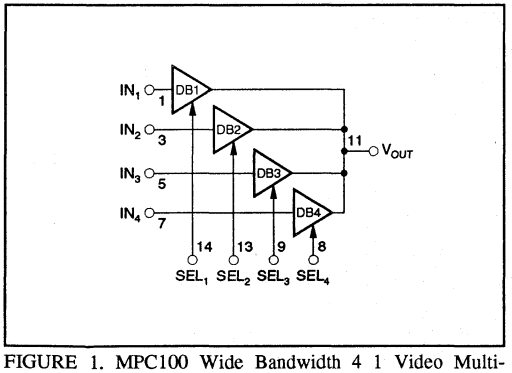


FIGURE 1. MPC100 Wide Bandwidth 4 1 Video Multiplexer.

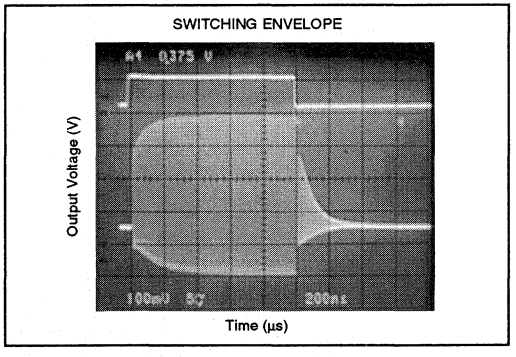


FIGURE 2. Switching Time from Channel to Channel of the MPC100.

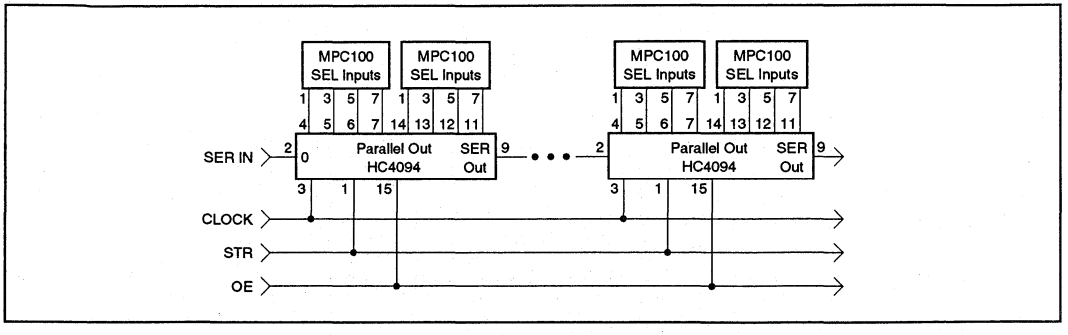
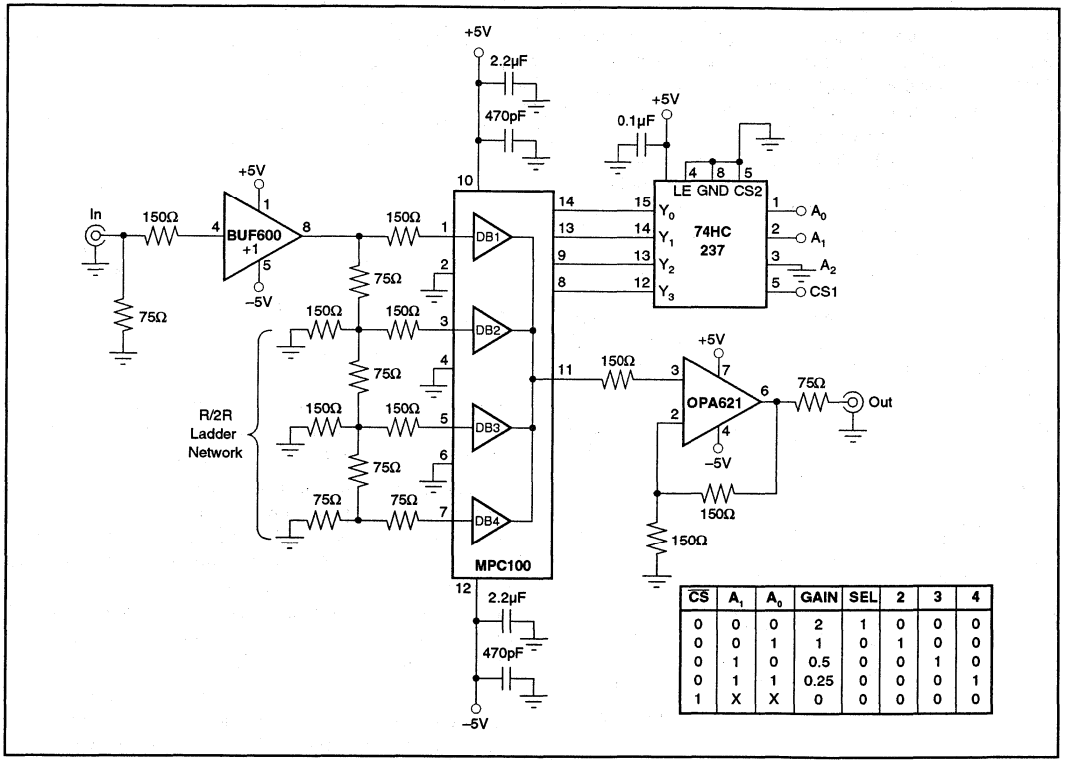


FIGURE 3. Serial Bus-controlled Distribution Field Using the MPC100.

rate of up to several MHz ensures control during the vertical blanking line, even in huge crosspoint fields.

Figure 4 shows the MPC100 used in a digitally controlled amplitude control system. With one MPC100, it is possible to perform four amplitude steps. Two MPC100s will perform eight steps. The R/2R ladder network used in this application varies the output swing by a factor of two when switching from one channel to the other, the highest gain being G = 1. The BUF600 decouples the RF input and drives the resistor network, which is connected from the amplifier's output to ground. The taps of the ladder network are tied to the channel inputs of the MPC100. A 74HC237 decoder controls the channel selection. As illustrated in the truth table in Figure 4, a two-bit logic can vary the amplitude of the RF signal at the output of the subsequent OPA621 within less than 0.5µs from a gain of zero when all channels are off to gain of two when DBI is selected. The digital amplitude control can easily be combined with an AGC amplifier. The MPC100 sets the rough range and the AGC circuit the fine tuning.

The MPC100 is available in a 14-pin plastic DIP or plastic SOIC package. Other performance highlights are low interchannel crosstalk (<60dB in SO package), a low differential gain of 0.05%, low phase errors of 0.01 degrees, a low quiescent current of ±230µA when no channel is selected.



$\overline{CS}$	A_1	A_0	GAIN	SEL	2	3	4
0	0	0	2	1	0	0	0
0	0	1	1	0	1	0	0
0	1	0	0.5	0	0	1	0
0	1	1	0.25	0	0	0	1
1	X	X	0	0	0	0	0

FIGURE 4. Digital Gain Control Circuit Using the MPC100.

BURR-BROWN® APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

MAKE A PRECISION CURRENT SOURCE OR CURRENT SINK

By R. Mark Stitt (602) 746-7445

A frequently asked question, not answered by the guide, has been: "How do I make the world's most accurate current source and current sink?" Figures 1 and 2 respectively show the circuits for making precision current sources and sinks.

The precision current source and sink are based on the new REF102 10.0V voltage reference. With 2.5ppm/°C V_{OUT} drift, and better than 5ppm/1000hrs long-term stability (see table on page 2), this buried-zener-based voltage reference offers the best performance available from a single-chip voltage reference today. The REF200 uses a band-gap type reference to allow low-voltage two-terminal operation. This makes it a good general-purpose part, but its drift and stability and initial accuracy cannot compare to that of the REF102.

The current source is shown in Figure 1. The voltage-follower connected op amp forces the voltage reference ground connection to be equal to the load voltage. The reference output then forces an accurate 10.0V across R_1 so that the current output is $10V/R_1$.

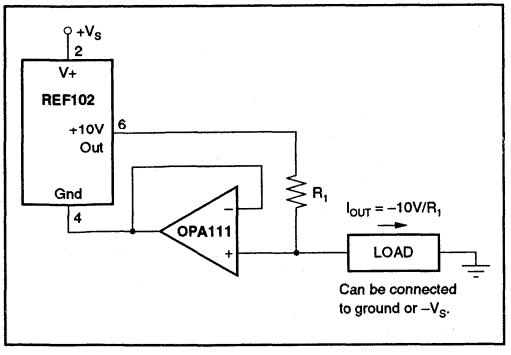


FIGURE 1. Precision Current Source.

The current sink is shown in Figure 2. The op amp drives both the voltage reference ground connection and the current-scaling resistor, R_1, so that the voltage reference output is equal to the load voltage. This forces –10.0V across R_1 so that the current sink output is $-10V/R_1$. The R_2, C_1 network provides local feedback around the op amp to assure loop stability. It also provides noise filtering. With the values shown, the reference noise is filtered by a single pole with $f_{-3dB} = 1/(2 \cdot \pi \cdot R_2 \cdot C_1) = 16kHz$.

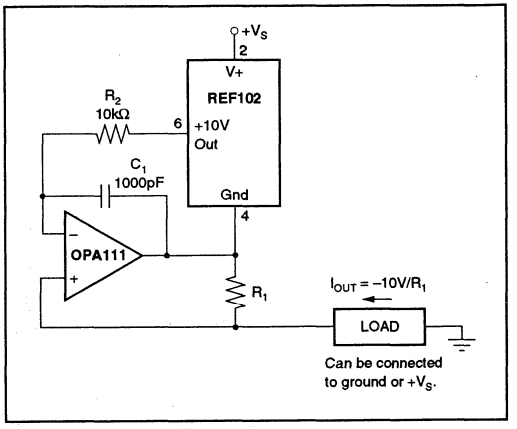


FIGURE 2. Precision Current Sink.

Compliance of the circuit depends on input and output range of the op amp used and the 11.4V minimum supply range of the REF102. The application guide goes into more detail.

Keep in mind that the accuracy of a voltage-reference-based current source depends on the absolute accuracy of the current scaling resistor (R_1). The absolute TCR and stability of the resistor directly affect the current source temperature drift and stability. If you use a 50ppm/°C resistor (common for 1% metal film resistors), the precision current source will have approximately 50ppm/°C drift with temperature—worse than the 25ppm/°C drift of a REF200.

The performance of circuits using current source references depends only on the ratio accuracy of the scaling resistors. It is much easier to get good resistor ratio accuracy than to get good absolute accuracy, especially when using resistor networks.

Burr-Brown offers a wide variety of support components which are excellent choices for generation or conversion of current. Application Guide (AN-165) has proven valuable in selecting these components.

REF102CM +10.0V REFERENCE STABILITY vs TIME

T_A = 25°C, V_S = +15V.

UNIT	V_{OUT} CHANGE FROM 1 HR TO 168 HRS [ppm]	V_{OUT} CHANGE FROM 1 HR TO 1008 HRS [ppm]	V_{OUT} CHANGE FROM 1 HR TO 2016 HRS [ppm]	V_{OUT} CHANGE FROM 1 HR TO 3072 HRS [ppm]	V_{OUT} CHANGE FROM 1 HR TO 5136 HRS [ppm]	V_{OUT} CHANGE FROM 1 HR TO 14205 HRS [ppm]
1	6.8	5.5	7.1	4.7	8.2	11.7
2	5.1	1.0	1.2	–2.1	0.1	1.3
3	9.4	6.5	3.2	1.0	1.8	2.0
4	9.6	6.9	7.7	5.6	7.6	10.3
5	12.9	7.8	9.6	6.7	9.5	12.8
6	10.5	6.4	5.3	3.0	5.4	9.4
7	10.3	5.7	6.2	3.7	5.8	8.2
8	17.0	14.5	12.9	9.2	9.9	13.7
9	6.2	5.1	3.8	1.7	2.7	4.1
10	7.1	1.7	1.3	0.1	1.0	2.4
11	13.0	9.6	9.6	10.0	13.0	16.5
12	7.5	4.7	3.9	4.2	5.0	7.4
13	13.0	9.5	10.4	8.2	9.9	13.7
14	4.2	3.0	0.5	–0.3	4.2	2.8
15	7.3	4.3	2.6	1.8	4.1	3.9

BURR-BROWN® APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

VOLTAGE-REFERENCE FILTERS

By R. Mark Stitt (602) 746-7445

IMPROVED VOLTAGE-REFERENCE FILTER HAS SEVERAL ADVANTAGES

- LOW OUTPUT IMPEDANCE AT HIGH FREQUENCY FOR DRIVING DYNAMIC LOADS SUCH AS HIGH-SPEED A/D CONVERTERS
- IMPROVED NOISE FILTERING
- BETTER ACCURACY BY ELIMINATING CAPACITOR LEAKAGE ERRORS
- DRIVES LARGE CAPACITIVE LOADS

The Burr-Brown REF102 is a buried-zener-based precision 10.0V reference. It has better stability and about five times lower output noise than band-gap-based voltage references such as the PMI REF-10. Still, its output noise is about 600μVp-p at a noise bandwidth of 1MHz (the output noise of the PMI REF-10 is about 3,000μVp-p at 1MHz).

So far as we know, the stability with time of the REF102 is significantly better than any other single-chip voltage reference on the market. We plan more characterization of stability vs time, but it will probably not be available this year. The following preliminary data is all we have for now. The devices used were off-the-shelf. They were not burned-in, or otherwise stabilized prior to this stability test.

Noise of a voltage reference can be reduced by filtering its output. Broadband noise can be reduced by the square-root of the reduction in noise bandwidth. Filtering the output of the reference to reduce the noise bandwidth by 100/1 (from 1MHz to 10kHz, for example) can reduce the noise by 10/1 (from 600μVp-p to 60μVp-p).

The conventional circuit, shown in Figure 1, uses a single-pole RC filter and a buffer amplifier. One problem with this circuit is that leakage current through the filter capacitor, C_1, flows through R_1 resulting in DC error. Furthermore, changes in leakage with temperature result in drift. The relatively low RC time constants often needed dictate large capacitor values prone to this problem.

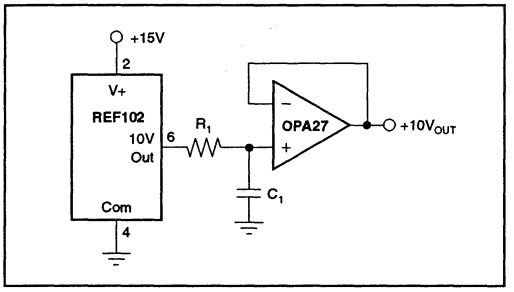


FIGURE 1. Voltage Reference with Conventional Filter.

REF102CM +10.0V REFERENCE STABILITY vs TIME

T_A = 25°C, V_S = +15V.

UNIT	V_{OUT} CHANGE FROM 1 HR TO 168 HRS [ppm]	V_{OUT} CHANGE FROM 1 HR TO 1008 HRS [ppm]	V_{OUT} CHANGE FROM 1 HR TO 2016 HRS [ppm]	V_{OUT} CHANGE FROM 1 HR TO 3072 HRS [ppm]	V_{OUT} CHANGE FROM 1 HR TO 5136 HRS [ppm]	V_{OUT} CHANGE FROM 1 HR TO 14205 HRS [ppm]
1	6.8	5.5	7.1	4.7	8.2	11.7
2	5.1	1.0	1.2	–2.1	0.1	1.3
3	9.4	6.5	3.2	1.0	1.8	2.0
4	9.6	6.9	7.7	5.6	7.6	10.3
5	12.9	7.8	9.6	6.7	9.5	12.8
6	10.5	6.4	5.3	3.0	5.4	9.4
7	10.3	5.7	6.2	3.7	5.8	8.2
8	17.0	14.5	12.9	9.2	9.9	13.7
9	6.2	5.1	3.8	1.7	2.7	4.1
10	7.1	1.7	1.3	0.1	1.0	2.4
11	13.0	9.6	9.6	10.0	13.0	16.5
12	7.5	4.7	3.9	4.2	5.0	7.4
13	13.0	9.5	10.4	8.2	9.9	13.7
14	4.2	3.0	0.5	–0.3	4.2	2.8
15	7.3	4.3	2.6	1.8	4.1	3.9

Another problem with the conventional filter is the added noise of the buffer amplifier. The noise of the buffer amplifier acts at the buffer's full unity-gain bandwidth adding to the output noise of the circuit. Even if the noise at the output of the RC filter is zero, the noise added by the buffer can be intolerable in many applications. The improved filter, shown in Figure 2, solves both problems.

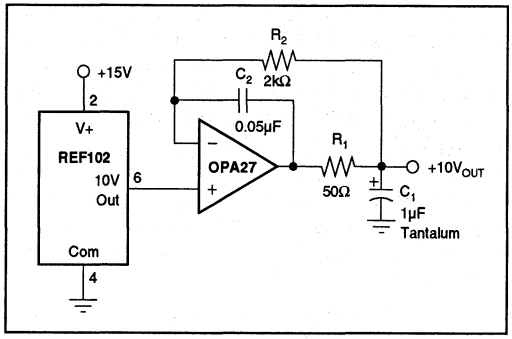


FIGURE 2. Voltage Reference with Improved Filter.

The improved filter places the RC filter at the output of the buffer amplifier. Reference noise is filtered by a single pole of $f_{-3dB} = 2 \cdot \pi \cdot R_1 \cdot C_1$. The R_2, C_2 network assures amplifier loop stability. Set $R_2 \cdot C_2 = 2 \cdot R_1 \cdot C_1$ to minimize amplifier noise gain peaking. Since buffer amplifier bias current flows through R_2, keep the value of R_2 low enough to minimize both DC error and noise due to op amp bias-current noise. Also, load current flows in R_1. The resulting voltage drop adds to the required swing at the output of the buffer amplifier. Keep the voltage drop across R_1 low, e.g. less than 1V at full load, to prevent the amplifier output from saturating by swinging too close to its power-supply rail.

With the RC filter at the output of the buffer, the noise of both the voltage reference and the buffer is filtered. Since the filter is in the feedback loop of the buffer amplifier, C_1 leakage current errors reacting with R_1 are divided down to an insignificant level by the loop gain of the buffer amp. The feedback also keeps the DC output impedance of the improved filter near zero. Also, leakage through C_2 is negligible since the voltage across it is nearly zero.

At high frequency, the output impedance of the improved filter is low due to C_1. The reactance of a 1µF capacitor is 0.16Ω at 1MHz. For an A/D converter reference, connect C_1 as close to the reference input pin as possible.

The improved filter can drive large capacitive loads without stability problems. Just keep $(C_{LOAD} + C_1) \cdot R_1 < 0.5 \cdot R_2 \cdot C_2$.

There is one caution with the improved filter. Although the output impedance is low at both high frequencies and DC, it peaks at midband frequencies. Reduced loop gain due to the R_2, C_2 network is responsible. A peak output impedance of about $0.7 \cdot R_1$ occurs near the filter pole frequency. If lower midband output impedance is required, R_1 must be reduced and C_1 increased accordingly.

BURR-BROWN® APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

CAREFUL LAYOUT TAMES SAMPLE-HOLD PEDESTAL ERRORS

by Anthony D. Wang

In most sampling systems, the inherent characteristics of the sample-hold dictate its overall performance. However, one error source that sample-hold users do have under their direct control is the external charge injection from the digital control signal. This is known as charge transfer when measured in coulombs or as charge offset when measured in volts. It is often also known as pedestal because of its manifestation as a step change to the output. The culprit is generally the parasitic capacitance between the digital control pin and some sensitive node(s) of the circuit.

Figure 1 shows the pinout of the SHC5320 with the addition of a parasitic capacitor between pins 1 (inverting input) and 14 (the mode control pin). The inverting input is the closest pin to the digital control signal that is sensitive enough to amplify the parasitic feedthrough.

This is a typical coupling path because a convenient layout approach would be to close the feedback loop between the output and the inverting input by routing the trace under-

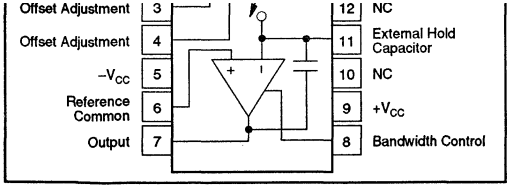


FIGURE 1. SCH5320 Pinout With Cp, Parasitic Capacitance.

Although the output of the sample-hold is considered a low impedance node, this is not true at all frequencies. The output impedance is kept low by the open-loop gain of the amplifier. As the open-loop gain falls, the output impedance rises and the amplifier is unable to swallow the high frequency component of the parasitically coupled signal.

The correct layout technique would minimize the surface area exposure between the inverting input node and the digital sample-hold control pin. Routing the feedback trace underneath the unit, as mentioned previously, would be acceptable if the line were kept to minimum width and spaced well away from the mode control line. Ideally, only one of those two traces would route beneath the package. Precautions should also be taken for two other pins that are sensitive to coupling from the digital control pin. These are pins 11 (external hold capacitor) and 8 (bandwidth control).

In case the sample-hold is configured for gain with a feedback network, position the resistors such that their junction with the inverting input occurs as close to that pin as possible. If pedestal error still results, lower the feedback network resistor values to reduce the sensitivity of this node to parasitic coupling.

A more insidious parasitic path occurs when sockets are used. Figure 2 shows the signal coupled across an empty socket. The attenuation is roughly 50dB, but can still provide enough of a signal to cause a significant pedestal error. This is suitably documented by the scope photo in Figure 3.

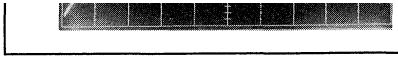


FIGURE 2. Signal Coupling from Pin 14 to Pin 1 for Empty Textool Socket.

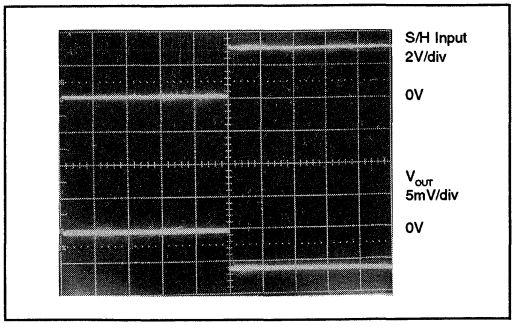


FIGURE 3. Pedestal Error Resulting from the Use of a Textool Socket.

The sample-hold was configured as a unity gain follower with its input grounded. The output trace displays a pedestal error of –6mV. Note that this is a negative excursion due to the rising edge of the digital mode control signal coupling to the inverting input of the sample-hold circuit.

The best way to avoid this is to solder the sample-hold directly into the board. If hard soldering is not a viable option, avoid the use of high profile sockets, especially the zero insertion force type. The optimum approach uses zero profile solderless sockets (such as Augut P/N 8134-HC-5P2).

The waveforms in Figure 4 confirm that a test board built with the zero profile pin connectors shows no evidence of signal coupling from the digital control pin to the inverting input. The board layout uses the technique mentioned earlier of routing a minimum width feedback trace underneath the circuit. In this example, the socket is empty and the signals are measured just as they were in Figure 2.

Figure 5 demonstrates the reward for the attention to detail covered by this discussion. The pedestal is a barely perceptible –0.5mV for the same unity gain configuration and for the same unit as illustrated in Figure 3.

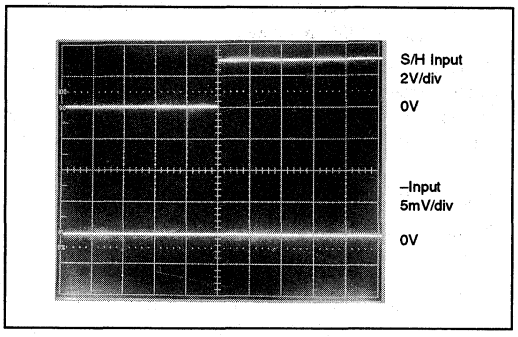


FIGURE 4. Signal Coupling from Pin 14 to Pin 1 for Empty Zero Profile Socket.

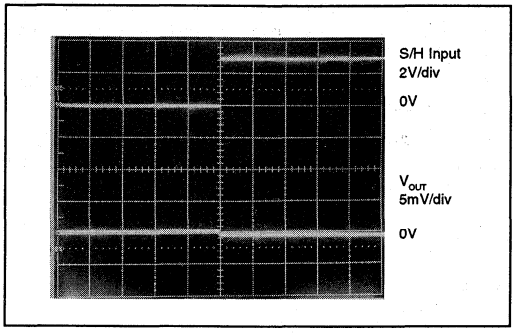


FIGURE 5. Pedestal Error Resulting from the Use of a Zero Profile Socket.

BURR-BROWN® APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

DC-TO-DC CONVERTER NOISE REDUCTION

The inherent switching inside the DC-to-DC converter gives rise to potential sources of noise. This noise manifests itself on the output voltage as spikes at the switching frequency. Due to size and cost requirements, internal filtering is limited but usually adequate for most applications. When excessive noise is suspected, you must rule out extraneous noise sources. Figure 1 illustrates two recommended methods for testing output voltage ripple and noise.

If your circuit requires less noise than the supply is capable of, there are two preferred filter techniques—LC filters or an output filter capacitor.

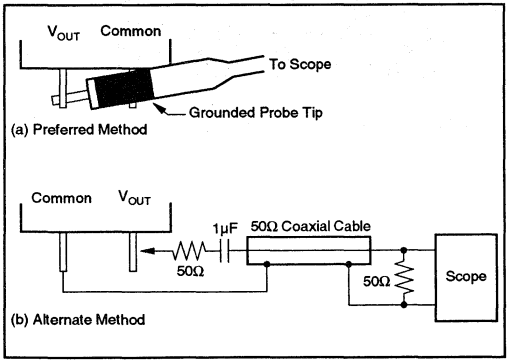


FIGURE 1. Recommended Noise Measurement Methods.

LC FILTERING

For applications requiring higher accuracy, such as analog measurements, LC filters should be used on each channel to attenuate high-frequency noise. Because of the output filter capacitor already present in the DC-to-DC converter, adding an inductor and capacitor to the output creates a pi filter (Figure 2).

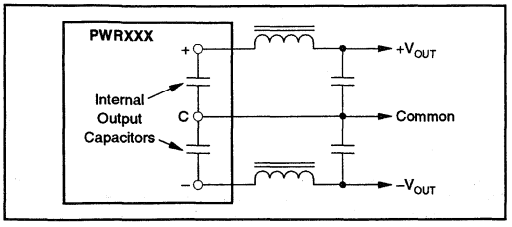


FIGURE 2. Output "PI" Filters.

It is important that the inductor wire size can carry the load current, including a safety factor, and that the core does not saturate. Also notice that the DC resistance of the inductor is outside the feedback loop for regulated units and subsequently degrades that regulation.

LC filters are generally used only where very accurate analog measurements are being taken, and the power supply rejection is poor at the ripple frequency. A much more common filtering technique is the output filter capacitor.

CHOOSING AN OUTPUT CAPACITOR

The saying "the more the better" is definitely not applicable to output capacitors of switching type power supplies. The basic design equations of the supply rules out any brute force approach. The parameter of major concern is the Effective Series Resistance (ESR). ESR is due to stray resistance inside the electrolytic capacitor that becomes significant at switching power supply frequencies and higher. Together with Effective Series Inductance (ESL), ESR can be modeled as the equivalent circuit shown in Figure 3.

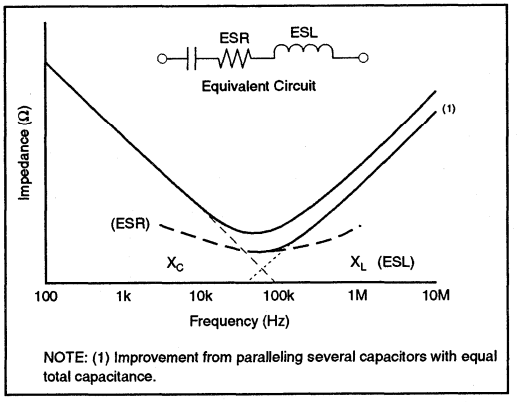


FIGURE 3. Typical Log/Log Impedance Plot for Aluminum Electrolytic Capacitor.

ESR is also a function of temperature and actually decreases as temperature is increased. This temperature dependency is particularly strong in the below zero range as shown in Figure 4. This, together with decreasing capacitance (Figure 5), can prove fatal to a switcher design that performed well on the bench.

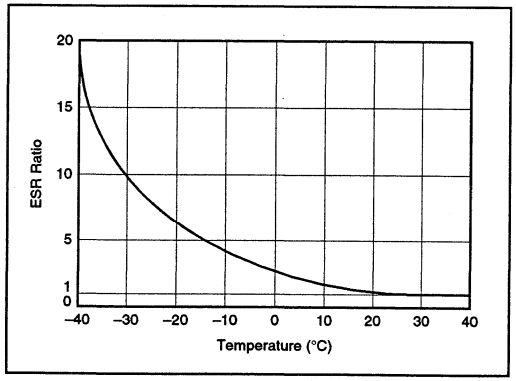


FIGURE 4. ESR Ratio Relative to Room Temperature.

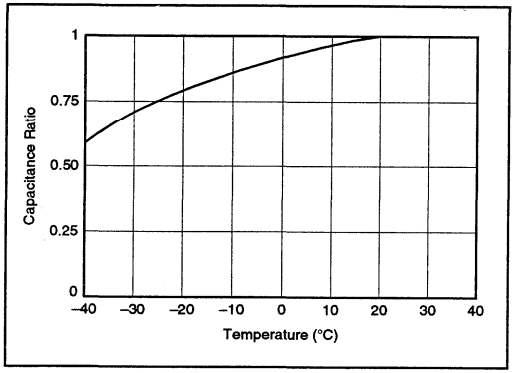


FIGURE 5. Capacitive Ratio Relative to Room Temperature.

The ESR becomes, in effect, a voltage divider with the internal output resistance of the supply. Therefore, the lower the ESR, the better suited the capacitor is for filtering the output of a switching type power supply. As the load increases, the capacitors' ripple current increases, causing a larger drop across the ESR, and consequently, a larger output ripple voltage (seen as noise). A commonly used method for estimating ESR is by means of the equation:

$$ESR = DF \times 0.01/2\pi fC$$

Where DF is given in %, f is given in hertz, and C is given in farads. Dissipation factor (DF) is a function of frequency and is useless if given at less than 1kHz. (If given at lower frequencies, it is more indicative of equivalent parallel resistance.) If given at 1kHz or greater, the above equation applies. Typical values are 8% to 24% at 1kHz for solid tantalums, and 0.1% to 3% at 1kHz for ceramics, and 8% at 120Hz for aluminum electrolytics. Most tantalum and aluminum electrolytic capacitor manufacturers do not specify the ESR, probably because it is not worth bragging about. One way of reducing ESR is to put two or more capacitors in parallel that add to the needed capacitance and reduce the ESR by the parallel resistance relation (see note in Figure 3). The second capacitor may be 1/10 or 1/100 the capacitance of the first, since it will provide bypassing for higher frequencies.

There are two basic families of electrolytic capacitors from which to choose: aluminum and tantalum. Aluminum types are available in many quality grades and fabrication techniques. Tantalum types come in foil, solid, and wet-slug subtypes. At first, this may present a bewildering array of choices, but these can quickly be reduced by your particular need. Cheap aluminum electrolytics of questionable quality are often used but all too frequently this leads to actual noise generation, with poor reliability, and, in general, criticisms of high frequency switching type supplies. Good quality aluminum electrolytics probably provide the best compromise, if one must be made, between cost and performance. These are "computer grade" and other types made especially for switchers. Some have specialized construction that produce very low ESR and ESL rather than low cost. The outstanding feature of all tantalum types is their high capacitance to volume efficiency. This is particularly seen in the wet-slug tantalum, an undisputed winner in the capacitance versus volume contest. Solid tantalums appeal where there is a great emphasis on longevity, both shelf life and operating life. The foil-type tantalum is a very good capacitor for switchers but is not cost competitive with aluminum types. Where switching frequencies are very high (1MHz and greater) and current demands are low, nonelectrolytic capacitors will probably replace the previously discussed electrolytics, providing bypassing at high frequencies where the ESL of electrolytics becomes too high.

In addition to considering the capacitance, ESR, ESL, and appropriate voltage derating for the application, most capacitors have a maximum rms ripple current (or max rms ripple voltage) rating which should not be exceeded. Ripple current can be estimated by $i_{RMS} = i_{P-P}/3.5$ (or $V_{RMS} = V_{P-P}/3.0$). These ratings are too often ignored, but the stress produced by exceeded ripple will adversely effect the lifespan of the output filter capacitor. The effect of ripple current flowing in the output capacitor is the dissipation of heat in the capacitor's ESR. Heat kills electrolytics in two ways—electrolytic depletion and electrolytic evaporation. The rate at which the electrolyte is lost depends on the electrolyte itself and the capacitor's internal structure. But whatever that rate, tests by aluminum capacitor makers indicate it nearly doubles for each 10°C rise in temperature. Thus, each 10°C rise nearly cuts the usable life of an aluminum capacitor in half. The best approach to counter this problem is to use capacitors designed and rated for higher temperatures.

Whatever capacitor is selected, its effective use depends greatly upon wiring techniques. For example, inductance can become dominant if good wiring practices are not followed and a low ESL requirement can be reduced through very careful wiring. Place the capacitor as close as possible to the load rather than the power supply. The reason for this

is the presence of inductance in the wire or PCB trace and the existing output capacitor inside the supply. A small pi filter is formed furthering the reduction of noise. Capacitor lead length including circuit wiring on both sides of the capacitor should be minimized. Short, wide straps are the best and these can be paralleled for further reduction in self-inductance.

It's true that good capacitors have played a big role in making switching type power supplies a technological and commercial success, but this success has inspired the capacitor makers to devise even better suited types. Because of this impetus and the versatility of the switching power supply, it is difficult to say that one type of capacitor is inherently better than another. Most capacitor manufacturers are willing and able to provide advice that would help you in your decision.

BURR-BROWN® APPLICATION BULLETIN

Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

10MHz ANALOG MULTIPLIER CARRIES OUTPUT AMP, BREAKS BANDWIDTH BARRIER

A transconductance multiplier chip, the first one fitted with an output amplifier, alleviates design worries in high-bandwidth communication circuits.

Beyond a 1MHz bandwidth, multiplier chips usually need external amplifiers and biasing, and many cannot deliver their promised accuracy and performance without external trimming components. Those burdens have largely kept single-chip multipliers out of communication applications. Mixer circuits, for example, have instead relied on signal-diode rings, even though those rings bring their own performance drawbacks, including poor low-frequency response and narrow frequency and power ranges.

With the introduction of the MPY634 multipliers, wideband analog multiplication need no longer be a multichip affair or imply performance compromises. Along with its 10MHz small-signal bandwidth, the four-quadrant chip has a laser-trimmed DC accuracy of 0.25%, an adjustable scale factor, and the ability to drive loads down to 2kΩ.

In addition, because it has three instead of two differential input pairs, the chip can divide, square, and find square roots. Those functions make it, in effect, a multifunction converter. As a result, adding just a few components creates any number of analog processors, including a voltage-controlled filler or a mixer.

The chip unites three voltage-to-current input converters, a transconductance core, a highly stable voltage reference, and a high-gain output amplifier (Figure 1). The three converters can be viewed as differential amplifiers with an extremely low transconductance. The benefits of which are a 10MΩ input impedance and a 20V/μs slew rate. Moreover, the converters' input voltages can be differential or single-ended; in the latter case, the second input can be used to nullify offsets.

HAVING THE DRIVE

The differential outputs of the converters drive the transconductance core, which actually performs the multiplication. The output of the core, a differential current, produces a voltage across a resistive load that feeds a high-gain, high-bandwidth amplifier. For multiplication, the output of the amplifier is fed back to converter Z; other mathematical operations are set up by different feedback connections.

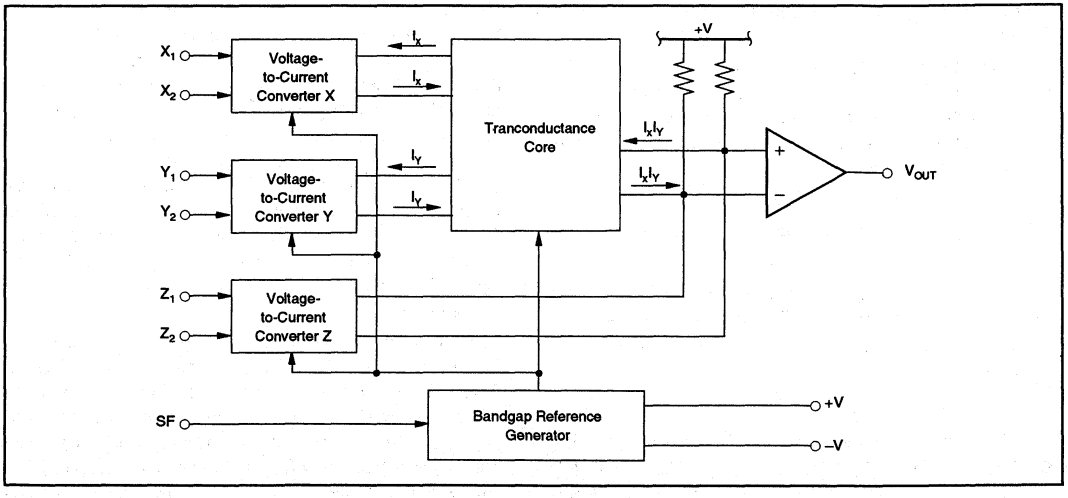


FIGURE 1. The MPY634 Multiplier Chip is the First to Break the 1MHz Barrier. Without the external wideband amplifier, a suitable alternative to diode mixers. It combines three voltage-to-current converters, a transconductance core, a voltage reference, and an output amplifier.

Like any mathematical circuit, the multiplier is only as good as its linearity, accuracy, and stability. Here linearity and accuracy depend on the transconductance core, and more specifically, on how precisely the base-to-emitter voltages of its six transistors match. To maximize linearity, the transistors are diagonally coupled (cross-coupled) on the die and then laser-trimmed.

Maintaining a constant scale factor over temperature requires stable bias current in the core. A built-in bandgap reference keeps the scale factor's temperature coefficient within 30ppm/°C over a temperature range of –55°C to +125°C. Nevertheless, the scale factor can be adjusted over the range of 10V to 3V by connecting a resistor from the negative supply to the Scale Factor Adjust pin.

As with an op amp, the multiplier's open-loop equation offers insight into the chip's operation, as well as into its constraints. The open-loop equation is:

$$V_{OUT} = A\left[\frac{(X_1 - X_2)(Y_1 - Y_2)}{SF} - (Z_1 - Z_2)\right]$$

where:

V_{OUT} is the output voltage;

A is the output amplifier's open-loop gain and is assumed to be infinite;

X_N, Y_N, and Z_N are input voltages;

SF is the scale factor, which is nominally 10V.

For stability, feedback is applied to one or more inputs. (However, when feedback involves more than one input, designers must take care that the overall feedback does not become positive.) Since the gain is always positive, inputs that receive feedback become dependent on the output voltage. Thus, the behavior of the circuit can be predicted by substituting V_{OUT} (or its function) for the appropriate input voltage.

For example, in a basic multiplier with single-ended inputs and no offset, X_2, Y_2, and Z_2 all equal zero. Feedback enters directly through the Z_1 input. Because converter Z drives the output amplifier's inverting input, the feedback is negative and the output voltage is given by:

$$V_{OUT} = A\ (X_1Y_1/SF - V_{OUT})$$

When A approaches infinity, the equation gives:

$$V_{OUT} = X_1Y_1/SF$$

Applying the feedback through a voltage divider increases the overall gain. For example, if a 10:1 attenuator makes Z_1 equal $0.1V_{OUT}$, as gain becomes infinite the open-loop equation becomes

$$V_{OUT} = 10\ X_1Y_1/SF$$

To make a divider circuit, single-ended inputs X_2, Y_1, and Z_2 are grounded. The feedback is applied to Y_2 so that it is negative for positive values of X_1. However, if X_1 is negative, then Y_2 is grounded and the feedback is applied to Y_1 In either case, the open-loop equation is:

$$V_{OUT} = A\left[\frac{(X_1)(-V_{OUT})}{SF} - Z_1\right]$$

As gain approaches infinity, V_{OUT} becomes Z_1/X_1SF.

The scope of the multiplier chip becomes apparent in a highly accurate voltage-controlled filter. Two multiplier chips, a universal active filter chip, four resistors, and six bypass capacitors team up to form a second-order filter with high-pass, low-pass, and bandpass outputs (Figure 2). The multipliers act like linear voltage-controlled resistors that set the filter's center frequency and thus the cutoff frequency of the high- and low-pass outputs. Although the active filter chip allows a compact implementation for bandwidths up to 200kHz and a Q of up to 500, the bandwidth can be extended to 1MHz by implementing the filter with discrete op amps instead.

Precision 1% resistors ensure accurate values for the full-scale center frequency and for Q. Two such resistors, between each multiplier's output and the filter chip, determine the full-scale frequency, which is the center frequency of the bandpass for a 10V control voltage. In operation, a control voltage drives both multipliers at once and must always be greater than 0V. If the voltage falls to zero or goes negative, the feedback around the filter chip is lost and the circuit becomes unstable.

With 0.1% resistors, the filter holds its full-scale frequency to 2% over a 10:1 range of control. Moreover, no external trimming adjustments are required, unless accuracy must be raised even further (in which case the input offsets can be nulled by trimming). The bandpass and cutoff frequencies drift no more than ±50ppm/°C over –55°C to +125°C. At a full-scale frequency of 25kHz, the wideband noise is typically less than 160µV. The output swing can go as high as 20Vp-p, yielding a dynamic range of 96dB.

Limits on the slew rate of the amplifiers inside the universal active filter restrict the input amplitude and Q. First, since the filter's internal amplifiers handle a maximum slew rate of 10V/µs, the full power bandwidth (10Vpk) is 160kHz compared with the gain bandwidth product of 4MHz As a result, the input voltage should be limited to 20Vp-p below 80kHz and 2Vp-p between 80 and 500kHz. Above that, the maximum input voltage is determined by the formula f_C/50,000, where f_C is the filter's cutoff frequency. Second, a high Q can make internal voltages larger than the input swing. Thus the maximum Q is below 4kHz and f_C/20,000 above 4kHz.

The high performance of this voltage-controlled oscillator justifies the use of the multiplier and the universal active filter. Though a switched-capacitor filter and a voltage-controlled oscillator represent an easier and less costly alternative, the arrangement's 75dB dynamic range and 30kHz upper frequency fall far short of the multipler-based configuration. Moreover, the switched-capacitor approach suffers from clock feedthrough and aliasing, which dictate additional filtering.

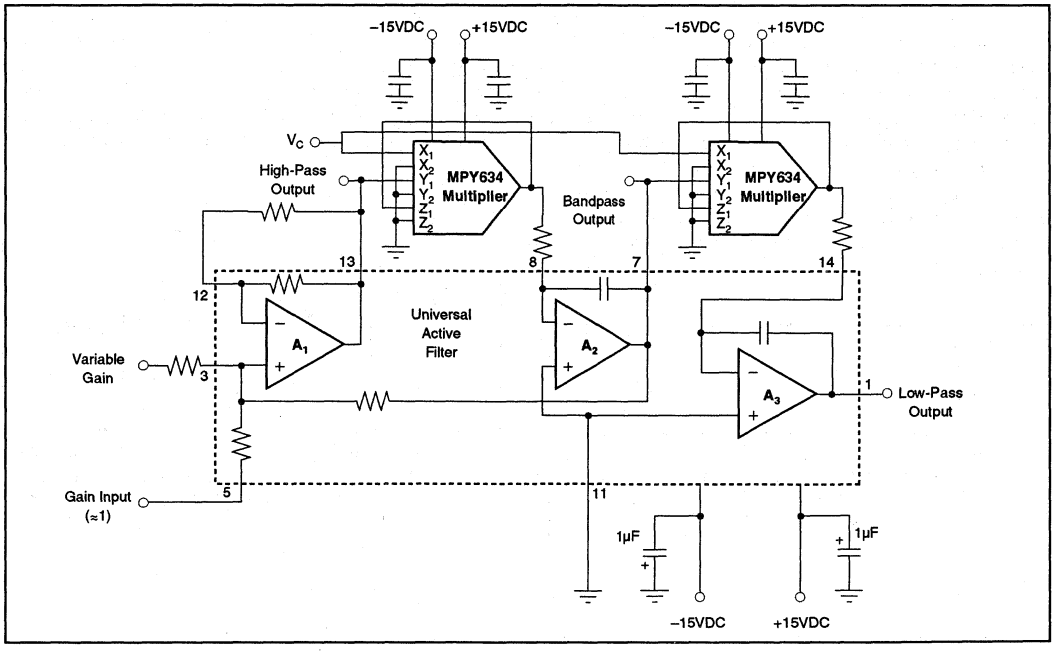


FIGURE 2. A Voltage-Controlled Second-Order Filter Revolves Around Two Multiplier Chips and a UAF42 Universal Active Filter. The multipliers act as linear voltage-controlled resistors that vary the center and cutoff frequencies of the active filter chip.

Since this transconductance multiplier needs no external circuitry to attain its wide bandwidth, it is a particularly good choice for building low-cost mixer circuits (see "Strike up the Bandwidth"). Mixers form the heart of heterodyning, which is used for modulating and demodulating signal amplitude.

A ring-diode circuit, one of the most common types of mixers, performs well at high frequencies but suffers numerous limitations. For instance, since the diodes in the ring must be biased, transformers must be coupled at the mixer's input and sometimes at the output. Unfortunately, transformer coupling precludes low-frequency operation. The low-end frequency of most diode mixers is limited to several hundred kilohertz, preventing them from modulating RF signals directly with audio signals.

On the other hand, the transconductance mixer is directly coupled and thus can modulate audio signals directly onto an RF carrier. For example, the amplitude of a 10MHz carrier can be modulated simply by applying an audio signal to the X input of the multiplier chip and feeding the output of a 10MHz local oscillator to the Y input.

A ring-diode mixer also requires a resistive impedance, usually 50Ω, at its input and output ports. A reactive impedance can severely degrade performance. The transconductance mixer, in contrast, is relatively insensitive to I/O impedances. At low frequencies, its input impedance is 10MΩ and, at about 1MHz, that starts to drop off, falling to a low of 25kΩ at 10MHz. If required, a 50Ω resistor can be shunted across the input to match impedances. The output is insensitive to load impedances greater than 2kΩ and less than 1000pF.

Transconductance mixers exhibit better linearity than typical double-balanced diode mixers (see the table). The input voltage to diode mixers is applied directly to the diode junction, so that the region of linear operation is small. Any nonlinearity causes harmonic distortion and feedthrough, which adversely affect almost all specifications. In addition, it generates spurious carriers, intermodulation distortion, and increased feedthrough. Within the transconductance mixer, the input voltage is converted into a current before being applied to the core, affording a much wider range of linear operation.

One mixing application combines a 1kHz low-pass filter with a 5MHz local oscillator to create a bandpass filter with an extremely high Q of 5000—normally an impractical if not impossible achievement. In a passive network, reaching that Q would necessitate many poles, which are difficult and costly to tune. In addition, a typical active circuit version would require expensive op amps with high gain-bandwidth products.

The input signal is first multiplied by the local oscillator and then sent through the low-pass filter (Figure 3). Since the filter has a 1kHz bandwidth, it passes all incoming components between the local oscillator frequency and 1kHz above it. The filter's output is then reconverted into the original frequency by multiplying it by the local oscillator output. An image frequency is created when the signal is reconverted. The circuit can also translate the center frequency of a bandpass filter, a useful feature when the required filter falls outside of the commonly available communications frequencies.

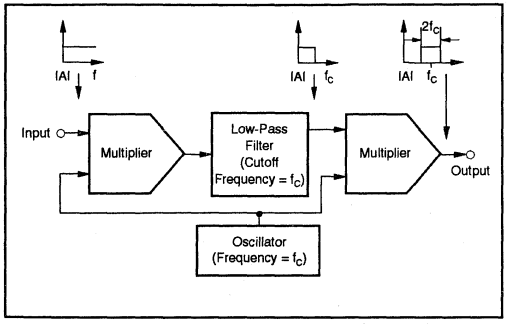


FIGURE 3. In a Frequency-Mixing Circuit, One Multiplier Chip Converts the Input Signal into DC, and Another Translates the DC Signal Back into the Original Frequency. With this technique, a 1kHz low-pass filter and a 5MHz local oscillator create a bandpass filter with an effective Q value of 5000 and a 5MHz center frequency.

The mixer circuit can also be adopted for phase detectors; the designer need only connect a low-pass filter to the multiplier chip's output (Figure 4). The configuration follows the principle that the product of two signals of equal frequency contains a DC component, and that component is proportional to the cosine of the angle between the signals.

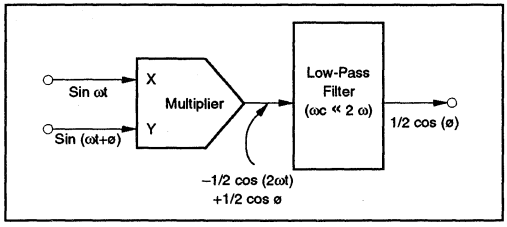


FIGURE 4. The Multiplier Chip Works In A Phase Detector. When two signals of equal frequency are multiplied, the operation produces a DC component proportional to the cosine of the angle between them.

COMPARING DOUBLE-BALANCED MIXERS

Specification	Typical Double-Balanced Diode Mixer	Multiplier Chip	
		DC to 0.5MHz	0.5 to 10MHz
Carrier Feedthrough	25dB	60dB	40dB
Isolation: RF Input to Local Oscillator	40dB	60dB	40dB
Local Oscillator to Mixer	30dB	60dB	40dB
RF Input to Mixer	25dB	60dB	35dB
Third-Order Intermodulation Intercept	1Vrms	50Vrms	2Vrms
Frequency Range	Several kHz to several GHz(1)	DC to 10MHz	DC to 10MHz

NOTE: (1) The frequency range for any one mixer is usually about three decades.

STRIKE UP THE BANDWIDTH

The limited bandwidth of transconductance multipliers is customarily attributed to the output amplifier. Though the bandwidth of the MPY634 multiplier chip can be kept to 50MHz by the core transistors, the output amplifier slashes that figure to 1MHz. The drop is caused by interaction between the core's output resistance and the large Miller capacitance at the amplifier's input, creating a pole at about 1MHz.

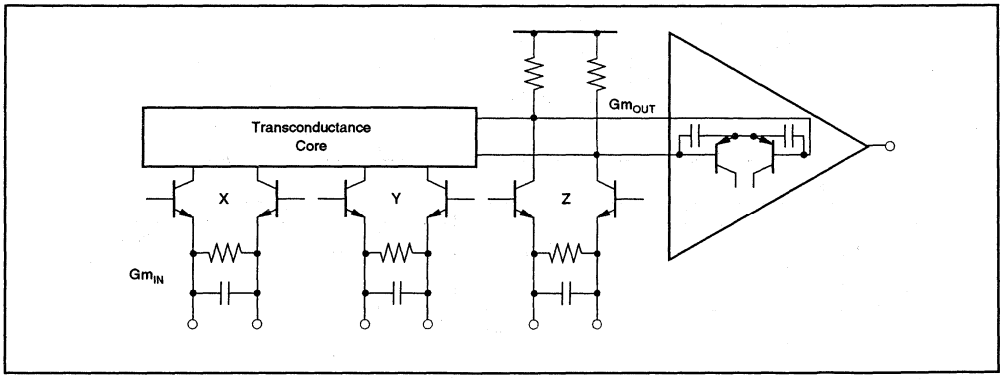
Designers have usually compensated for that interaction by making the output amplifier's –3dB cutoff frequency occur at or before the pole. However, the new chip shifts out that pole in frequency, so that the gain can be sustained far beyond 1MHz. Keeping the gain constant, however, mandates an unchanging ratio of transconductances in the output and input amplifier stages. To keep the ratio constant over a wide band, the input stage's transconductance, Gm_{IN}, must decrease at the same rate that the output transconductance, Gm_{OUT}, does for increasing frequency.

The gain of each input amplifier is the ratio of its load impedance to the transconductance of the input amplifier stage (see the figure). Also, the overall transconductance of the output stage is the output resistance of the core plus the input capacitance and transconductance of the output amplifier. This lumped value looks like a direct load to voltage-to-current converter Z and to the core. Since the core is transparent to converters X and Y, they see Gm_{OUT} as the direct load. Moreover, because Gm_{OUT} represents the load impedance for all the converters, the wideband gain is Gm_{OUT}/Gm_{IN}.

For Gm_{IN}/Gm_{IN} to remain constant over a broad frequency range, the RC time constants of both transconductances must be within 100% of each other. Fortunately, with worst-case process and temperature variations, the match between the RC time constants can be held to within 20%.

In this multiplier chip, a reactive element of the input stage keeps the transconductance ratio constant. The element, a small nitride capacitor, parallels the normally high resistance Gm_{IN}. In fact, this purely resistive transconductance causes Gm_{OUT} to limit the bandwidth in the first place.

The resistive portions comprise thin-film resistors that can be matched to within 1%.The capacitive portion of Gm_{OUT} depends mainly on the quiescent current of the output amplifier's differential inputs. That current is laser-trimmed to a known value. Consequently, only the absolute tolerance of the added nitride capacitor determines the match between the capacitive portions of Gm_{OUT} and Gm_{IN}.



The substance of this application note appeared in article form in the January 9, 1986 issue of *Electronic Design*.

For Immediate Assistance, Contact Your Local Salesperson

BURR-BROWN® **APPLICATION BULLETIN**

Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

DIGITALLY PROGRAMMABLE, TIME-CONTINUOUS ACTIVE FILTER

by Johnnie Molina, (602) 746-7592

Programmable active filters have increased in popularity over the past decade. With the advent of switched capacitor topologies, filter parameters such as the natural frequency and filter Q can be changed simply by varying the clock frequency. But switched capacitor filters are sampled data systems and are subject to anomalies such as clock feedthrough noise and aliasing errors.

The circuit in Figure 1 shows how an analog, digitally programmable filter can be built using a UAF42. This monolithic, state-variable active filter chip provides a two pole filter building block with low sensitivity to external component variations. It eliminates aliasing errors and clock feedthrough noise common to switched capacitor filters. Lowpass, highpass, bandpass and notch (band reject) outputs are available simultaneously.

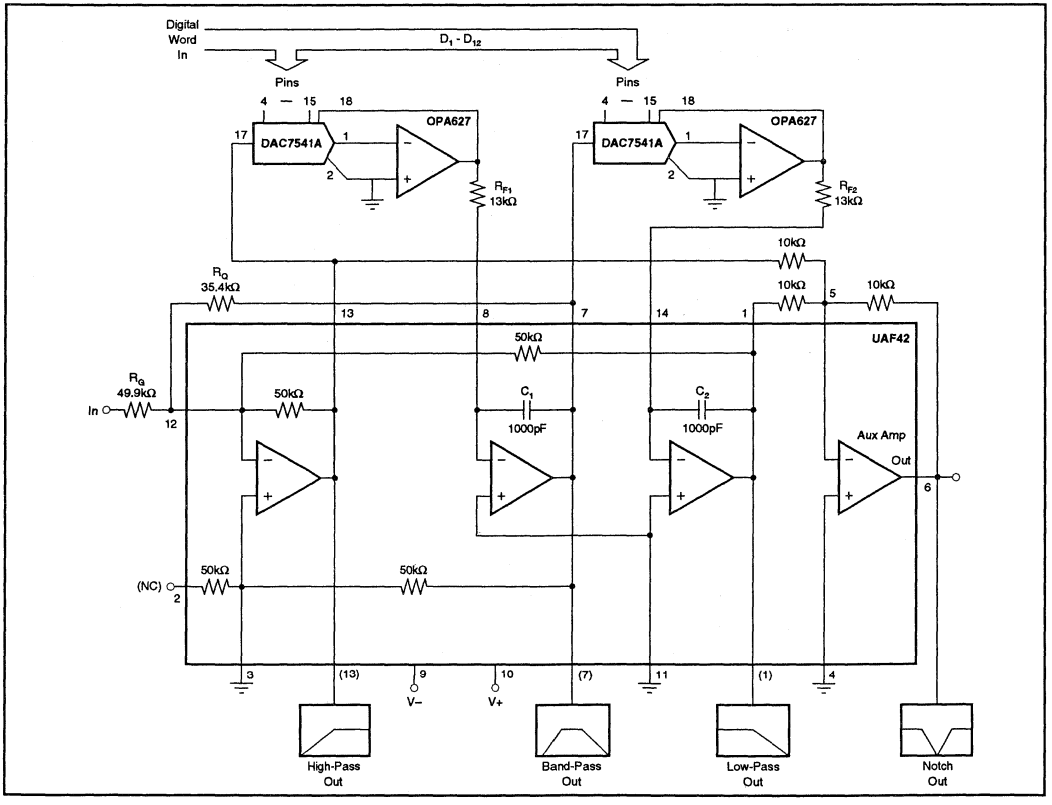


FIGURE 1. Digitally Programmable Analog Filter.

The circuit uses the UAF42 state-variable filter IC, two op amps, a few resistors and two common MDACs. Capacitors aren't required because the UAF42 has on chip 1000pF, 0.5% precision capacitors. The MDACs function as voltage attenuators which influence the unity-gain bandwidth of the integrators on board the UAF42. The filter's natural frequency, f_O, is described by the following relationships:

$$f_O = DAC_{GAIN} \bullet f_{O_{MAX}} \quad (1)$$

Where:

$$DAC_{GAIN} = \frac{X}{2^n}$$

$$f_{O_{MAX}} = \frac{1}{2 \bullet \pi \bullet 10^{-9} \bullet R_F} \qquad R_F = R_{F1} = R_{F2}$$

and,

X = digital word at DAC inputs $D_1 - D_{12}$

n = number DAC bits

BUILD A NOTCH FILTER

For example, to program a 60Hz notch filter with the circuit shown in Figure 1, the digital word to the MDAC is given using Equation 1,

$$X = 6.28 \bullet 10^{-9} \bullet R_F \bullet f_O \bullet 2^n$$

Given that,

$$f_O = 60 \quad R_F = 13k\Omega \quad n = 12$$

then,

$$X = 20.1$$

The 12-bit digital word to the DAC should be 20 or 000000010100. The rounding error introduced is 0.3% (f_{NOTCH} = 59.8Hz). Note that the natural frequency, f_O, is equal to f_{NOTCH}.

Figure 2 shows the response seen at the band reject or "Notch Out" node.

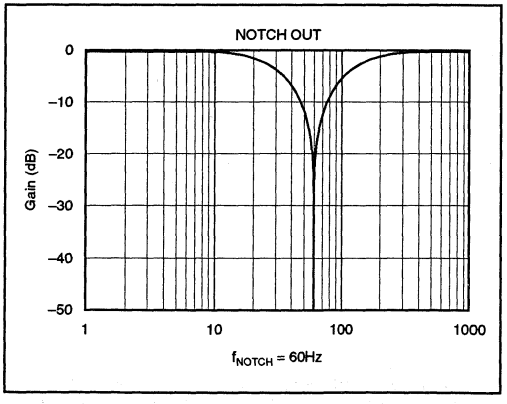


FIGURE 2. 60Hz Notch Response.

The highpass, bandpass and lowpass outputs yield the responses shown in Figure 3.

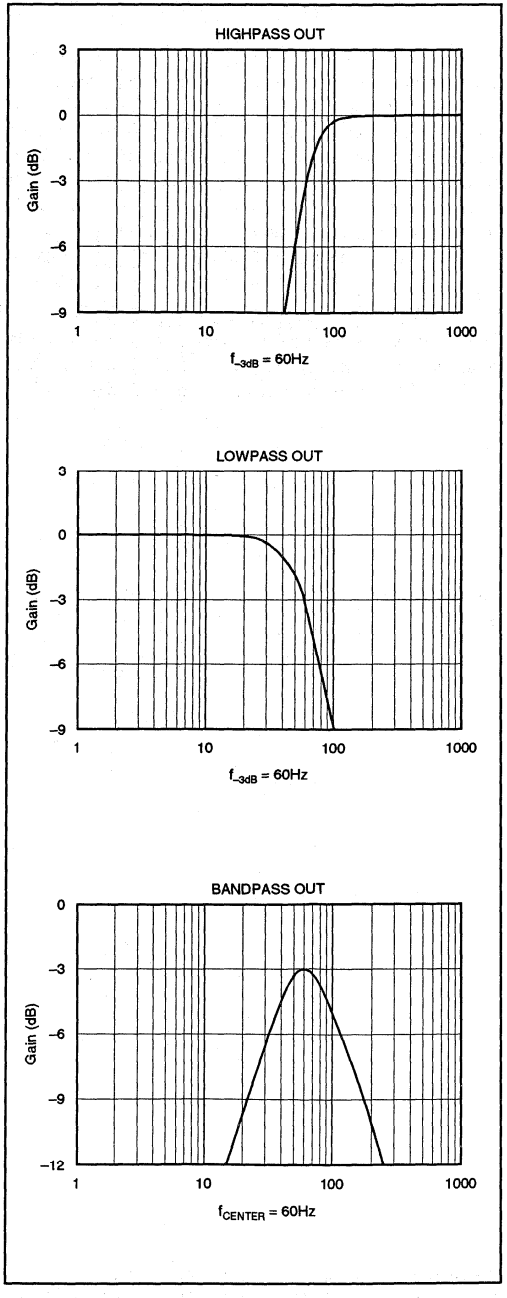


FIGURE 3. Highpass, Lowpass and Bandpass f_o = 60Hz Response.

The filter in Figure 1 is set for a Q of 0.707. This can be adjusted using Equation 2 where,

$$R_Q = 50k\Omega \bullet Q \qquad (2)$$

Setting the filter to a Q of 0.707 produces second-order Butterworth responses. The Q is not affected by the natural frequency programmed by the DACs. Note that for Butterworth filters, the natural frequency is also the –3dB (half power point) for lowpass and highpass responses. It also is the center frequency for bandpass filters and the notch frequency for band reject responses. The passband gain is unity for all response types except the bandpass. For the bandpass output, the gain at f_{CENTER} is equal to the filter Q.

LIMITATIONS

The maximum f_0 in Figure 1 is set for 12.25kHz. This can be adjusted using Equation 1. Set the DAC gain term equal to $(2^n - 1)/2^n$, f_0 = desired maximum natural frequency and solve for RF.

For example, to extend the maximum f_0 to 20kHz,

$$RF = \frac{\frac{4095}{4096}}{2 \bullet \pi \bullet 10^{-9} \bullet 20kHz} = 7.96k\Omega$$

The maximum natural frequency obtainable for the UAF42 is 100kHz.

f_0 accuracy can decrease as the DAC gain decreases in an attempt to program low natural frequencies. For example, for a 12-bit DAC and maximum f_0 set to 20kHz, the resolution giving one LSB change is,

$$\text{Resolution} = \frac{1}{2^{12}} \bullet f_{O_{MAX}} = \frac{1}{4096} \bullet 20kHz = 4.9Hz$$

When trying to program low natural frequencies like 12Hz, the digital word to the DAC would be 2.

So,

$$f_O = \frac{2}{4096} \bullet f_{O_{MAX}} = \frac{2}{4096} \bullet 20kHz = 9.8Hz$$

This is an 18% error. Resolution can be increased by reducing f_{OMAX} or using a higher order DAC. RF resistor tolerance should be kept below 1% to maintain f_0 error to within ±1%.

The OPA627 op amps are chosen for their low offset voltage, low noise, low input bias current (FET input), and high unity gain bandwidth (GBW = 16MHz) to maintain stability.

BURR-BROWN® APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

THERMAL AND ELECTRICAL PROPERTIES OF SELECTED PACKAGING MATERIALS

	MATERIAL	THERMAL CONDUCTIVITY (W/in-°C) NOM	LOW	HIGH	THERMAL EXPANSION (10^{-6}/°C) NOM	LOW	HIGH	TCR (10^{-6}/°C)	RESISTIVITY AT 20°C (μΩ-cm)
ELEMENTS	ALUMINUM	6.02	5.63	6.38	23.9	19.4	25	4290	2.66
	ANTIMONY	0.620	0.481	0.648(β)		8.46	10.8		41.7
	ARSENIC	1.28	1.08(α)	1.37(β)	4.7				33.3
	BARIUM	0.468			18				50.0
	BERYLLIUM	5.10	4.04	5.54(β)	12			25000	5.9
	BISMUTH	0.201(k)	0.134(a)	0.233(b)	13				106.8
	BORON	0.696	0.478(α)	0.808(β)	8.3				1.8×10^{12}(m)
	CADMIUM	2.46(k)	2.11(g)	2.62(d)	29.9			4200	6.83
	CALCIUM	5.10	3.20	5.23	22			4160	3.43
	CARBON	3.70(c)	0.0404(j)	58.9(z)		0.54	4.32		1375(l)
	CESIUM	0.912			97				20.0
	CHROMIUM(k)	2.38			6.1			3000	13.0
	COBALT(k)	2.54			12			6040	6.24
	COPPER	10.2			17			6800	1.673
	GALLIUM	1.04(e)	0.404(g)	2.24(f)	18				56.8
	GERMANIUM	1.53	1.18(α)	1.69(β)	5.9				10^2 - 10^7(t)
	GOLD (10.2 oz. troy/in³)	8.08			14.2			4000	2.19
	HAFNIUM	0.584	0.569(α)	0.592(β)	5.9			3800	32.4
	INDIUM(k)	2.08	1.94(α)	2.12(β)	32				8.37
	IRIDIUM	3.73			6.8			3925	5.3
	IRON	2.04	1.85(h)	2.20(β)	11.7			6510	9.71
	LEAD	0.897	0.874(α)	0.904(β)	29.3			3360	20.65
	MAGNESIUM(k)	3.96			25			16500	4.46
	MANGANESE	0.198			22				185
	MOLYBDENUM	3.50			5.4				5.17
	NICKEL	2.31	2.10(α)	2.39(β)	13			6900	6.84
	NIOBIUM	1.36			7.1				12.5
	OSMIUM(k)	1.55			4.7			4200	9.5
	PALLADIUM	1.82			11.9			3770	10.8
	PHOSPHORUS		.0064(j)	.307(k)	126				10^{17}
	PLATINUM	1.82			8.8			3927	9.83
	RHENIUMk	1.22			6.7			3950	19.3
	RHODIUM	3.81			8.3			4200	4.51
	RUBIDIUM	1.48			90				12.5
	RUTHENIUM	2.97			9.6				7.6(l)
	SELENIUM	0.033(q)	0.013(j)	0.115(q)	38				12(AC)
	SILICON	3.78	2.1	4.27(β)	3.5[111](AB)	2.9	7.4		10^2 to 10^9(t)
	SILVER	10.9			19.6			4100	1.59
	STRONTIUM	0.899	0.826(α)	0.924(β)					23.0
	SULFUR(k)	0.0069	0.0039(α)	0.0073(β)	65				2×10^{23}(m)

NOTES: Values at 20°C unless otherwise specified. (α) At 100°C. (β) At 0°C. (a) ∥ to triangle axis. (b) ⊥ to triangle axis. (c) Average value; graphite varies from 2.0 to 5.6 depending on type and orientation. Pyrolytic graphite is 0.16 and 50 ⊥ and ∥ to layer planes. (d) Crystalline, ⊥ to c-axis; polycrystalline = 0.006W/in-°C. (e) ∥ to a-axis. (f) ∥ to b-axis. (g) ∥ to c-axis. (h) Armco iron. (i) White phosphorous. (j) Amorphous. (k) Polycrystalline. (l) Resistivity at 0°C. (m) Intrinsic value, actual value sensitive to purity. (t) With 10^{21}/cm³ to 10^{14}/cm³ impurity concentration. (z) Type IIa diamond. (AB) Measured by J. Naylor. (AC) Crystalline, amorphous ≈ 10^6μΩ-cm.

THERMAL AND ELECTRICAL PROPERTIES OF SELECTED PACKAGING MATERIALS (CONT)

	MATERIAL	THERMAL CONDUCTIVITY (W/in-°C)			THERMAL EXPANSION (10^{-6}/°C)			TCR [10^{-6}/°C]	RESISTIVITY AT 20°C [μΩ-cm]
		NOM	LOW	HIGH	NOM	LOW	HIGH		
ELEMENTS	TANTALUM	1.46			6.5			3830	12.4
	TELLURIUM	0.150			17				2×10^5
	TIN	1.70[k]	1.31[g]	1.89[d]	23	20	25	4700	11.5
	TITANIUM[k]	0.556	0.526[α]	0.569[β]	8.5				47.8
	TUNGSTEN	4.39	4.14	4.50	4.3	4.2	4.5	5240	5.6
	VANADIUM	0.780			7.7				24.8-26.0
	ZINC[k]	2.95				17	40	4190	5.8
	ZIRCONIUM	0.576	0.554	0.589	5.6			4400	41.0
ORGANIC	EPOXIES		0.0042	0.035		11.0	60		10^{21}[m]
	GLASS-EPOXY (PC-G10)	0.08			(n)	$10^{(n)}$	$15^{(n)}$		10^{21}[m]
	KAPTON	0.0039				34	40		10^{24}[m]
	NYLON		0.0054	0.0085		82.8	128		10^{20}[m]
	PARYLENE	0.0032				35	69		10^{22}[m]
	RTV	0.0053	0.004	0.008	930				3×10^{15}[m]
	TEFLON		0.0056	0.0296	83	50	162		10^{24}[m]
	MYLAR		0.0045	0.0073		60	95		10^{21}[m]
MISCELLANEOUS	AIR	0.00066							
	Al_2O_3	0.53[v]	0.42[w]	0.85[x]	6.7[v]	6.5	7.3		5×10^{21}[m]
	BRASS[p]	2.95				18	21	2000	6.4
	BeO	6.0	5.5	7.1	8.0	6.5	8.7		10^{22}[m]
	EUTECTIC (Au-Si) MP 370°C	5.5			13.7				2.53
	EUTECTIC (Au-Sn) MP 280°C	6.4			16				2.6
	EUTECTIC (Au-Ge) MP 356°C	6.7			12.6				2.6
	FERRITE	0.085		0.159		8	12		127×10^6
	GLASS[y]		0.010	0.037		0.55	12.4		10^{24}[m]
	KOVAR	0.425			5.5				49.0
	KOVAR-42	0.28			4.9				78
	MANGANIN	0.564	0.523	0.635	18.7			±15	44
	MICA	0.011	0.009	0.017		32.4	48.6		10^{21}[m]
	QUARTZ (SiO_2)	0.035	0.19[β][d]	0.37[β][q]	0.55				10^{24}[m]
	SAPPHIRE	0.821	0.691	1.0	6.67[q]	5.0[r]	8.33[s]		10^{25}[m]
	SOLDER (60/40)	1.0			23				13.5
	STEEL (1008)	1.2			12			6510	11
	STEEL, STAINLESS	0.35[303]	0.30[310]	0.94[501]	18[304]			170[AA]	112[AA]

NOTES: Values at 20°C unless otherwise specified. (α) At 100°C. (β) At 0°C. (d) ⊥ to c-axis. (e) ∥ to a-axis. (f) ∥ to b-axis. (g) ∥ to c-axis. (k) Polycrystalline. (m) Intrinsic value; actual value sensitive to purity. (n) 40-300 for vertical axis. (p) Yellow brass. (q) ∥ to c-axis at 50°C. (r) ⊥ to c-axis at 50°C. (s) ∥ to c-axis at 500°C. (v) 96%. (w) 90%. (x) 99.5%. (y) See quartz. (AA) Nichrome 60% Ni, 25% Fe, 15% Cr.

THERMAL CONDUCTIVITY (K) CONVERSIONS

	CONVERSION UNIT					
ORIGINAL UNIT	cal / s-cm-°C	watt / cm-°C	watt / in-°C	BTU / hr-ft-°F	kg-cal / hr-m-°C	watt / m-°C
1 cal/s-cm-°C	1.0	4.186	10.63	241.9	360.0	418.6
1 watt/cm-°C	0.2389	1.0	2.540	57.8	86.00	100
1 watt/in-°C	0.09405	0.3937	1.0	22.75	33.86	39.37
1 BTU/hr-ft-°F	4.134(10^{-3})	0.01730	0.0440	1.0	1.488	1.730
1 kg-cal/hr-m-°C	2.778(10^{-3})	0.01163	0.0295	0.672	1.0	1.163
1 watt/m-°C	0.002389	0.01	0.0254	0.578	0.8600	1.0

EXAMPLE
232 (BTU/hr-ft-°F) x 0.0440 = 10.2 (watt/°C-in)

FORMULAE

$$°C/W = \frac{\text{Length (in)}}{\text{Area (in}^2\text{)} \bullet K \text{ (W/in-°C)}}$$

Or, Call Customer Service at 1-800-548-6132 (USA Only)

BURR-BROWN® APPLICATION BULLETIN

Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

MFB LOW-PASS FILTER DESIGN PROGRAM

By Bruce Trump and R. Mark Stitt (602) 746-7445

Although low-pass filters are vital in modern electronics, their design and verification can be tedious and time consuming. The Burr-Brown FilterPro™ program, FILTER2, makes it easy to design low-pass active filters. The program is intended to aid in the design of low-pass filters implemented with the Multiple Feedback (MFB) topology. Because there are instances where the Sallen-Key filter topology is a better choice, the program also supports Sallen-Key low-pass filter design.

An ideal low-pass filter would completely eliminate signals above the cutoff frequency, and perfectly pass signals below cutoff (in the pass-band). In real filters, various trade-offs are made in an attempt to approximate the ideal. Some filter types are optimized for gain flatness in the pass-band, some trade-off gain variation (ripple) in the pass-band for steeper roll-off, still others trade-off both flatness and rate of roll-off in favor of pulse-response fidelity. FILTER2 supports the three most commonly used all-pole filter types: Butterworth, Chebyshev, and Bessel.

Butterworth (maximally flat magnitude). This filter has the flattest possible pass-band magnitude response. Attenuation is –3dB at the design cutoff frequency. Attenuation above the cutoff frequency is a moderately steep –20dB/decade/pole. The pulse response of the Butterworth filter has moderate overshoot and ringing.

Chebyshev (equal ripple magnitude). (Also transliterated Tschebychev, Tschebyscheff or Tchevysheff.) This filter type has steeper attenuation above the cutoff frequency than Butterworth. This advantage comes at the penalty of amplitude variation (ripple) in the pass-band. Unlike Butterworth and Bessel responses, which have 3dB attenuation at the cutoff frequency, Chebyshev cutoff frequency is defined as the frequency at which the response falls below the ripple band. For even-order filters, all ripple is above the 0dB-gain DC response, so cutoff is at 0dB—see Figure 1A. For odd-order filters, all ripple is below the 0dB-gain DC response, so cutoff is at –(ripple) dB—see Figure 1B. For a given number of poles, a steeper cutoff can be achieved by allowing more pass-band ripple. The Chebyshev has even more ringing in its pulse response than the Butterworth.

Bessel (maximally flat time delay). (Also called Thomson.) Due to its linear phase response, this filter has excellent pulse response (minimal overshoot and ringing). For a given number of poles, its magnitude response is not as flat, nor is its attenuation beyond the –3dB cutoff frequency as steep as the Butterworth. It takes a higher-order Bessel filter to give a magnitude response which approaches that of a given Butterworth filter, but the pulse response fidelity of the Bessel filter may make the added complexity worthwhile.

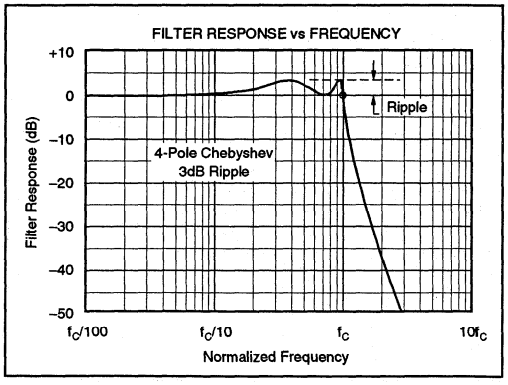


FIGURE 1A. Response vs Frequency of Even-Order (4-pole), 3dB Ripple Chebyshev Filter Showing Cutoff at 0dB.

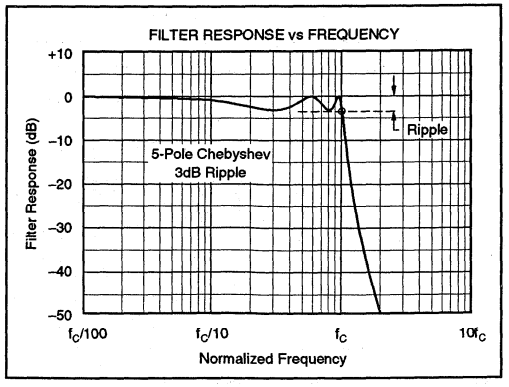


FIGURE 1B. Response vs Frequency of Odd-Order (5-pole), 3dB Ripple Chebyshev Filter Showing Cutoff at –3dB.

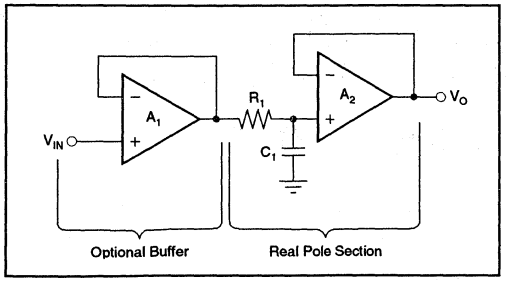


FIGURE 2. Real Pole Section (Unity-Gain, First-Order Butterworth; $f_{-3dB} = 1/2 \cdot \pi \cdot R_1 \cdot C_1$).

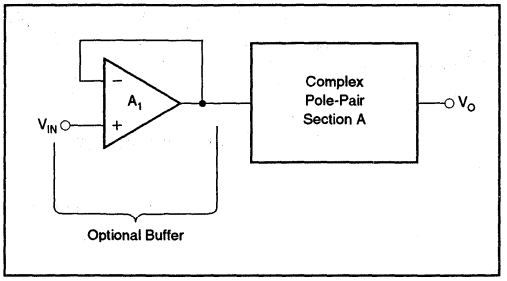


FIGURE 3. Second-Order Low-Pass Filter.

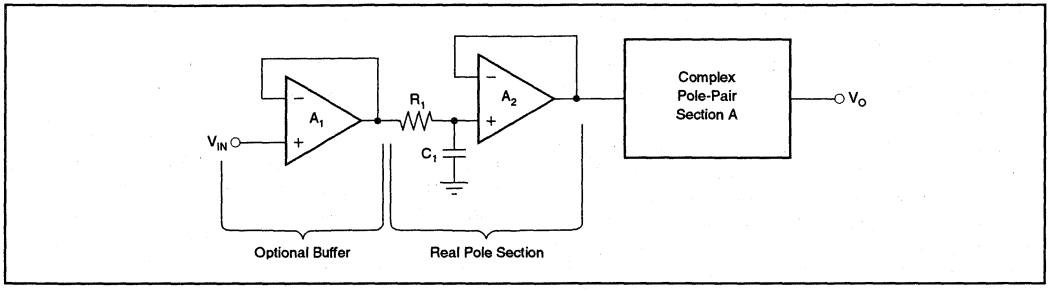


FIGURE 4. Third-Order Low-Pass Filter.

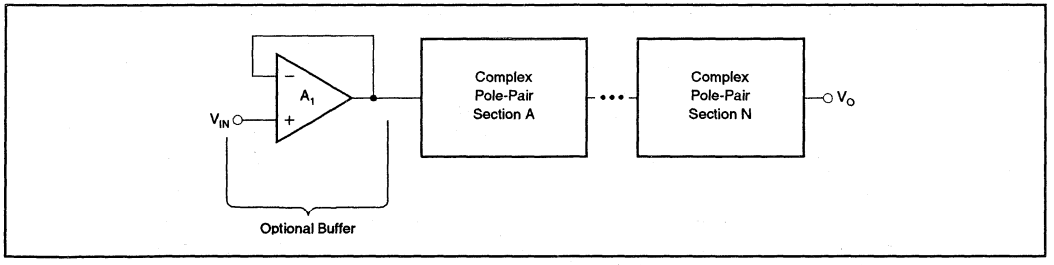


FIGURE 5. Even-Order Low-Pass Filter Using Cascaded Complex Pole-Pair Sections.

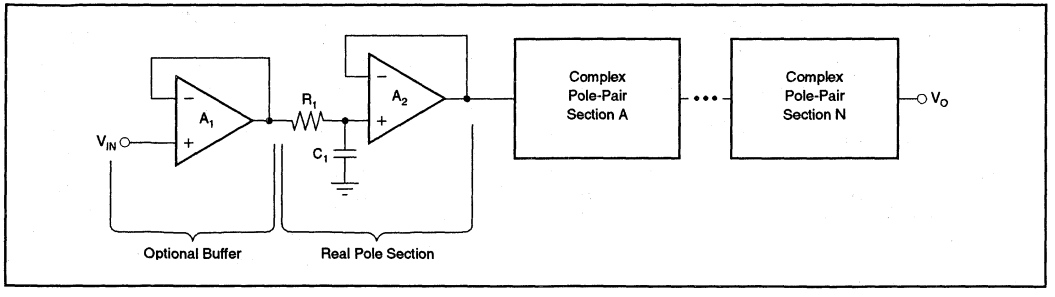


FIGURE 6. Odd-Order Low-Pass Filter Using Cascaded Complex Pole-Pair Sections Plus One Real-Pole Section.

SUMMARY

Butterworth

Advantages	Maximally flat magnitude response in the pass-band. Good all-around performance. Pulse response better than Chebyshev. Rate of attenuation better than Bessel.
Disadvantages	Some overshoot and ringing in step response.

Chebyshev

Advantages	Better attenuation beyond the pass-band than Butterworth.
Disadvantages	Ripple in pass-band. Considerable ringing in step response.

Bessel

Advantages	Best step response—very little overshoot or ringing.
Disadvantages	Slower rate of attenuation beyond the pass-band than Butterworth.

CIRCUIT IMPLEMENTATION

Even-order filters designed with this program consist of cascaded sections of complex pole-pairs. Odd-order filters contain an additional real-pole section. Figures 2 through 6 show the recommended cascading arrangement. The program automatically places lower Q stages ahead of higher Q stages to prevent op amp output saturation due to gain peaking. The program can be used to design filters up to 8th order.

FILTER ORDER	FIGURE
1 pole	Figure 2
2 poles	Figure 3
3 poles	Figure 4
4 or more poles (even order)	Figure 5
5 or more poles (odd order)	Figure 6

TABLE I. Filter Circuit vs Filter Order.

COMPLEX POLE-PAIR CIRCUIT

The choice of a complex pole-pair circuit depends on performance requirements. FILTER2 supports the two most commonly used op amp pole-pair circuit topologies:

- Multiple Feedback (MFB)—shown in Figure 7.
- Sallen-Key—shown in Figures 8 and 9.

The MFB topology (sometimes called Infinite Gain or Rauch) is often preferred due to assured low sensitivity to component variations—see sensitivity section. There are instances, however, where the Sallen-Key topology is a better choice.

As a rule of thumb, the Sallen-Key topology is better if:

1) Gain accuracy is important, *AND*
2) A unity-gain filter is used, *AND*
3) Pole-pair Q is low (e.g. Q < 3)

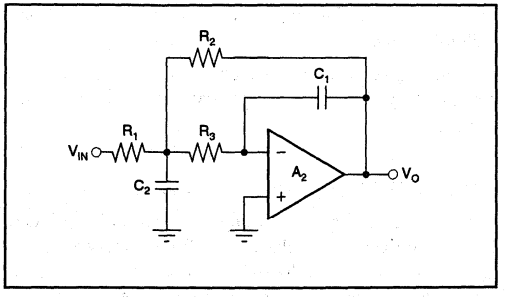


FIGURE 7. MFB Complex Pole-Pair Section. (Gain = $-R_2/R_1$)

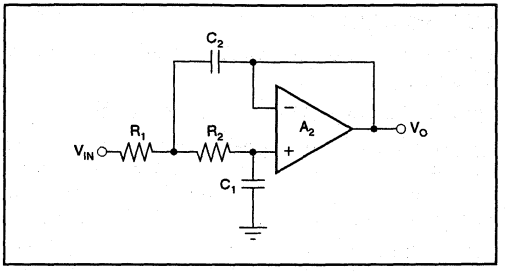


FIGURE 8. Unity-Gain Sallen-Key Complex Pole-Pair Section. (Gain = 1)

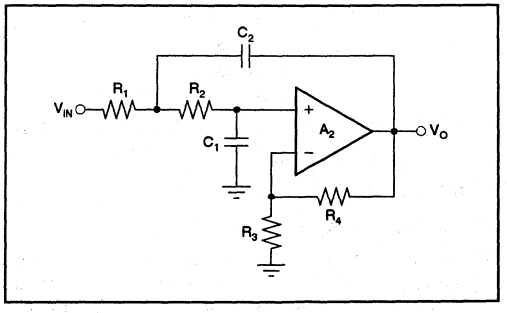


FIGURE 9. Sallen-Key Complex Pole-Pair Section. (Gain = $1 + R_4/R_3$)

At unity-gain, the Sallen-Key topology inherently has excellent gain accuracy. This is because the op amp is used as a unity-gain buffer. With the MFB topology, gain is determined by the R_2/R_1 resistor ratio. The unity-gain Sallen-Key topology also requires fewer components—two resistors vs three for MFB.

The Sallen-Key topology may also be preferable for high-Q high frequency filter sections. In these sections the value required for C_1 in a MFB design can be quite low for reasonable resistor values. Low capacitor values can result in significant errors due to parasitic capacitances.

The best filter design may be a combination of MFB and Sallen-Key sections.

Use the appropriate circuits along with component values generated by the FILTER2 program to build your filter design.

USING THE FILTERPRO™ PROGRAM

With each data entry, the program automatically calculates filter performance and values for all filter components. This allows you to use a "what if" spreadsheet-type design approach. For example, you can quickly determine, by trial and error, how many poles are needed for a given roll-off.

GETTING STARTED

The first time you use the program, you may want to follow these steps.

Type **FILTER2 <ENTER>** to start the program.

At this point, you have already designed a 3-pole, 1kHz Butterworth filter. Component values are shown on the display screen. For a different filter design, use the arrow keys to move the cursor to the menu selection desired.

Start at the top of the menu and work your way down. On-screen prompts, to the left of the menu selections, will guide you in program use. Refer to this bulletin for more detail, if needed.

1) Choose pole-pair **Circuit**: MFB or Sallen-Key
2) Select **Filter type**: Butterworth
   Chebyshev
   Bessel
3) For Chebyshev filter type, enter **Ripple**: >0dB to 4dB
4) Enter **Number of poles**: 1 to 8
5) Enter filter **Cutoff frequency**: (Hz)

The following steps are optional:

6) If you want to view the gain/phase response of the current filter design at a particular frequency, enter the frequency of interest on the **Response @ fx** line. The gain/phase information can be viewed on the **fn, Q, Response** display window—see step 11.
7) If you want to change the resistor scaling, enter a value on the **Scale Resistors** line.
8) If you want to change the gain of a section, press **<ENTER>** on the **Gain Entry** line. Default value for gain is 1.0V/V in each section.
9) If you want to enter your own capacitor values, press **<ENTER>** on the **Capacitor Menu** line.
10) If you want to design with standard 1% resistors instead of exact resistors, press **<ENTER>** on the **Resistors** line.
11) To change the display screen press **<ENTER>** on the **Display** line. Available display screens are: Component values; fn, Q, Response; Sensitivities.

TO RETURN TO DOS

To exit the program and return to DOS, press **<F1>**.

USING THE PLOT FEATURE

A Plot feature allows you to view graphical results of filter gain and phase vs frequency. This feature is useful for comparing filter types.

To view a plot of the current filter design, press **<F2>**.

GRAPHIC DISPLAY COMMANDS

While viewing the graphic display, several commands can be used to compare filter responses:

S—Saves the plot of the current design for future recall.

R—Recalls the Saved plot and plots it along with the current design.

P—Recalls the Previous plot of the last design plotted from the main program (by pressing **<F2>**) and plots it along with the current design. You can recall the Previous design and the Saved design to plot all three together.

C—Clears the display and replots only the current design.

GRAPHIC DISPLAY CURSOR CONTROL

While viewing the graphics display you can also use the left/right *arrow* keys to move a cursor and view gain and phase for plotted filter responses. The gain/phase of the current design is always displayed. In addition, the gain/phase of the Recalled or Previous design can be viewed by pressing **R** or **P**.

TO PRINT RESULTS

To print results press **<F3>**. All three display screens will automatically be printed.

SENSITIVITY

Sensitivity is the measure of the vulnerability of a filter's performance to changes in component values. The important filter parameters to consider are natural frequency (f_n) and Q.

f_n SENSITIVITY FOR BOTH MFB AND SALLEN-KEY

Sensitivity of f_n to resistor, capacitor, and amplifier gain variations is always low for both the Sallen-Key and MFB filter topologies.

$S_R^f = S_C^f = \pm 0.5\%/\%$

$S_K^f = 0$

Where:
S_R^f, S_C^f, S_K^f = Sensitivity of f_n to resistor, capacitor, and gain variations (%/%)

Q SENSITIVITY

For the MFB topology, sensitivities to Q are also always low, but sensitivities for the Sallen-Key topology can be quite high—exceeding $2 \cdot K \cdot Q^2$. At unity gain, the Sallen-Key Q sensitivity to resistor and capacitor variations will always be low. Unfortunately, however, the sensitivity of the unity-gain Sallen-Key pole-pair to op amp gain can be high.

Q Sensitivity for MFB Pole-Pair

$S_C^Q = \pm 0.5\%/\%$

$$S_R^Q = \pm \frac{R_2 - R_3 - K \cdot R_3}{2(R_2 + R_3 + K \cdot R_3)} \quad \text{(MFB complex pole-pair)}$$

$$S_K^Q = \frac{K \cdot R_3}{R_2 + R_3 + K \cdot R_3} \quad \text{(MFB complex pole-pair)}$$

Notice, by inspection: S_R^Q is always less than $\pm 0.5\%/\%$, and S_K^Q is always less than $1.0\%/\%$.

Q Sensitivity for Gain = 1 Sallen-Key Pole-Pair

$S_C^Q = \pm 0.5\%/\%$

$$S_R^Q = \pm \frac{R_1 - R_2}{2(R_1 + R_2)} \quad \text{(Sallen-Key complex pole-pair)}$$

So, S_R^Q is always less than $0.5\%/\%$.

$Q^2 < S_K^Q < 2 \cdot Q^2$ (Sallen-Key complex pole-pair)

Where:
S_R^Q, S_C^Q, S_K^Q = Sensitivity of f and Q to resistor, capacitor, and gain variations (%/%)
K = Op amp gain (V/V)
Figure 7 circuit, $K = R_2/R_1$
Figure 8 circuit, $K = 1.0$
Figure 9 circuit, $K = 1 + R_4/R_3$

NOTE: FilterPro™ always selects component values so unity-gain Sallen-Key S_K^Q will be closer to Q^2 than to $2 \cdot Q^2$.

However, FILTER2 will allow you to design Sallen-Key pole-pairs with high sensitivities (high Qs and GAIN >> 1). You must make sure that sensitivities to component variations do not make these designs impractical. A feature in the **Display** menu allows you to view the f_n and Q sensitivity of filter sections to resistor and capacitor variations.

USING THE SENSITIVITY DISPLAY FEATURE

To use the **Sensitivity** display option, move the cursor to the **Display** menu, press **<ENTER>**, move the cursor to the **Sensitivity** selection, and press **<ENTER>** again. The display shows sensitivity of f_n and Q to each component for each filter section. The format is S^f; S^Q.

Rather than displaying the derivative with respect to component variations, the program calculates f_n and Q change for a 1% change in component values. This gives a more realistic sensitivity value for real-world variations.

USING THE SCALE RESISTORS MENU OPTION

The **Scale Resistors** option allows you to scale the computer-selected resistor values to match the application. Move the cursor to the **Scale Resistors** menu selection and enter your *seed* resistor value. The default value of 10kΩ is suggested for most applications.

Higher resistor values, e.g. 100kΩ, can be used with FET-input op amps. At temperatures below about 70°C, DC errors and excess noise due to op amp input bias current will be small. Remember, however, that noise due to the resistors will be increased by $\sqrt{n}$ where n is the resistor increase multiplier.

Lower resistor values, e.g. 500Ω, are a better match for high-frequency filters using the OPA620 or OPA621 op amps.

CAPACITOR VALUES

Compared to resistors, capacitors with tight tolerances are more difficult to obtain and can be much more expensive. The **Capacitor** menu option allows you to enter actual measured capacitor values. In this way, an accurate filter response can be achieved with relatively inexpensive components.

USING THE CAPACITOR MENU OPTION

To use the **Capacitor** menu option, move the cursor to the **Capacitor** menu selection and press **<ENTER>**. Move the cursor to any capacitor and enter your value. Prompts on the left of the screen advise min/max capacitor entry limits. With each capacitor entry, the program will select exact or closest standard 1% resistor values as before.

COMPENSATE FOR OP AMP INPUT CAPACITANCE—SALLEN-KEY ONLY

If the common-mode input capacitance of the op amp used in a Sallen-Key filter section is more than approximatcly $C_1/400$ (0.25% of C_1), it must be considered for accurate filter response. You can use the **Capacitor** menu option to compensate for op amp input capacitance by simply adding the value of the op amp common-mode input capacitance to the actual value of C_1. The program then automatically

recalculates the exact or closest 1% resistor values for accurate filter response. No compensation for op amp input capacitance is required with MFB designs.

CAPACITOR SELECTION

Capacitor selection is very important for a high-performance filter. Capacitor behavior can vary significantly from ideal, introducing series resistance and inductance which limit Q. Also, nonlinearity of capacitance vs voltage causes distortion.

Common ceramic capacitors with high dielectric constants, such as "high-K" types, can cause errors in filter circuits. Recommended capacitor types are: NPO ceramic, silver mica, metallized polycarbonate; and, for temperatures up to 85°C, polypropylene or polystyrene.

OP AMP SELECTION

It is important to choose an op amp that can provide the necessary DC precision, noise, distortion, and speed.

OP AMP BANDWIDTH

In a low-pass filter section, maximum gain peaking is very nearly equal to Q at f_n (the section's natural frequency). So, as a rule of thumb:

For an MFB section: Op amp bandwidth should be at least $100 \cdot \text{GAIN} \cdot f_n$.

High-Q Sallen-Key sections require higher op amp bandwidth.

For a Sallen-Key section: For $Q > 1$, op amp gain-bandwidth should be at least $100 \cdot \text{GAIN} \cdot Q^3 \cdot f_n$.
For $Q \leq 1$, op amp gain-bandwidth should be at least $100 \cdot \text{GAIN} \cdot f_n$.

For a real-pole section: Op amp bandwidth should be at least $50 \cdot f_n$.

Although Q is formally defined only for complex poles, it is convenient to use a Q of 0.5 for calculating the op amp gain required in a real-pole section.

For example, a unity-gain 20kHz 5-pole, 3dB ripple Chebyshev MFB filter with a 2nd pole-pair f_n of 19.35kHz and a Q of 8.82 needs an op amp with unity gain bandwidth of at least 17MHz. On the other hand, a 5-pole Butterworth MFB filter, with a worst case Q of 1.62 needs only a 3.2MHz op amp. The same 5-pole Butterworth filter implemented with a Sallen-Key topology would require a 8.5MHz op amp in the high-Q section.

USING THE f_n AND Q DISPLAY OPTION

To aid in selection of the op amp, a feature in the **Display** menu section allows you to view pole-pair section f_n and Q.

To use this feature move the cursor to the **Display** menu, press **<ENTER>**, move the cursor to the **f_n & Q** selection, and press **<ENTER>** again. The f_n and Q information is also useful when trouble-shooting filters by comparing expected to actual response of individual filter sections.

OP AMP SLEW RATE

For adequate full-power response, the slew rate of the op amp must be greater than $\pi \cdot V_{OP}\text{-p} \cdot$ FILTER BANDWIDTH. For example, a 100kHz filter with 20Vp-p output requires an op amp slew rate of at least 6.3V/µs. Burr-Brown offers an excellent selection of op amps which can be used for high performance active filters. The guide on P-7 lists some good choices.

THE UAF42 UNIVERSAL ACTIVE FILTER

For other filter designs, consider the Burr-Brown UAF42 Universal Active Filter. It can easily be configured for a wide variety of low-pass, high-pass, band-pass, or band-reject (notch) filters. It uses the classical state-variable architecture with an inverting amplifier and two integrators to form a pole-pair. The integrators include on-chip 1000pF, ±0.5% capacitors. This solves one of the most difficult problems in active filter implementation—obtaining tight tolerance, low-loss capacitors at reasonable cost.

Simple design procedures for the UAF42 allow implementation of Butterworth, Chebyshev, Bessel, and other types of filters. An extra FET-input op amp in the UAF42 can be used to form additional stages or special filter types such as Inverse Chebyshev. The UAF42 is available in a standard 14-pin DIP. For more information, request the Burr-Brown Product Data Sheet PDS-1070 and Application Bulletin AB-035.

EXAMPLES OF MEASURED MFB FILTER RESPONSE

Figures 10 and 11 show actual measured magnitude response plots for 5th-order 20kHz Butterworth, 3dB Chebyshev and Bessel filters designed with the program. The op amp used in all filters was the OPA627. As can be seen in Figure 10, the initial roll-off of the Chebyshev filter is fastest and the roll-off of the Bessel filter is the slowest. However, each of the 5th-order filters ultimately rolls off at $-N \cdot 20\text{dB/decade}$, where N is the filter order (–100dB/decade for a 5-pole filter).

The oscilloscope photographs (Figures 12-14) show the step response for each filter. As expected, the Chebyshev filter has the most ringing, while the Bessel has the least. Figure 15 shows distortion plots vs frequency for the three filters.

See Application Bulletin AB-017 for measured Sallen-Key filter performance of the same three designs.

OP AMP SELECTION GUIDE (In Order of Increasing Slew Rate)

T_A = 25°C, V_S = ±15V, specifications typ, unless otherwise noted, min/max specifications are for high-grade model.

OP AMP MODEL	BW typ (MHz)	FPR [1] typ (kHz)	SR typ (V/µs)	V_{OS} max (µV)	V_{OS}/dT max (µV/°C)	NOISE at 10kHz (nV/√Hz)	C_{CM} [3] (pF)
OPA177	0.6	3	0.2	10	±0.1	8	1
OPA27	8	30	1.9	25	±0.6	2.7	1
OPA2107 dual [2]	4.5	280	18	500	±5	8	4
OPA602 [2]	6	500	35	250	±2	12	3
OPA404 quad [2]	6	500	35	1000	±3 typ	12	3
OPA627 [2]	16	875	55	100	±0.8	4.5	7
OPA620 (V_S = ±5V)	300	16MHz(5Vp-p)	250	500	±8 typ	2.3 @ 1MHz	1

NOTES: (1) Unless otherwise noted, FPR is full power response at 20Vp-p as calculated from slew rate. (2) These op amps have FET inputs. (3) Common-mode input capacitance.

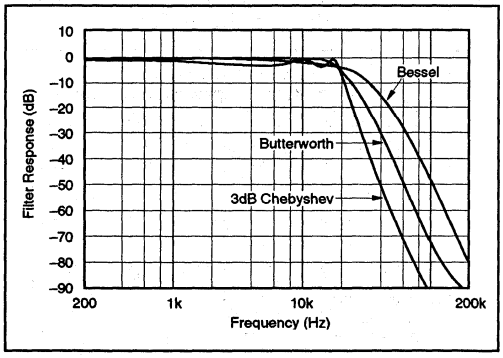


FIGURE 10. Gain vs Frequency for Fifth-Order 20kHz Butterworth, Chebyshev, and Bessel Unity-Gain MFB Low-Pass Filters, Showing Overall Filter Response.

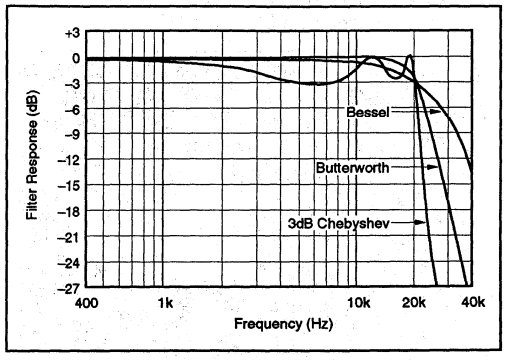


FIGURE 11. Gain vs Frequency for Fifth-Order 20kHz Butterworth, Chebyshev, and Bessel Unity-Gain MFB Low-Pass Filters, Showing Transition-Band Detail.

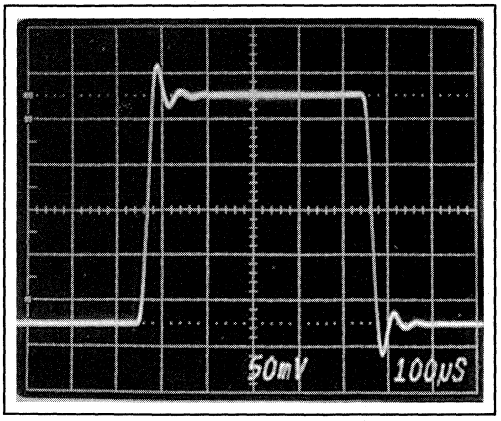


FIGURE 12. Step Response of Fifth-Order 20kHz Butterworth Low-Pass MFB Filter.

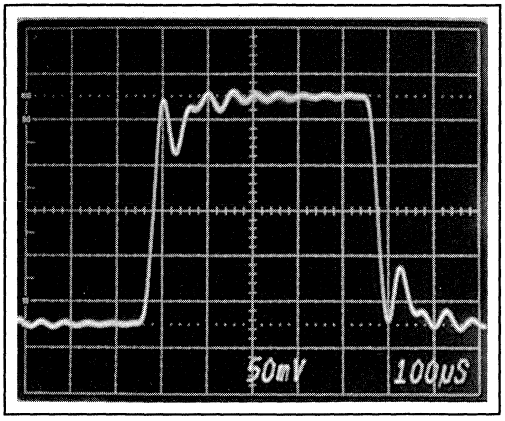


FIGURE 13. Step Response of Fifth-Order 20kHz Chebyshev Low-Pass MFB Filter.

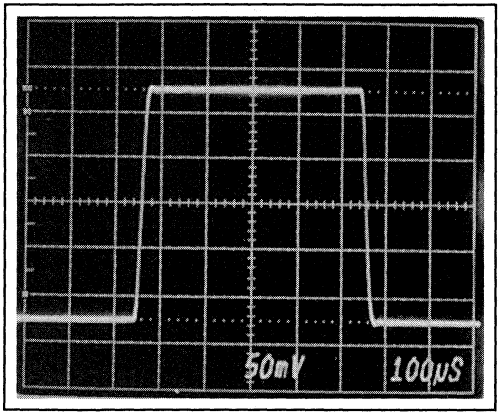


FIGURE 14. Step Response of Fifth-Order 20kHz Bessel Low-Pass MFB Filter.

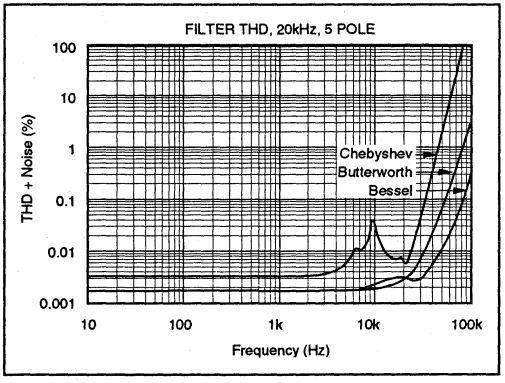


FIGURE 15. Measured Distortion for the Three 20kHz MFB Low-Pass Filters.

BURR-BROWN® APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

SIMPLE FILTER TURNS SQUARE WAVES INTO SINE WAVES

by R. Mark Stitt (602) 746-7445

Many signals are digitally generated or transmitted as square waves. It is often desirable to convert these signals into sine waves. For example, the 350Hz, 440Hz, 480Hz, and 620Hz telephone supervisory tones transmitted over fiber-optics may appear at curb-side as square waves. To be used in telephone equipment it is desirable to convert the square waves into low-distortion sine waves. This can be done with a simple filter.

According to its Fourier series, a 50% duty-cycle square wave consists of odd order harmonic sine waves with the fundamental at the same frequency as the square wave.

Fourier Series for a Square Wave

$$\frac{4k}{\pi}\left(\sin x + \tfrac{1}{3}\sin 3x + \tfrac{1}{5}\sin 5x + \cdots\right)$$

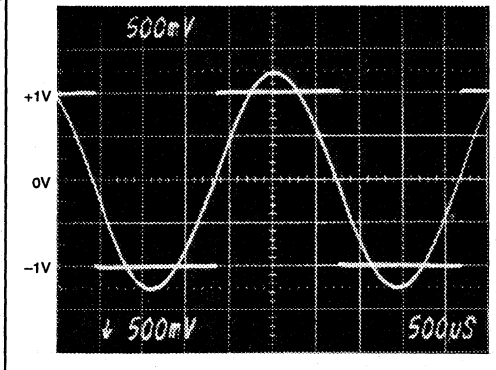
where k = peak amplitude of the square wave

A sine wave with the same frequency as the square wave can be gleaned by filtering out the harmonics above the fundamental. A "tuned-circuit" bandpass filter with a Q of 10 attenuates signals at three times the bandpass frequency by 28.4dB. Since the amplitude of the third harmonic is 1/3 that of the fundamental, the total attenuation of the third harmonic compared to the fundamental is nearly 40dB. The result is a low distortion sine wave as shown in Figure 1A. Notice that although the filter has unity gain, the amplitude of the sine wave output signal is greater than that of the square wave. This is because the fundamental has an amplitude of $4/\pi$ times that of the square wave as shown by the Fourier series. The bandpass filter will also filter out any DC component of the square wave input as shown in Figure 1B.

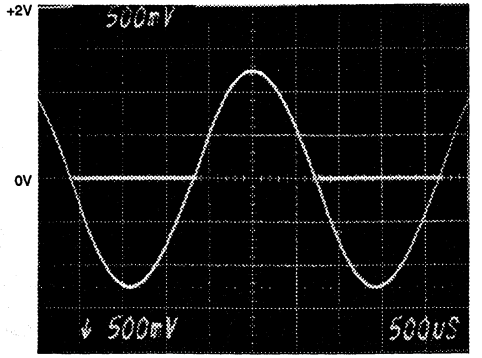
The circuit for a "tuned-circuit" bandpass filter using a Burr-Brown UAF42 universal active filter chip is shown in Figure 2. The UAF42 contains op amps, gain-set resistors, and on-chip precision (0.5%) 1000pF capacitors to form a time continuous filter, free from the anomalies and switching noise associated with switched-capacitor filters. The only external components required are three 1% resistors to set center frequency and Q. In this example, resistors are selected to produce a "tuned-circuit" bandpass filter simulating a tuned-circuit response with 350Hz center frequency and Q = 10. A computer-aided design program, FilterPro, is available free of charge from Burr-Brown to make it easy to design all kinds of active filters using the UAF42.

To design a "tuned-circuit" bandpass filter with Q = 10: load FilterPro FILTER42, select Bandpass filter response, select Order n = 2, set the desired center frequency (f_{CENTER}), and set the bandwidth to 1/10 the center frequency. You can plot the filter response and print out component values.

A fourth, auxiliary, op amp in the UAF42 is available for use in other circuitry. If the auxiliary op amp is not used, connect it as a unity-gain follower with the input to ground (connect –IN to V_{OUT} and +IN to ground).



1a. A square wave passed through a simple "tuned-circuit" bandpass filter produces a low distortion sine wave.

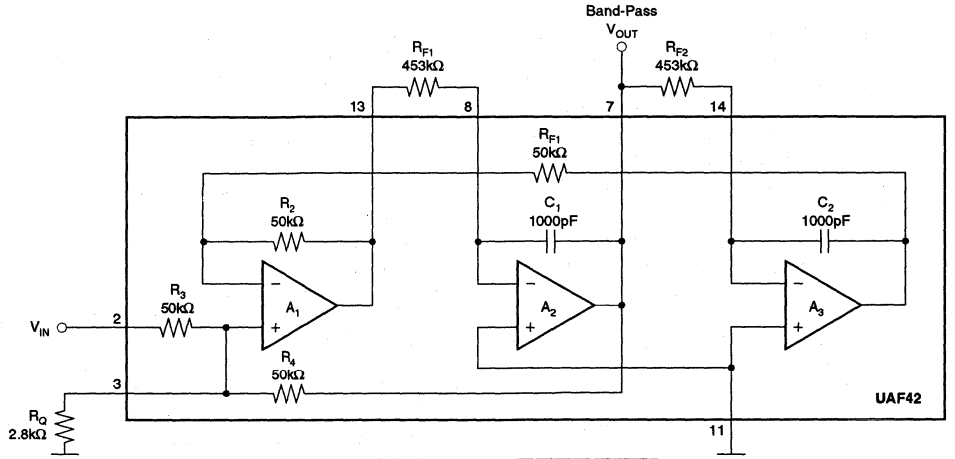


1b. DC components of a square wave passed through bandpass filter are eliminated to produce a low distortion sine wave.

FIGURE 1. Low Distortion Sine Wave.

Mismatches between the frequency of the input square wave and the center frequency of the bandpass filter will affect the sine wave output. Figure 3 shows measured sine wave output total harmonic distortion (THD) and gain variation for mismatches from 0 to ±5%. A typical mismatch of 1% gives less than 1.5% THD and less than 2% gain deviation.

Variations of the square-wave duty cycle from 50% will also increase distortion due to second-order harmonic content. In applications with a pulse train or other non-50% duty cycle square wave, it may be desirable to place an inexpensive divide by two digital flip-flop ahead of the filter to assure a 50% duty cycle square-wave input.



CENTER FREQUENCY (Hz)	R_{F1}, R_{F2} (Ω)	R_Q (Ω)
350	453k	2.8k
440	365k	2.8k
480	332k	2.8k
620	255k	2.8k

Component values for selected Q = 10 "tuned-circuit" bandpass filters.

FIGURE 2. A Simple 350kHz, Q = 10, "Tuned-Circuit" Bandpass Filter Built with the UAF42 Requires Only Three External Components.

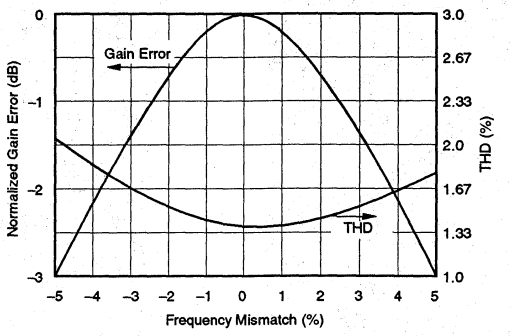


FIGURE 3. Measured Sine Wave Output THD and Normalized Gain Error vs Mismatch between Filter Center Frequency and Square Wave Input Frequency for the "Tuned-Circuit" Bandpass Filter Shown in Figure 2.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

BURR-BROWN® APPLICATION BULLETIN

Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

FILTER DESIGN PROGRAM FOR THE UAF42 UNIVERSAL ACTIVE FILTER

By Johnnie Molina and R. Mark Stitt (602) 746-7592

Although active filters are vital in modern electronics, their design and verification can be tedious and time consuming. To aid in the design of active filters, Burr-Brown provides a series of FilterPro™ computer-aided design programs. Using the FILTER42 program and the UAF42 it is easy to design and implement all kinds of active filters. The UAF42 is a monolithic IC which contains the op amps, matched resistors, and precision capacitors needed for a state-variable filter pole-pair. A fourth, uncommitted precision op amp is also included on the die.

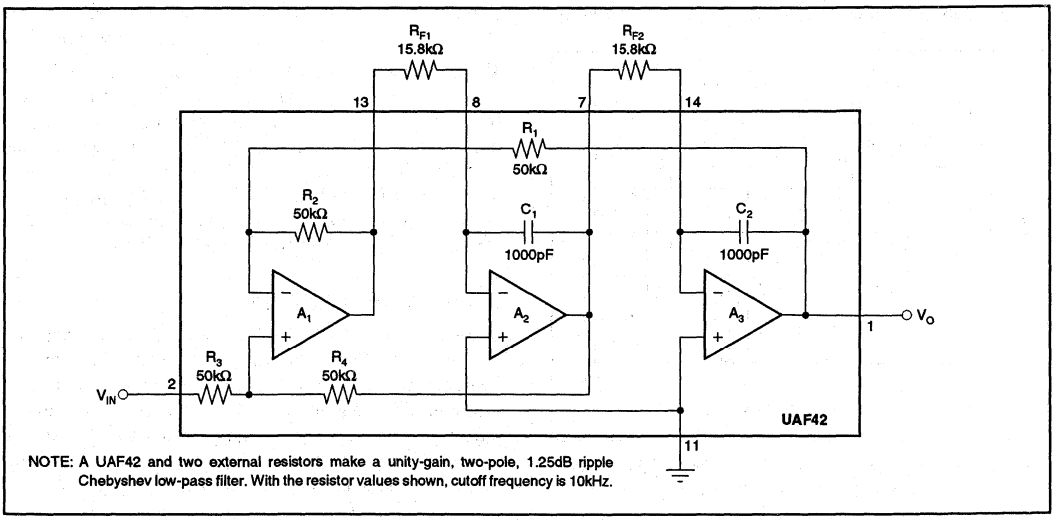
Filters implemented with the UAF42 are time-continuous, free from the switching noise and aliasing problems of switched-capacitor filters. Other advantages of the state-variable topology include low sensitivity of filter parameters to external component values and simultaneous low-pass, high-pass, and band-pass outputs. Simple two-pole filters can be made with a UAF42 and two external resistors—see Figure 1.

The DOS-compatible program guides you through the design process and automatically calculates component values. Low-pass, high-pass, band-pass, and band-reject (or notch) filters can be designed.

Active filters are designed to approximate an ideal filter response. For example, an ideal low-pass filter completely eliminates signals above the cutoff frequency (in the stop-band), and perfectly passes signals below it (in the pass-band). In real filters, various trade-offs are made in an attempt to approximate the ideal. Some filter types are optimized for gain flatness in the pass-band, some trade-off gain variation or ripple in the pass-band for a steeper rate of attenuation between the pass-band and stop-band (in the transition-band), still others trade-off both flatness and rate of roll-off in favor of pulse-response fidelity. FILTER42 supports the three most commonly used all-pole filter types: Butterworth, Chebyshev, and Bessel. The less familiar Inverse Chebyshev is also supported. If a two-pole band-pass or notch filter is selected, the program defaults to a resonant-circuit response.

Butterworth (maximally flat magnitude). This filter has the flattest possible pass-band magnitude response. Attenuation is –3dB at the design cutoff frequency. Attenuation beyond the cutoff frequency is a moderately steep –20dB/decade/pole. The pulse response of the Butterworth filter has moderate overshoot and ringing.

Chebyshev (equal ripple magnitude). (Other transliterations of the Russian о • – are Tschebychev, Tschebyscheff or Tchevysheff). This filter response has steeper initial rate of attenuation beyond the cutoff frequency than Butterworth.



NOTE: A UAF42 and two external resistors make a unity-gain, two-pole, 1.25dB ripple Chebyshev low-pass filter. With the resistor values shown, cutoff frequency is 10kHz.

FIGURE 1. Two-Pole Low-Pass Filter Using UAF42.

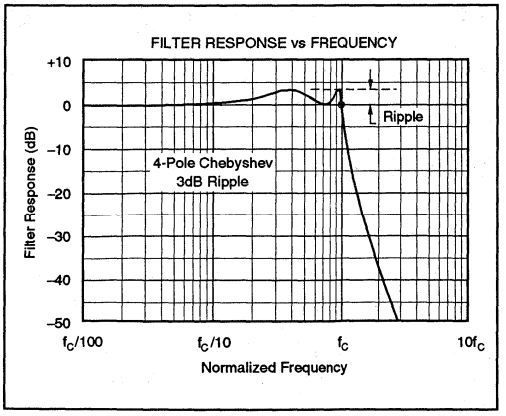


FIGURE 2A. Response vs Frequency for Even-Order (4-pole) 3dB Ripple Chebyshev Low-Pass Filter Showing Cutoff at 0dB.

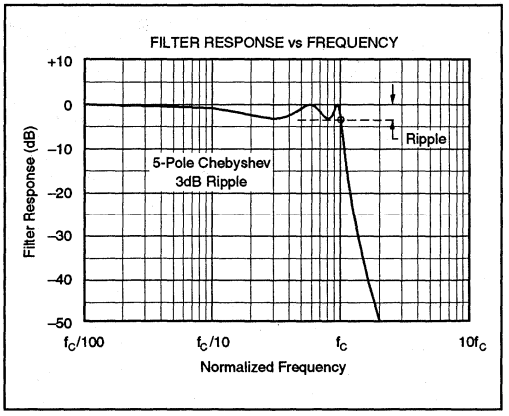


FIGURE 2B. Response vs Frequency for Odd-Order (5-pole) 3dB Ripple Chebyshev Low-Pass Filter Showing Cutoff at –3dB.

This advantage comes at the penalty of amplitude variation (ripple) in the pass-band. Unlike Butterworth and Bessel responses, which have 3dB attenuation at the cutoff frequency, Chebyshev cutoff frequency is defined as the frequency at which the response falls below the ripple band. For even-order filters, all ripple is above the dc-normalized passband gain response, so cutoff is at 0dB (see Figure 2A). For odd-order filters, all ripple is below the dc-normalized passband gain response, so cutoff is at –(ripple) dB (see Figure 2B). For a given number of poles, a steeper cutoff can be achieved by allowing more pass-band ripple. The Chebyshev has more ringing in its pulse response than the Butterworth—especially for high-ripple designs.

Inverse Chebyshev (equal minima of attenuation in the stop band). As its name implies, this filter type is cousin to the Chebyshev. The difference is that the ripple of the Inverse Chebyshev filter is confined to the stop-band. This filter type has a steep rate of roll-off and a flat magnitude response in the pass-band. Cutoff of the Inverse Chebyshev is defined as the frequency where the response first enters the specified stop-band—see Figure 3. Step response of the Inverse Chebyshev is similar to the Butterworth.

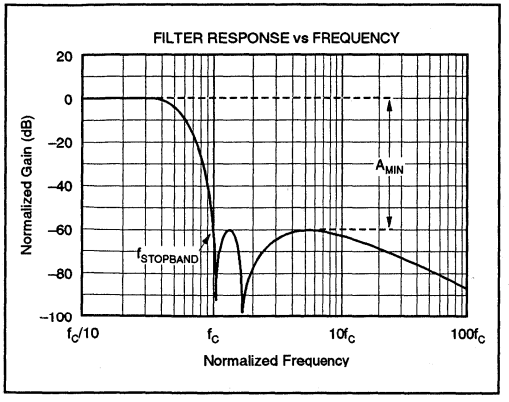


FIGURE 3. Response vs Frequency for 5-pole, –60dB Stop-Band, Inverse Chebyshev Low-Pass Filter Showing Cutoff at –60dB.

Bessel (maximally flat time delay), also called Thomson. Due to its linear phase response, this filter has excellent pulse response (minimal overshoot and ringing). For a given number of poles, its magnitude response is not as flat, nor is its initial rate of attenuation beyond the –3dB cutoff frequency as steep as the Butterworth. It takes a higher-order Bessel filter to give a magnitude response similar to a given Butterworth filter, but the pulse response fidelity of the Bessel filter may make the added complexity worthwhile.

Tuned Circuit (resonant or tuned-circuit response). If a two-pole band-pass or band-reject (notch) filter is selected, the program defaults to a tuned circuit response. When band-pass response is selected, the filter design approximates the response of a series-connected LC circuit as shown in Figure 4A. When a two-pole band-reject (notch) response is selected, filter design approximates the response of a parallel-connected LC circuit as shown in Figure 4B.

CIRCUIT IMPLEMENTATION

In general, filters designed by this program are implemented with cascaded filter subcircuits. Subcircuits either have a two-pole (complex pole-pair) response or a single real-pole response. The program automatically selects the subcircuits required based on function and performance. A program option allows you to override the automatic topology selection routine to specify either an inverting or noninverting pole-pair configuration.

The simplest filter circuit consists of a single pole-pair subcircuit as shown in Figure 5. More complex filters consist of two or more cascaded subcircuits as shown in Figure 6. Even-order filters are implemented entirely with UAF42 pole-pair sections and normally require no external capacitors. Odd-order filters additionally require one real pole section which can be implemented with the fourth uncommitted op amp in the UAF42, an external resistor, and an external capacitor. The program can be used to design filters up to tenth order.

The program guides you through the filter design and generates component values and a block diagram describing the filter circuit. The *Filter Block Diagram* program output shows the subcircuits needed to implement the filter design labeled by type and connected in the recommended order. The *Filter Component Values* program output shows the values of all external components needed to implement the filter.

SUMMARY OF FILTER TYPES

Butterworth

Advantages: Maximally flat magnitude response in the pass-band. Good all-around performance. Pulse response better than Chebyshev. Rate of attenuation better than Bessel.

Disadvantages: Some overshoot and ringing in step response.

Chebyshev

Advantages: Better rate of attenuation beyond the pass-band than Butterworth.

Disadvantages: Ripple in pass-band. Considerably more ringing in step response than Butterworth.

Inverse Chebyshev

Advantages: Flat magnitude response in pass-band with steep rate of attenuation in transition-band.

Disadvantages: Ripple in stop-band. Some overshoot and ringing in step response.

Bessel

Advantages: Best step response—very little overshoot or ringing.

Disadvantages: Slower initial rate of attenuation beyond the pass-band than Butterworth.

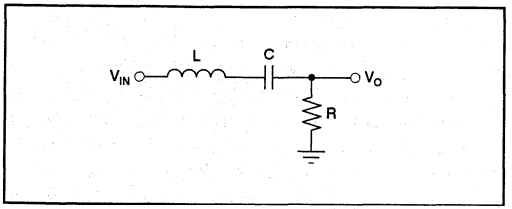


FIGURE 4A. n = 2 Band-Pass Filter Using UAF42 (approximates the response of a series-connected tuned L, C, R circuit).

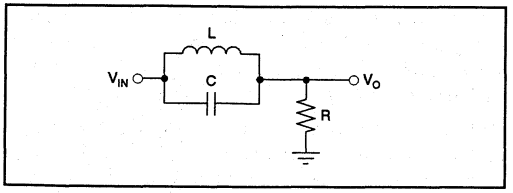


FIGURE 4B. n = 2 Band-Reject (Notch) Filter Using UAF42 (approximates the response of a parallel-connected tuned L, C, R circuit).

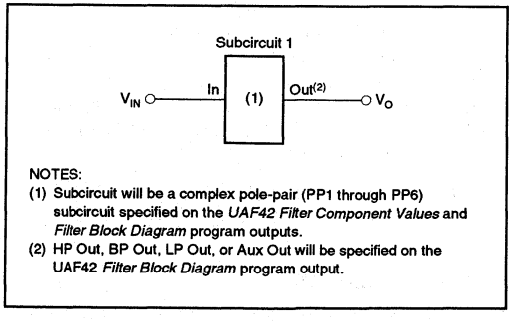


FIGURE 5. Simple Filter Made with Single Complex Pole-Pair Subcircuit.

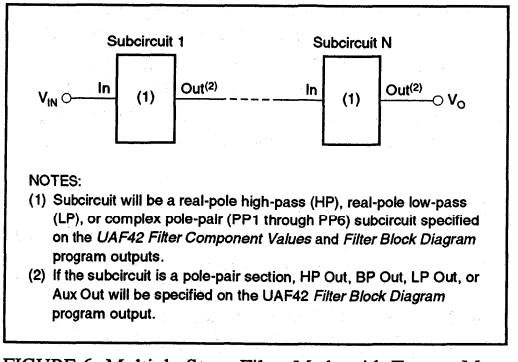


FIGURE 6. Multiple-Stage Filter Made with Two or More Subcircuits.

The program automatically places lower Q stages ahead of higher Q stages to prevent op amp output saturation due to gain peaking. Even so, peaking may limit input voltage to less than ±10V (V_S = ±15V). The maximum input voltage for each filter design is shown on the *filter block diagram.* If the UAF42 is to be operated on reduced supplies, the maximum input voltage must be derated commensurately. To use the filter with higher input voltages, you can add an input attenuator.

The program designs the simplest filter that provides the desired AC transfer function with a pass-band gain of 1.0V/V. In some cases the program cannot make a unity-gain filter and the pass-band gain will be less than 1.0V/V. In any case, overall filter gain is shown on the *filter block diagram.* If you want a different gain, you can add an additional stage for gain or attenuation as required.

To build the filter, print-out the block diagram and component values. Consider one subcircuit at a time. Match the subcircuit type referenced on the component print-out to its corresponding circuit diagram—see the Filter Subcircuits section of this bulletin.

The *UAF42 Filter Component Values* print-out has places to display every possible external component needed for any subcircuit. Not all of these components will be required for any specific filter design. When no value is shown for a component, omit the component. For example, the detailed schematic diagrams for complex pole-pair subcircuits show external capacitors in parallel with the 1000pF capacitors in the UAF42. No external capacitors are required for filters above approximately 10Hz.

After the subcircuits have been implemented, connect them in series in the order shown on the *filter block diagram.*

FILTER SUBCIRCUITS

Filter designs consist of cascaded complex pole-pair and real-pole subcircuits. Complex pole pair subcircuits are based on the UAF42 state-variable filter topology. Six variations of this circuit can be used, PP1 through PP6. Real pole sections can be implemented with the auxiliary op amp in the UAF42. High-pass (HP) and low-pass (LP) real-pole sections can be used. The subcircuits are referenced with a two or three letter abbreviation on the *UAF42 Filter Component Values* and *Filter Block Diagram* program outputs. Descriptions of each subcircuit follow:

POLE-PAIR (PP) SUBCIRCUITS

In general, all complex pole-pair subcircuits use the UAF42 in the state-variable configuration. The two filter parameters that must be set for the pole-pair are the filter Q and the natural frequency, f_O. External resistors are used to set these parameters. Two resistors, R_{F1} and R_{F2}, must be used to set the pole-pair f_O. A third external resistor, R_Q, is usually needed to set Q.

At low frequencies, the value required for the frequency-setting resistors can be excessive. Resistor values above about 5MΩ can react with parasitic capacitance causing poor filter performance. When f_O is below 10Hz, external capacitors must be added to keep the value of R_{F1} and R_{F2} below 5MΩ. When f_O is in the range of about 10Hz to 32Hz, An external 5.49kΩ resistor, R_{2A}, is added in parallel with the internal resistor, R_2, to reduce R_{F1} and R_{F2} by $\sqrt{10}$ and eliminate the need for external capacitors. At the other extreme, when f_O is above 10kHz, R_{2A}, is added in parallel with R_2 to improve stability.

External filter gain-set resistors, R_G, are always required when using an inverting pole-pair configuration or when using a noninverting configuration with Q < 0.57.

PP1 (Noninverting pole-pair subcircuit using internal gain-set resistor, R_3)—See Figure 7. In the automatic topology selection mode, this configuration is used for all band-pass filter responses. This configuration allows the combination of unity pass-band gain and high Q (up to 400). Since no external gain-set resistor is required, external parts count is minimized.

PP2 (Noninverting pole-pair subcircuit using an external gain-set resistor, R_G)—See Figure 8. This configuration is used when the pole-pair Q is less than 0.57.

PP3 (Inverting pole-pair subcircuit)—See Figure 9A. In the automatic topology selection mode, this configuration is used for the all-pole low-pass and high-pass filter responses. This configuration requires an external gain-set resistor, R_G. With R_G = 50kΩ, low-pass and high-pass gain are unity.

PP4 (Noninverting pole-pair/zero subcircuit)—See Figure 10. In addition to a complex pole-pair, this configuration produces a jω-axis zero (response null) by summing the low-pass and high-pass outputs using the auxiliary op amp, A_4, in the UAF42. In the automatic topology selection mode, this configuration is used for all band-reject (notch) filter responses and Inverse Chebyshev filter types when Q > 0.57. This subcircuit option keeps external parts count low by using the internal gain-set resistor, R_3.

PP5 (Noninverting pole-pair/zero subcircuit)—See Figure 11. In addition to a complex pole-pair, this configuration produces a jω-axis zero (response null) by summing the low-pass and high-pass outputs using the auxiliary op amp, A_4, in the UAF42. In the automatic topology selection mode, this configuration is used for all band-reject (notch) filter responses and Inverse Chebyshev filter types when Q < 0.57. This subcircuit option requires an external gain-set resistor, R_G.

PP6 (Inverting pole-pair/zero subcircuit)—See Figure 12. In addition to a complex pole-pair, this configuration produces a jω-axis zero (response null) by summing the low-pass and high-pass outputs using the auxiliary op amp, A_4, in the UAF42. This subcircuit is only used when you override the automatic topology selection algorithm and specify the inverting pole-pair topology. Then it is used for all band-reject (notch) filter responses and Inverse Chebyshev filter types.

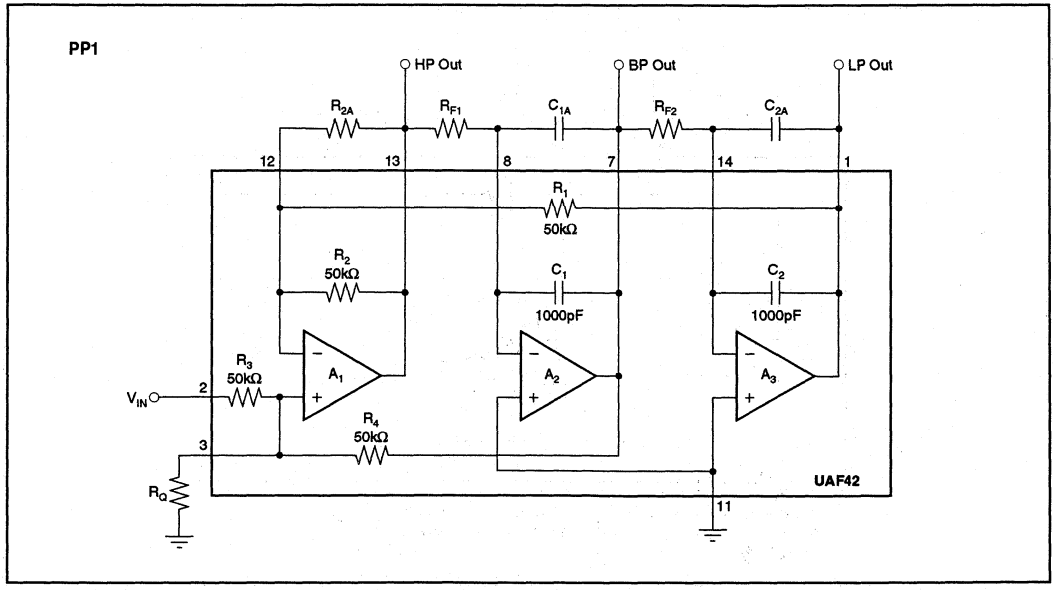


FIGURE 7. PP1 Noninverting Pole-Pair Subcircuit Using Internal Gain-Set Resistor R_3.

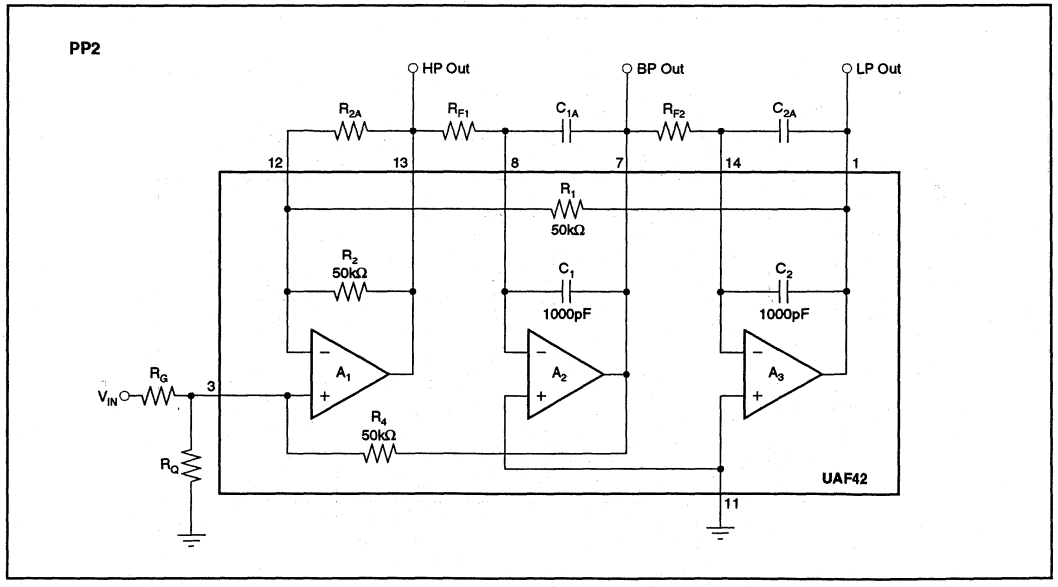


FIGURE 8. PP2 Noninverting Pole-Pair Subcircuit Using External Gain-Set Resistor R_G.

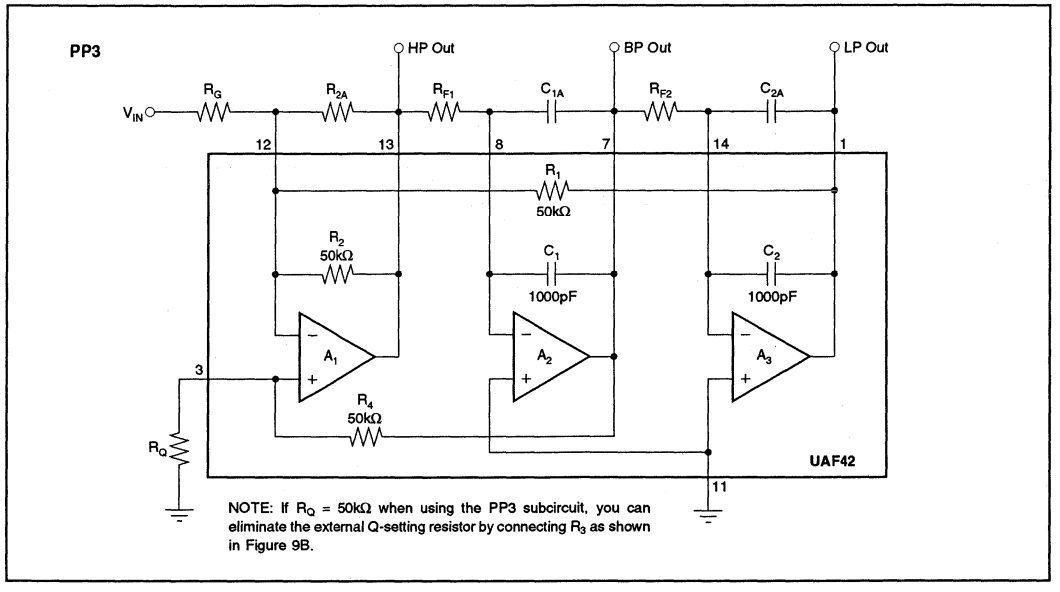


FIGURE 9A. PP3 Inverting Pole-Pair Subcircuit.

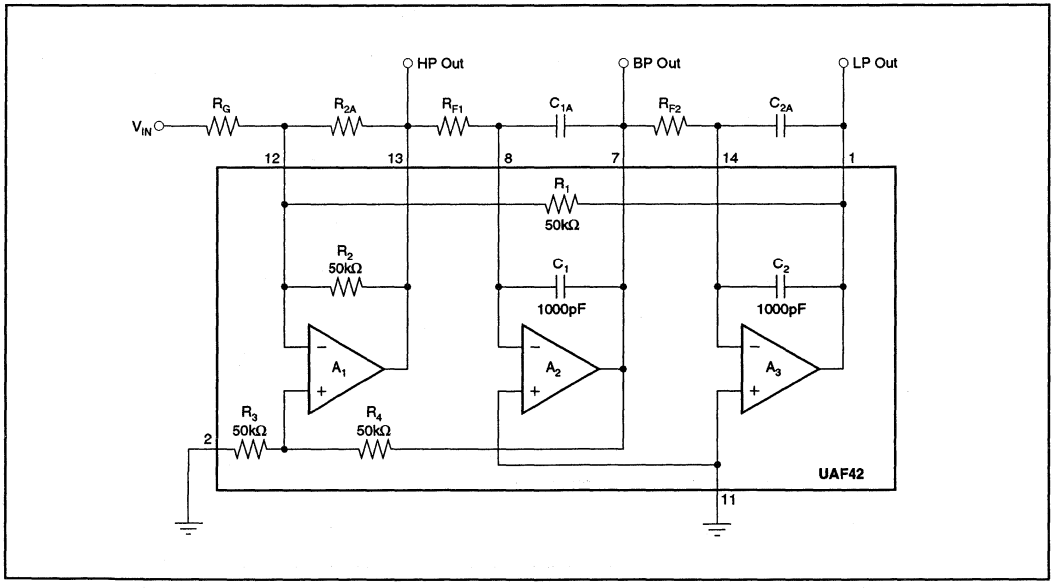


FIGURE 9B. Inverting Pole-Pair Subcircuit Using R_3 to Eliminate External Q-Setting Resistor R_G.

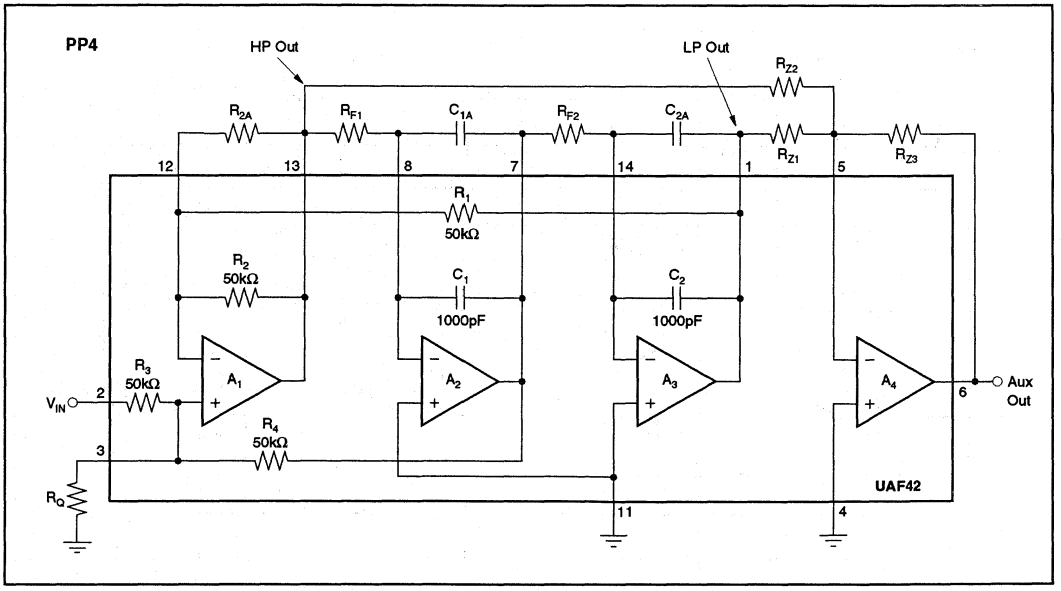


FIGURE 10. PP4 Noninverting Pole-Pair/Zero Subcircuit Using Internal Gain-Set Resistor R_3.

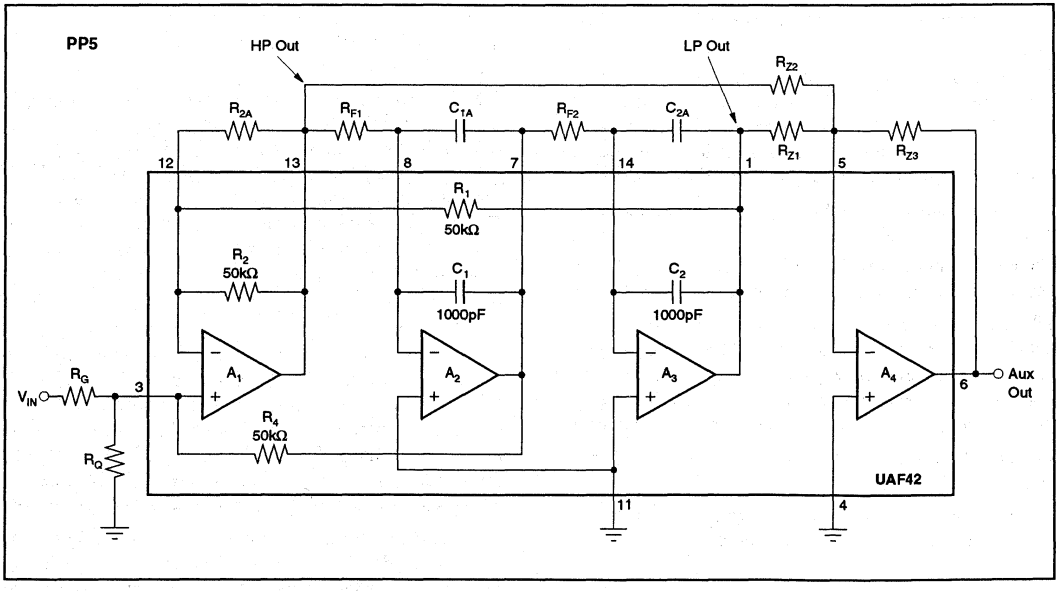


FIGURE 11. PP5 Noninverting Pole-Pair/Zero Subcircuit Using External Gain-Set Resistor R_G.

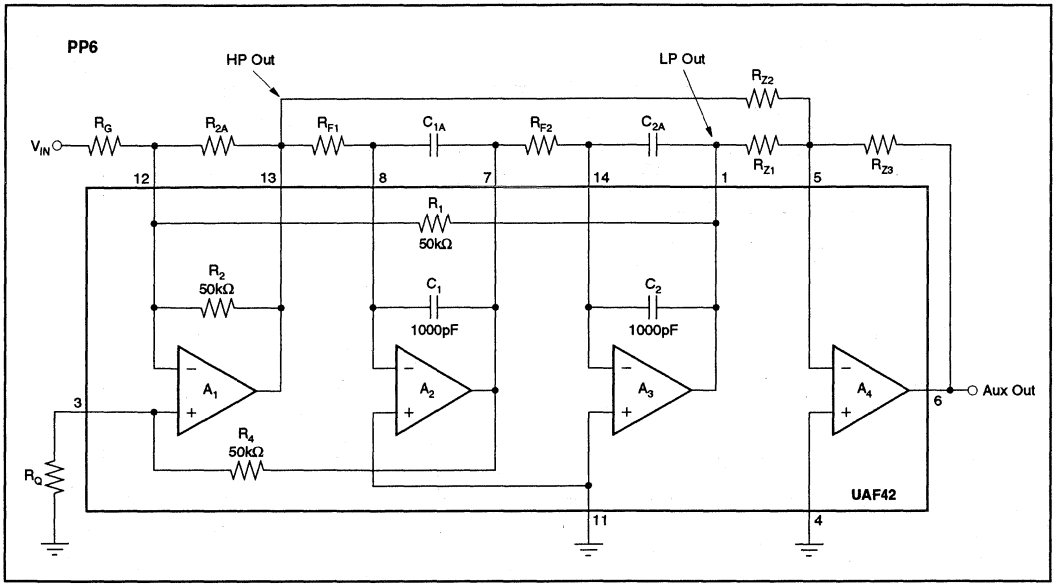


FIGURE 12. PP6 Inverting Pole-Pair/Zero Subcircuit.

This subcircuit option requires an external gain-set resistor, R_G.

LP (Real-pole low-pass subcircuit). The basic low-pass subcircuit (LP) is shown in Figure 13A. A single pole is formed by R_P and C_P. A_2 buffers the output to prevent loading from subsequent stages. If high input impedance is needed, an optional buffer, A_1, can be added to the input.

For an LP subcircuit with gain, use the optional circuit shown in Figure 13B.

For an LP subcircuit with inverting gain or attenuation, use the optional circuit shown in Figure 13C.

HP (Real-pole high-pass subcircuit). The basic high-pass subcircuit (HP) is shown in Figure 14A. A single pole is formed by R_P and C_P. A_2 buffers the output to prevent loading from subsequent stages. If high input impedance is needed, an optional buffer, A_1, can be added to the input.

For an HP subcircuit with gain, use the optional circuit shown in Figure 14B.

For an HP subcircuit with inverting gain or attenuation, use the optional circuit shown in Figure 14C.

IF THE AUXILIARY OP AMP IN A UAF42 IS NOT USED

If the auxiliary op amp in a UAF42 is not used, connect it as a grounded unity-gain follower as shown in Figure 15. This will keep its inputs and output in the linear region of operation to prevent biasing anomalies which may affect the other op amps in the UAF42.

ELIMINATING THE LP SUBCIRCUIT IN ODD-ORDER INVERSE CHEBYSHEV LOW-PASS FILTERS

Odd-order Inverse Chebyshev low-pass filters can be simplified by eliminating the LP input section and forming the real pole in the first pole-pair/zero subcircuit. To form the real pole in the pole-pair/zero subcircuit, place a capacitor, C_1, in parallel with the summing amplifier feedback resistor, R_{Z3}. The real pole must be at the same frequency as in the LP subcircuit. One way to achieve this is to set $C_1 = C_P$ and $R_{Z3} = R_P$, where C_P and R_P are the values that were specified for the LP section. Then, to keep the summing amplifier gains the same, multiply R_{Z1} and R_{Z2} by R_P/R_{Z3}.

Figures 16A and 16B show an example of the modification of a 3-pole circuit. It is a 347Hz-cutoff inverse Chebyshev low-pass filter. This example is from an application which required a low-pass filter with a notch for 400Hz system power-supply noise. Setting the cutoff at 347Hz produced the 400Hz notch. The standard filter (Figure 16A) consists of two subcircuits, an LP section followed by a PP4 section.

In the simplified configuration (Figure 16B), the summing amplifier feedback resistor, R_{Z3} is changed from 10kΩ to 130kΩ and paralleled with a 0.01µF capacitor. Notice that these are the same values used for R_P and C_P in the LP section of Figure 16A. To set correct the summing amplifier gain, resistors, R_{Z1} and R_{Z2} are multiplied by R_P/R_{Z3} (130kΩ/10kΩ). R_{Z1} and R_{Z2} must be greater than 2kΩ to prevent op amp output overloading. If necessary, increase R_{Z1}, R_{Z2}, and R_{Z3} by decreasing C_P.

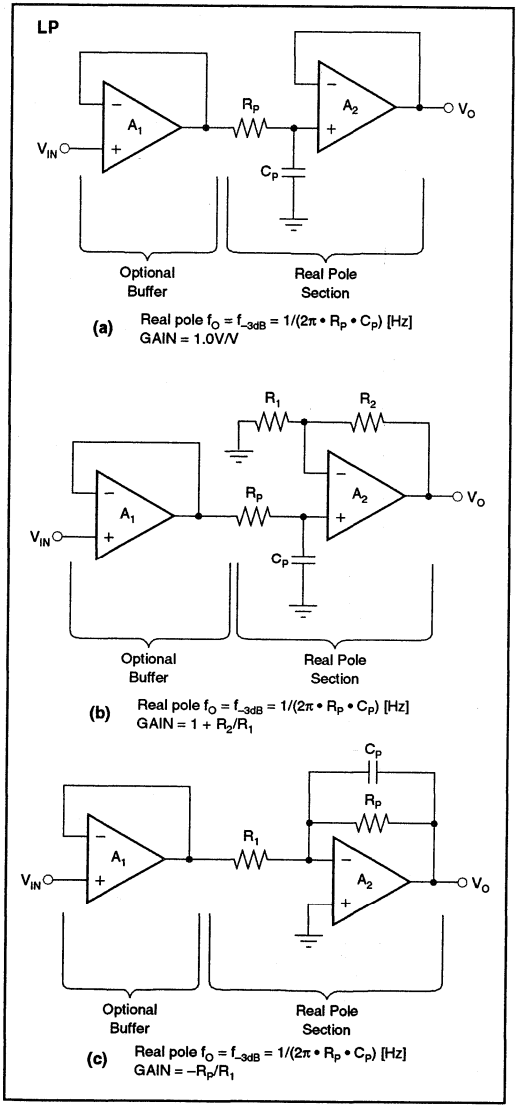


FIGURE 13. Low-Pass (LP) Subcircuit: (a) Basic; (b) with Noninverting Gain; (c) with Inverting Gain.

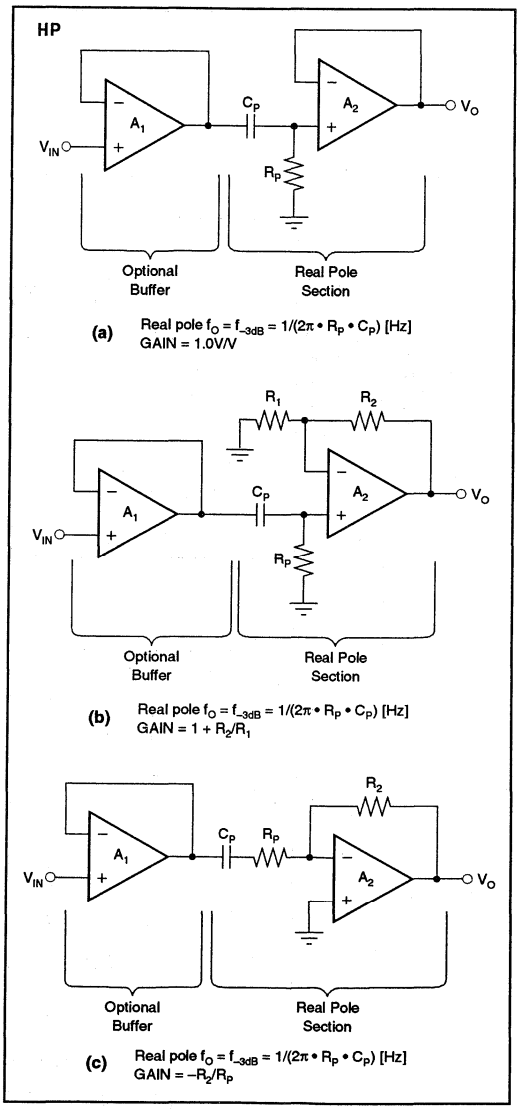


FIGURE 14. High-Pass (HP) Subcircuit: (a) Basic; (b) with Noninverting Gain; (c) with Inverting Gain.

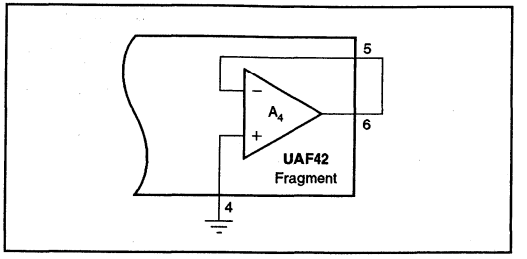


FIGURE 15. Connect Unused Auxiliary Op Amps as Grounded-Input Unity-Gain Followers.

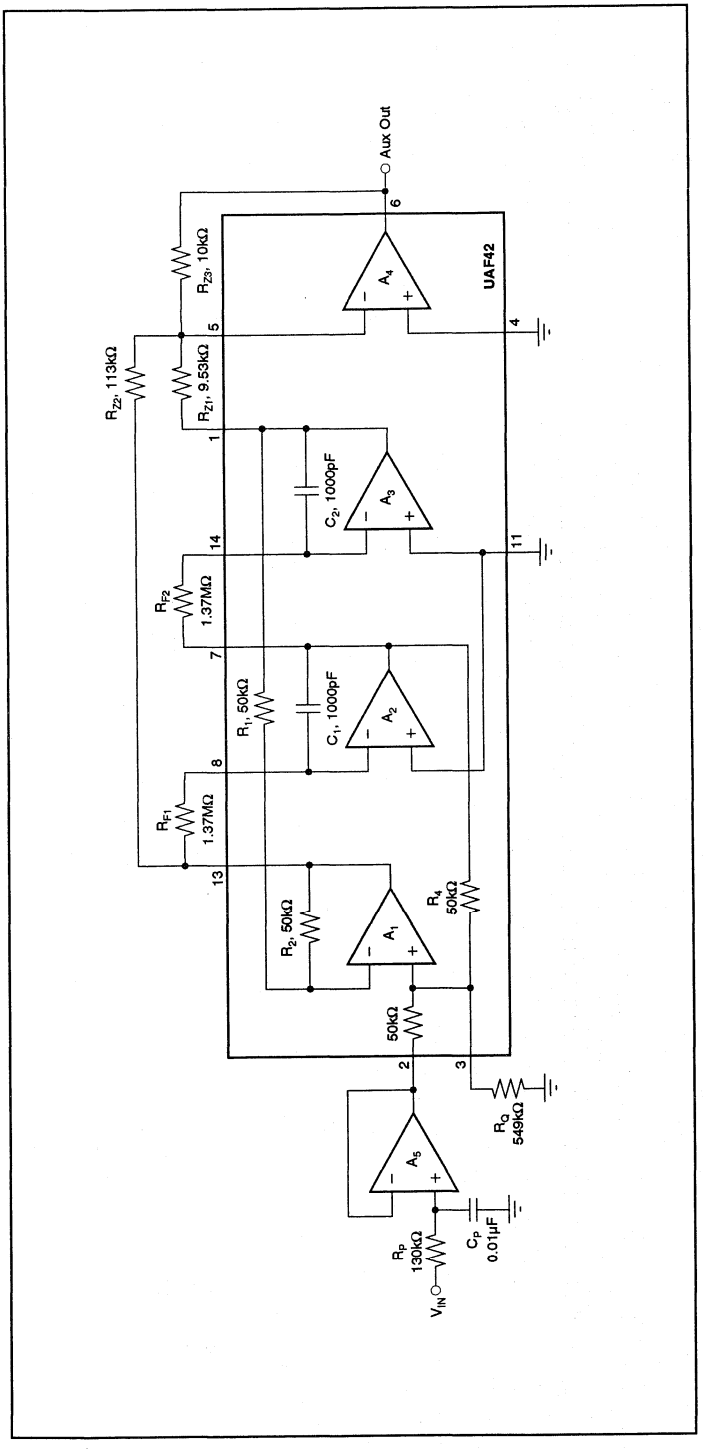


FIGURE 16A. Three-Pole 347Hz Inverse Chebyshev Low-Pass Filter Designed by FilterPro™ Program.

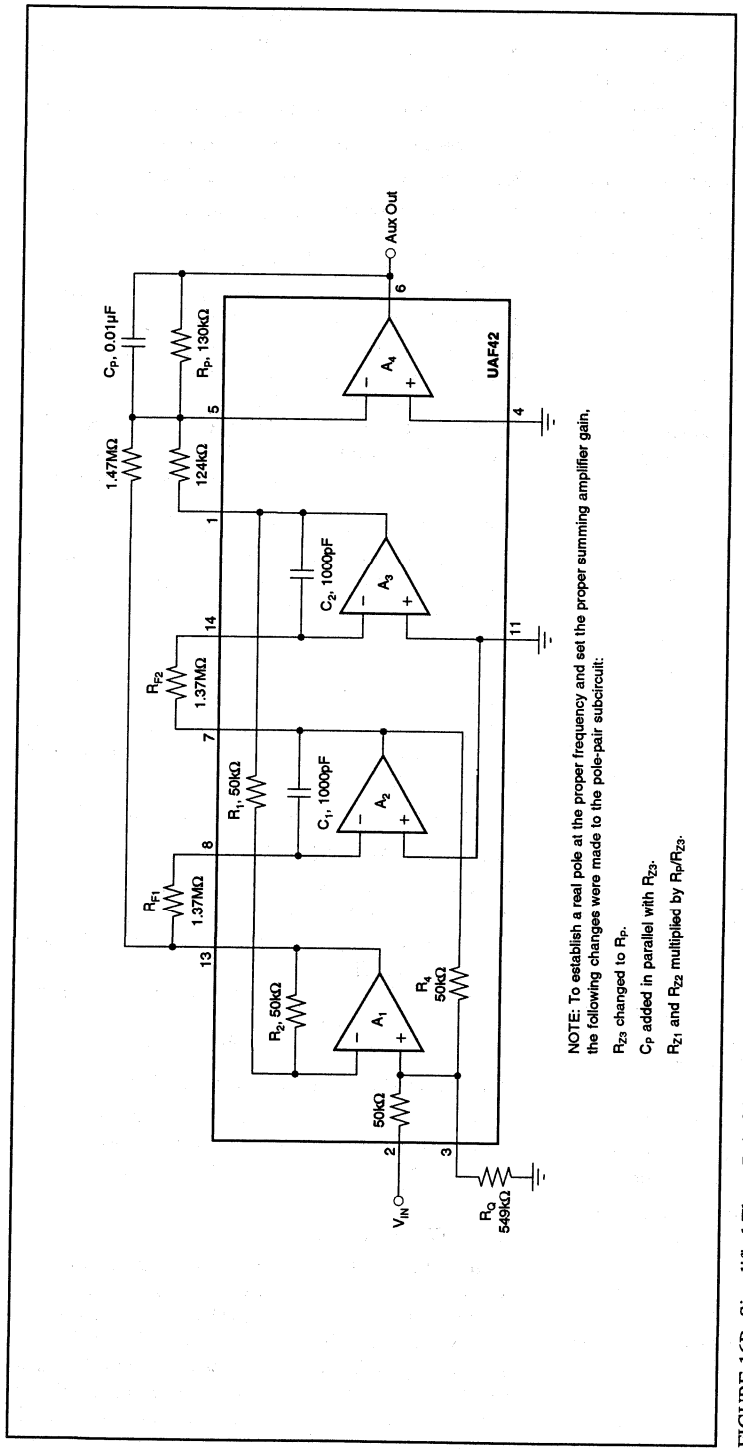


FIGURE 16B. Simplified Three-Pole 347Hz Inverse Chebyshev Low-Pass Filter (created by moving real pole to feedback of A_4 and eliminating LP input section).

Q ENHANCEMENT

When the f_O • Q product required for a pole-pair section is above ≈100kHz at frequencies above ≈3kHz, op amp gain-bandwidth limitations can cause Q errors and gain peaking. To mitigate this effect, the program automatically compensates for the expected error by decreasing the design-Q according to a Q-compensation algorithm[1]. When this occurs, the value under the Q heading on the *UAF42 Filter Component Values* print-out will be marked with an asterisk indicating that it is the theoretical Q, not the actual design Q. The actual design Q will be shown under an added heading labeled Q_{COMP}.

USING THE FilterPro™ PROGRAM

With each data entry, the program automatically calculates filter performance. This allows you to use a "what if" spreadsheet-type design approach. For example; you can quickly determine, by trial and error, how many poles are needed for a desired roll-off.

GETTING STARTED

The first time you use the program, you may want to follow these suggested steps.

Type **FILTER42 <ENTER>** to start the program.

Use the arrow keys to move the cursor to the **Filter Response** section.

1) SELECT FILTER RESPONSE

Press **<ENTER>** to toggle through four response choices:

Low-pass
High-pass
Band-pass
Notch (band-reject)

When the desired response appears, move the cursor to the **Filter Type** section.

2) SELECT FILTER TYPE

Move the cursor to the desired filter type and press **<ENTER>**. The selected filter type is highlighted and marked with an asterisk. There are four filter-type choices:

Butterworth	Bessel
Chebyshev	Inverse Chebyshev

If you choose Chebyshev, you must also enter ripple (i.e. pass-band ripple—see Chebyshev filter description).

If you choose Inverse Chebyshev, you must also enter A_{MIN} (i.e. min attenuation or max gain in stop-band—see Inverse Chebyshev filter description).

3) ENTER FILTER ORDER

Move the cursor to the **Filter Order** line in the **Parameters** section. Enter filter order **n** (from 2 to 10).

4A) ENTER FILTER FREQUENCY

Move the cursor to the **Filter Frequency** line in the **Parameters** section.

Low-pass/high-pass filter: enter the f_{-3dB} or cutoff frequency.

Band-pass filter: enter the center frequency, f_{CENTER}.

Band-reject (notch) filter: enter the notch frequency, f_{NOTCH}.

If your filter is low-pass or high-pass, go to step 5.

4B) ENTER FILTER BANDWIDTH

If the filter is a band-pass or band-reject (notch), move the cursor to the bandwidth line and enter bandwidth.

If you press **<ENTER>** with no entry on the bandwidth line, you can enter f_L and f_H instead of bandwidth. f_L and f_H are the f_{-3dB} points with regard to the center frequency for Butterworth and Bessel filters. They are the end of the ripple-band for Chebyshev types. This method of entry may force a change in center frequency or notch frequency.

5) PRINT-OUT COMPONENT VALUES

Press function key **<F4>** to print-out **Filter Component Values** and a **Filter Block Diagram.** Follow the instructions in the filter implementation section of this bulletin to assemble a working filter.

USING THE PLOT FEATURE

A Plot feature allows you to view graphical results of filter gain and phase vs frequency. This feature is useful for comparing filter types.

To view a plot of the current filter design, press **<F2>**.

GRAPHIC DISPLAY COMMANDS

While viewing the graphic display, several commands can be used to compare filter responses:

<F1> or **S**—*S*aves the plot of the current design for future recall.
<F2> or **R**—*R*ecalls the *S*aved plot and plots it along with the current design.
<F3> or **Z**—Plots a Zero dB reference line.

GRAPHIC DISPLAY CURSOR CONTROL

While viewing the graphics display you can also use the arrow keys to move a cursor and view gain and phase for plotted filter responses.

RESISTOR VALUES

With each data entry, the program automatically calculates resistor values. If external capacitors are needed, the program selects standard capacitor values and calculates exact resistor values for the filter you have selected. The **1% Resistors** option in the Display menu can be used to calculate the closest standard 1% resistor values instead of exact resistor values. To use this feature, move the cursor to the **resistors** line in the **Filter Response** section and press

(1) L.P. Huelsman and P. E. Allen, *Theory and Design of Active Filters*, p. 241.

OP AMP SELECTION GUIDE (In Order of Increasing Slew Rate)

T_A = 25°C, V_S = ±15V, specifications typ, unless otherwise noted, min/max specifications are for high-grade model.

OP AMP MODEL	BW typ (MHz)	FPR (1) typ (kHz)	SR typ (V/µs)	V_{OS} max (µV)	V_{OS}/dT max (µV/°C)	NOISE at 10kHz (nV/√Hz)	C_{CM} (3) (pF)
OPA177	0.6	3	0.2	10	±0.1	8	1
OPA27	8	30	1.9	25	±0.6	2.7	1
OPA2107 dual (2)	4.5	280	18	500	±5	8	4
OPA602 (2)	6	500	35	250	±2	12	3
OPA404 quad (2)	6	500	35	1000	±3 typ	12	3
OPA627 (2)	16	875	55	100	±0.8	4.5	7
UAF42 aux amp (2)	4	160	10	5000	±3 typ	10	4

NOTES: (1) FPR is full power response at 20Vp-p as calculated from slew rate. (2) These op amps have FET inputs. (3) Common-mode input capacitance.

<ENTER>. The program will toggle between **exact resistors** and **standard 1% resistors.**

CAPACITOR SELECTION

Even-order filters above 10Hz normally will not require external capacitors. Odd order filters require one external capacitor to set the real pole in the LP or HP section. Capacitor selection is very important for a high-performance filter. Capacitor behavior can vary significantly from ideal, introducing series resistance and inductance which limit Q. Also, nonlinearity of capacitance vs voltage causes distortion. The 1000pF capacitors in the UAF42 are high performance types laser trimmed to 0.5%.

If external capacitors are required, the recommended capacitor types are: NPO ceramic, silver mica, metallized polycarbonate; and, for temperatures up to 85°C, polypropylene or polystyrene. Common ceramic capacitors with high dielectric constants, such as "high-K" types should be avoided—they can cause errors in filter circuits.

OP AMP SELECTION

Normally you can use the uncommitted fourth op amp in the UAF42 to implement any necessary LP, HP, or gain stages. If you must use additional op amps, it is important to choose an op amp that can provide the necessary DC precision, noise, distortion, and speed.

OP AMP SLEW RATE

The slew rate of the op amp must be greater than $\pi \cdot V_{OPP} \cdot$ BANDWIDTH for adequate full-power response. For example, operating at 100kHz with 20Vp-p output requires an op amp slew rate of at least 6.3V/µs. Burr-Brown offers an excellent selection of op amps which can be used for high performance active filter sections. The guide above lists some good choices.

OP AMP BANDWIDTH

As a rule of thumb, in low-pass and band-pass applications, op amp bandwidth should be at least 50 • GAIN • f_O, where GAIN = noise gain of the op amp configuration and f_O = filter f_{-3dB} or f_{CENTER} frequency.

In high-pass and band-reject (notch) applications, the required op amp bandwidth depends on the upper frequency of interest. As with most active filters, high-pass filters designed with the UAF42 turn into band-pass filters with an upper roll-off determined by the op amp bandwidth. Error due to op amp roll-off can be calculated as follows:

$$\% = 100\left(1 - \frac{1}{\sqrt{(1 + f^2 \cdot (NGAIN)^2/(UGBW)^2)}}\right)$$

or

$$f = \frac{\sqrt{200 - \%} \cdot \sqrt{\%} \cdot UGBW}{NGAIN \cdot (\% - 100)}$$

Where:
% = Percent gain error f = Frequency of interest (Hz)
NGAIN = Noise gain of op amp (V/V)
= GAIN of noninverting configuration
= 1 + |GAIN| of inverting configuration
UGBW = Unity-gain bandwidth of the op amp (Hz):

GAIN ACCURACY (%)	f (NGAIN)/(UGBW)
–29.29	1.000
–10.00	0.484
–1.00	0.142
–0.10	0.045
–0.01	0.014

EXAMPLES OF MEASURED UAF42 FILTER RESPONSE

Figures 17 and 18 show actual measured magnitude response plots for 5th-order 5kHz Butterworth, 3dB Chebyshev, –60dB Inverse Chebyshev and Bessel low-pass filters designed with the program and implemented with UAF42s. As can be seen, the initial roll-off of the Chebyshev filter is the fastest and the roll-off of the Bessel filter is the slowest. However, each of the 5th-order all-pole filters ultimately rolls off at –N • 20dB/decade, where N is the filter order (–100dB/decade for a 5-pole filter).

The oscilloscope photographs (Figures 19-22) show the step response for each filter. As expected, the Chebyshev filter has the most ringing, while the Bessel has the least.

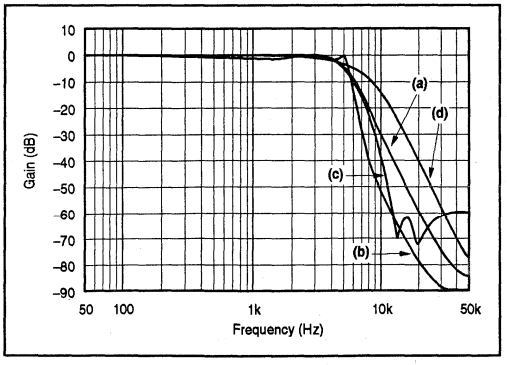


FIGURE 17. Gain vs Frequency for Fifth-Order 5kHz (a) Butterworth, (b) 3dB Chebyshev, (c) –60dB Inverse Chebyshev, and (d) Bessel Unity-Gain Low-Pass Filters, Showing Overall Filter Response.

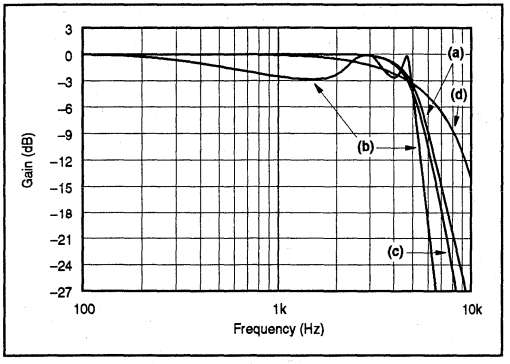


FIGURE 18. Gain vs Frequency for Fifth-Order 5kHz (a) Butterworth, (b) 3dB Chebyshev, (c) –60dB Inverse Chebyshev, and (d) Bessel Unity-Gain Low-Pass Filters, Showing Transition-Band Detail.

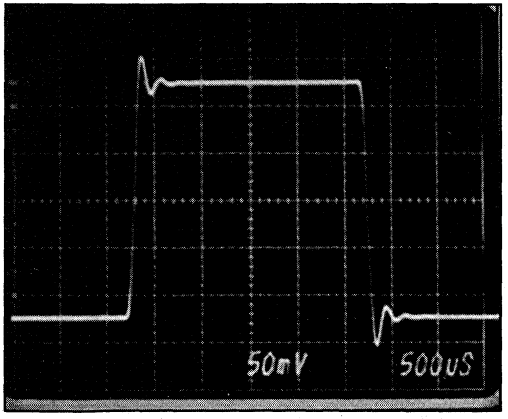


FIGURE 19. Step Response of Fifth-Order 5kHz Butterworth Low-Pass Filter.

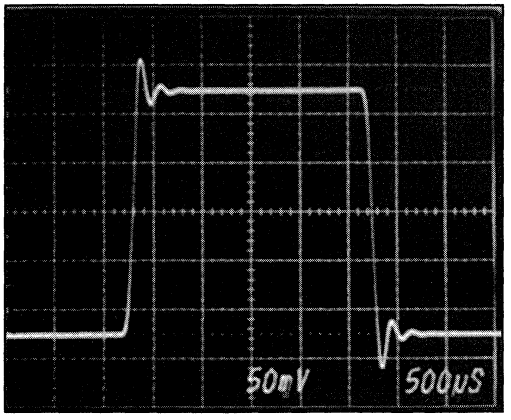


FIGURE 21. Step Response of Fifth-Order 5kHz, –60dB Inverse Chebyshev Low-Pass Filter.

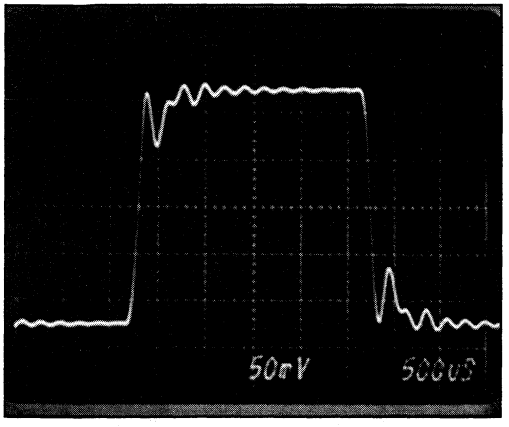


FIGURE 20. Step Response of Fifth-Order 5kHz, 3dB Ripple Chebyshev Low-Pass Filter.

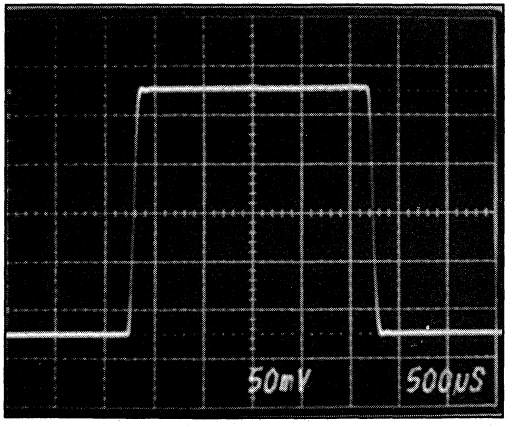


FIGURE 22. Step Response of Fifth-Order 5kHz Bessel Low-Pass Filter.

BURR-BROWN® APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

DESIGN A 60Hz NOTCH FILTER WITH THE UAF42

by Johnnie Molina, (602) 746-7592

DESIGN A 60Hz NOTCH FILTER WITH THE UAF42

The UAF42 is a monolithic, time-continuous, 2nd-order active filter building block for complex and simple filter designs. It uses the classical state-variable analog architecture with a summing amplifier plus two integrators. This topology offers low sensitivity of filter design parameters f_O (natural frequency) and Q to external component variations along with simultaneous high-pass, low-pass and band-pass outputs. An auxiliary high performance operational amplifier is also provided which can be used for buffering, gain, real pole circuits, or for summing the high-pass and low-pass outputs to create a band reject (notch) filter (see Figure 1).

A notch filter is easily realized with the UAF42 and six external resistors. Figure 2 shows the UAF42 configured into a 60Hz notch filter. The auxiliary operational amplifier is used to sum both the high-pass and low-pass outputs. At $f = f_{NOTCH}$, both of these outputs times their respective gain at the summing circuit are equal in magnitude but 180° out of phase. Hence, the output goes to zero. Figure 3 shows the response plot for the circuit shown in Figure 2 where f_O = 60Hz and Q = 6.

The notch frequency for the notch filter is set by the following calculations:

$$f_{NOTCH} = \sqrt{(A_{LP} / A_{HP} \bullet R_{Z2} / R_{Z1})} \bullet f_O$$

where,

A_{LP} = gain from input to low-pass out at f = 0Hz.

A_{HP} = gain from input to high-pass out of $f >> f_O$.

Typically, $A_{LP}/A_{HP} \bullet R_{Z2}/R_{Z1}$ is equal to one. This simplifies f_{NOTCH} to be,

$$f_{NOTCH} = f_O$$

f_O is given by, $f_O = \dfrac{1}{R_F \bullet C \bullet 2\pi}$

where, $R_F = R_{F1} = R_{F2}$ and $C = C_1 = C_2$

Note that the notch frequency can be modified by simply changing the R_F resistors and/or adding external capacitors. NPO ceramic, mica or a good film capacitor with low dissipation factor characteristics is recommended.

The –3dB bandwidth, as shown in Figure 3, can be set by the following calculations.

$$BW_{-3dB} = f_{NOTCH}/Q$$

where, $BW_{-3dB} = f_H - f_L$

The filter Q can be determined by setting R_Q to a value given by,

$$R_Q = \frac{25k\Omega}{Q-1}$$

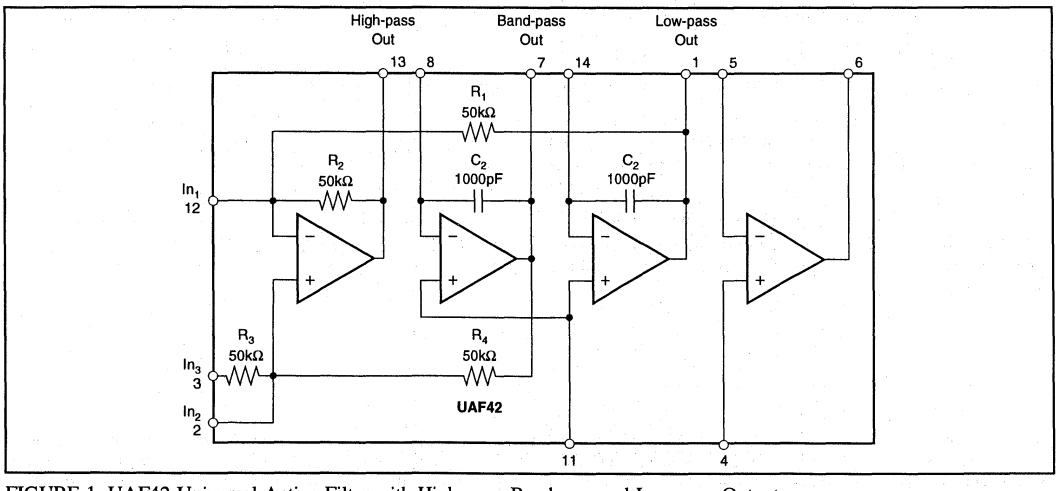


FIGURE 1. UAF42 Universal Active Filter with High-pass, Band-pass and Low-pass Outputs.

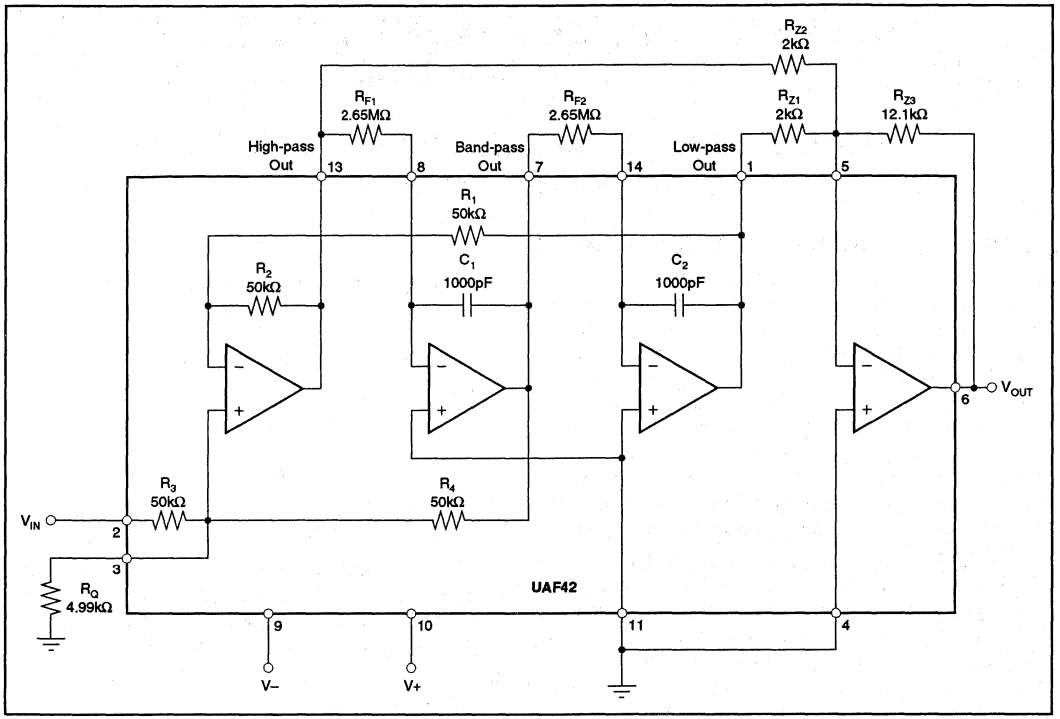


FIGURE 2. UAF42 Configured as a 60Hz Notch Filter.

The pass-band gain of the notch filter is influenced by the filter Q and should be adjusted for unity by setting the summing circuit feedback and input resistor ratios such that,

$$Q = \frac{R_{Z3}}{R_{Z1}} = \frac{R_{Z3}}{R_{Z2}}$$

Note that both filter parameters f_o and Q can be independently set with the proper selection of external components R_{F1}, R_{F2} and R_Q.

A UAF42 filter design program, FILTER42, along with application bulletin AB-035 is available at no cost which greatly simplifies the design process. A spreadsheet-style "what if" approach can be used to design a variety of filter approximations (Butterworth, Inverse Chebyschev, etc). Response plots, component values and circuit topology information is all provided.

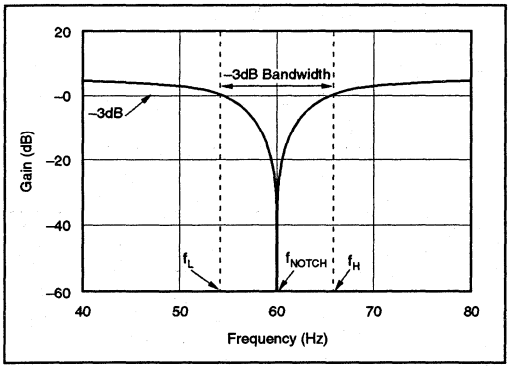


FIGURE 3. 60Hz Notch Filter Response.

BURR-BROWN® APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

THE ACF2101 USED AS A BIPOLAR SWITCHED INTEGRATOR

By Bonnie Baker

The ACF2101 is a dual, switched integrator that is typically used to convert a positive input current to a negative output voltage by integration, using an integration capacitor (C_{INT}), either on the chip or a external capacitor provided by the user. Typical applications for the ACF2101 are photo diode integrators (as shown in Figure 1), current measurements, charge measurements, and a CT scanner front end. In Figure 1, 1/2 of the ACF2101 integrates a positive input current to a 0 to –10V output signal. The transfer function of the integrator is:

$$V_{OUT} = -\frac{1}{C_{INT}} \int_0^t I_{IN}\, dt + \text{constant}$$

where C_{INT} = integration capacitor
I_{IN} = positive input current
constant = initial voltage at output

Assuming that the initial voltage at the output of the integrator is 0V, the transfer function becomes:

$$V_{OUT} = -\frac{1}{C_{INT}} \int_0^t I_{IN}\, dt$$

The ACF2101 is specified for a maximum input current of 100µA. The input current magnitude is limited by the slew rate of the operational amplifier and by the resistance of the hold switch. The slew rate is specified at 1V/µs minimum. If the user has an input device that supplies a higher maximum positive current, an external capacitor can be added to comply with the slew rate specification of the operational amplifier and the input signal can be connected to the "In" pin, bypassing the hold switch.

The hold and reset switches are used to control the ACF2101. Three basic modes of operation are controlled by these switches. In the integrate mode, the output voltage integrates from 0 to –10V. In the hold mode, the output voltage is held at the present level. In the reset mode, the output returns to zero so the integration cycle can start again. The switching diagram for these modes are shown in Figure 2. The output of the ACF2101 is selectable by use of the select switches, which can be used to multiplex the outputs when multiple integrators are connected to a common bus. The internal capacitor (C_F) can be used alone or in parallel with an external capacitor (C_{OPT}). In addition, the external capacitor can be used without the internal capacitor if needed.

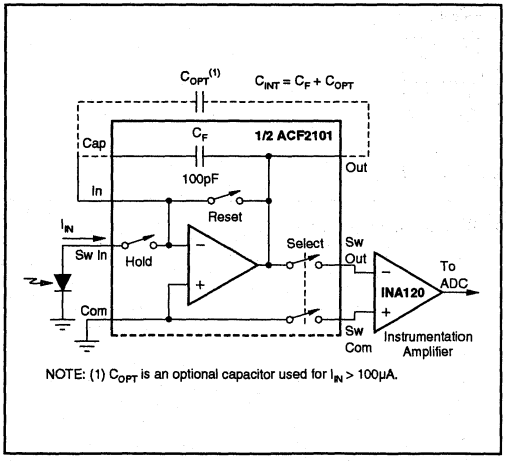
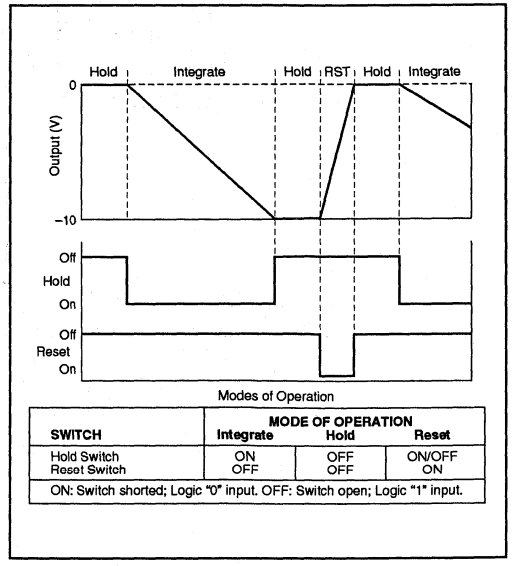


FIGURE 1. A Typical Application for the ACF2101 Switched Integrator.



SWITCH	MODE OF OPERATION Integrate	Hold	Reset
Hold Switch	ON	OFF	ON/OFF
Reset Switch	OFF	OFF	ON

ON: Switch shorted; Logic "0" input. OFF: Switch open; Logic "1" input.

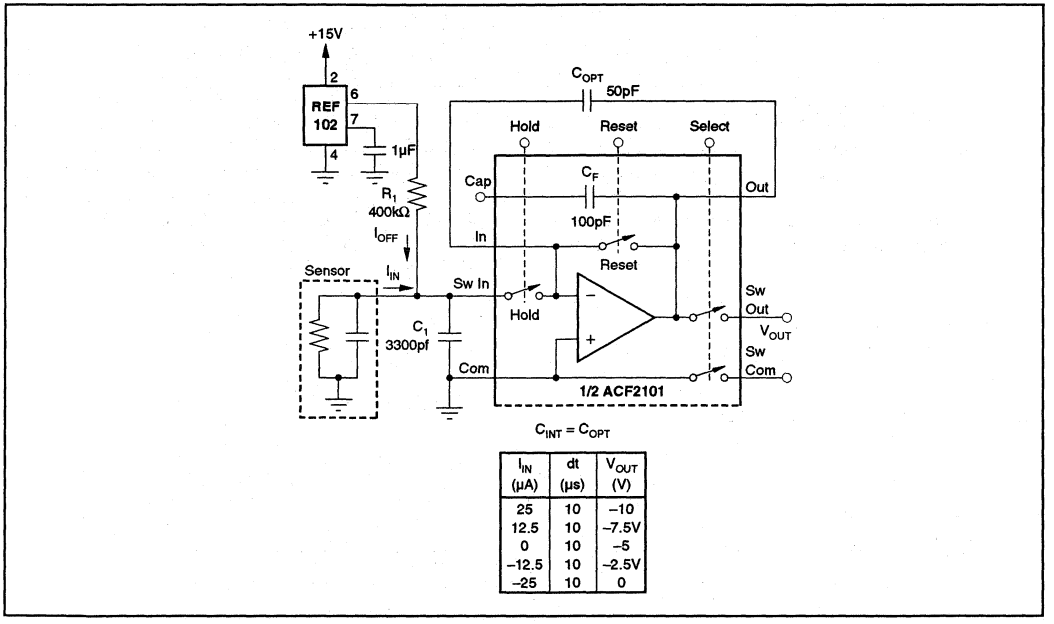
FIGURE 2. Modes of Operation for the ACF2101.

A second application for the ACF2101 is shown in Figure 3. Here the input current is bipolar such as found in radar or accelerometer applications. The hold and reset switches are designed to withstand –10V to +0.5V. A bipolar input signal will cause the protection circuitry of the reset and hold switch to conduct if the input or output exceeds +0.5V. A positive dc offset current (I_{OFF}) is injected into the input of the integrator to balance the effects of the bipolar signal. The magnitude of the offset current (I_{OFF}) must be equal to or greater than the magnitude of the negative portion of the bipolar input current.

As an example, if the full scale input current of the input device is ±25µA, an offset current of +25µA is required to insure the output will integrate negative. C_{OPT} is 50pf to take advantage of slew rate minimum of the ACF2101. With a 10µs integration time, the output of the ACF2101 will always be between 0V and –10V. A zero input current will produce a –5V output at the end of conversion. Output voltage vs bipolar input current is tabulated in Figure 3. C_1 clamps the input of the hold switch to less than +0.5V. As another example, the input current could be ±1µA. R_1 would be changed to 10MΩ and C_{OPT} is no longer needed. With an integration time of 1ms, the output of the ACF2101 will always be between 0V and –10V.

In low current applications, errors are dominated by noise and offset error in the REF102, the input bias current of the operational amplifier in the ACF2101, and the tolerance error of C_F.

The ACF2101 dual integrator was intended to operate in a unipolar mode and features low noise of 10µVrms, low 100fA bias current and a wide 120dB dynamic range. With the addition of a REF102 and a resistor, the device can also be operated in a bipolar mode.



I_{IN} (µA)	dt (µs)	V_{OUT} (V)
25	10	–10
12.5	10	–7.5V
0	10	–5
–12.5	10	–2.5V
–25	10	0

FIGURE 3. Using the ACF2101 with a Current Offset on the Input to Allow Bipolar Operation.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

BURR-BROWN®

APPLICATION BULLETIN

Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

COMPARISON OF NOISE PERFORMANCE BETWEEN A FET TRANSIMPEDANCE AMPLIFIER AND A SWITCHED INTEGRATOR

By Bonnie C. Baker

Low-input current FET operational amplifiers are universally used to monitor photodetector, or more commonly photodiode currents. These photodetectors bridge the gap between a physical event, light, and electronics. There are a variety of amplifier configurations to select from and the choice is based on noise, bandwidth, offset, and linearity. The most popular design approach is shown in Figure 1. A considerable amount has been written on the performance of this traditional transimpedance amplifier. This topology has dominated applications such as CT scanners, star-tracking instruments, electron microscopes, etc., where a light-to-voltage conversion is required.

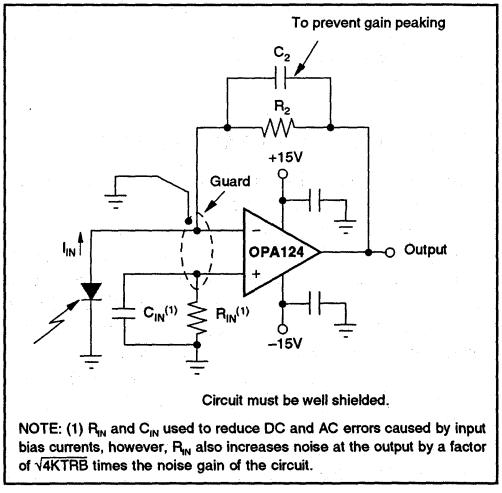


FIGURE 1. Most Popular Design Approach to Gain Precise Low Level Currents from a Photodetector.

Until now, the only feasible solution to the high precision, current-to-voltage design problem has been an op amp network with a resistor in the feedback loop. Variations such as using resistor T-networks or an instrumentation amplifier, as shown in Figure 2, still use the fundamental concept of a resistive feedback loop to perform the I/V conversion function. In these circuits, the fundamental transfer function is:

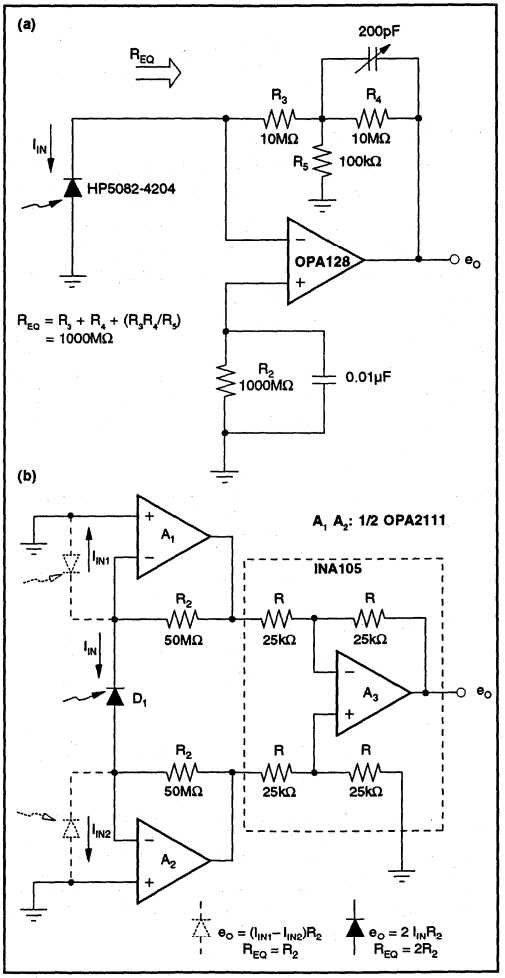


FIGURE 2 (a) Using a T-Network to Design the Feedback Resistor for a Transimpedance Circuit.
(b) An Instrumentation Amplifier Topology Can Be Used to Convert Low-Level Photodiode Currents to a Voltage Output.

$V_{OUT} = R_{EQ} \bullet I_{IN}$,
where V_{OUT} = Output voltage
R_{EQ} = Equivalent resistive feedback element
I_{IN} = Current generated by the photodetector

An alternative design method, a switched integrator, is shown in Figure 3. With this topology, the capacitor in the feedback loop of the amplifier dominates the transfer function. The switches perform the functions of removing the excitation signal from the input of the amplifier (S_1) and resetting the output of the amplifier to ground (S_2). The fundamental transfer function of this circuit is:

$$V_{OUT} = -\frac{1}{C_2}\int_0^t I_{IN}\, dt,$$

where V_{OUT} = Output voltage
C_2 = Capacitive feedback element
I_{IN} = Current generated by the photodetector

The discrete design of the switched integrator is impractical for low noise, precision applications because of the switching noise of S_1 and S_2. The switching noise is caused by the injection of charge across the parasitic gate-to-source, gate-to-drain, and source-to-drain capacitances of the FET switches. The ACF2101 (block diagram shown in Figure 3) implements the switched integrator design on a monolithic chip and uses a charge injection cancellation design for S_1 and S_2 (see Figure 4) to reduce the switch contribution to DC offset and noise.

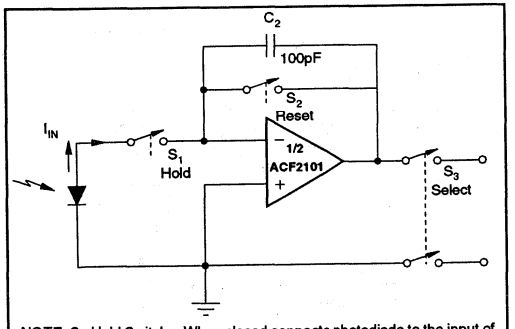


FIGURE 3. Block Diagram of 1/2 of the Dual ACF2101 Switched Integrator.

As illustrated in Figure 4, when the LOGIC node changes from low to high the voltage change (V_1) across the capacitors, C_A and C_B, pull charge out of the SIGNAL IN node and SIGNAL OUT node. The inverted LOGIC signal at V_2 pushes an equal amount of charge through C_C and C_D back into the SIGNAL IN node and SIGNAL OUT node. If

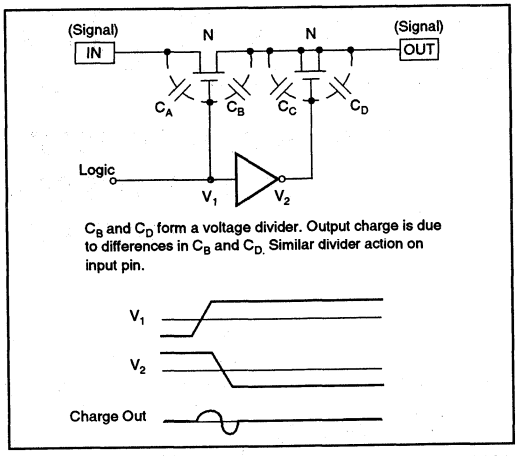


FIGURE 4. Topology Used for the Switches in the ACF2101 Switched Integrator to Reduce Charge Injection Errors.

parasitic capacitors C_A, C_B, C_C and C_D are carefully matched, the total charge injection caused by switching at the SIGNAL IN node and the SIGNAL OUT node is zero.

The comparison of the noise performance of the traditional resistor feedback transimpedance amplifier and the switched integrator starts with the analysis of the input sensor, the photodetector.

PHOTO DETECTOR CHARACTERISTICS

Photodiodes generate low level currents that are proportional to the level of illumination. An equivalent circuit for the photodiode is shown in Figure 5. The value of the junction capacitor, C_1, can have a wide range of values dependent of the diode junction area and bias voltage. A value of 50pF at zero bias is typical for small area diodes. The value of the shunt resistor, R_1, is usually in the order of $10^8\Omega$ at room temperature and decreases by a factor of two every 10°C rise in temperature. The range of the shunt resistor, R_1, can be as high as 100GΩ and low as 10kΩ at room temperature. There is no direct correlation between the values of C_1 and R_1. C_1 can usually be found in the product data sheet of the photodiode. The value of R_1 is not always published by the manufacturer, however, its effect on noise

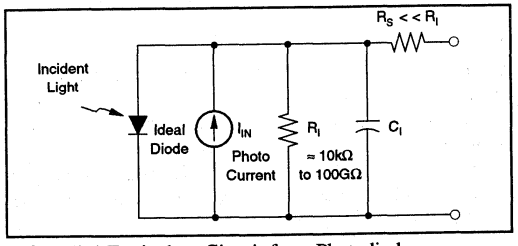


FIGURE 5. Equivalent Circuit for a Photodiode.

in both the traditional transimpedance amplifier and the switched integrator occur at lower frequencies. The overall noise contribution in the lower frequencies is usually very small compared to the contribution at higher frequencies, therefore, knowing the exact value of R_1 is not critical.

NOISE ANALYSIS OF TRADITIONAL TRANSIMPEDANCE AMPLIFIER

For the noise comparison between the transimpedance amplifier and the switched integrator refer to Figure 6 for a more complete circuit diagram. The optimum amplifier would have infinite bandwidth, zero voltage noise, zero input bias current, and zero offset voltage. The optimum amplifier does not exist; however, several op amps come close to meeting one or a few of these general requirements. Table I summarizes key specifications of the FET amplifiers OPA111, OPA124, OPA128, OPA404, OPA2111, OPA2107 and OPA627, which are usually used in transimpedance applications.

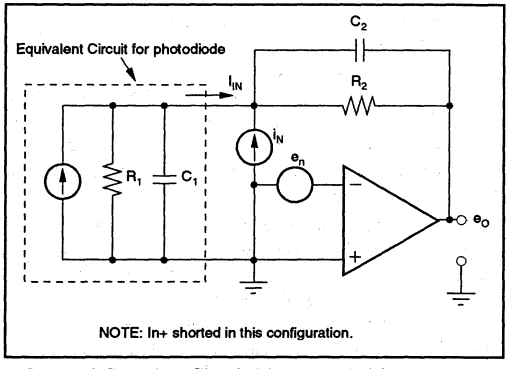


FIGURE 6. Complete Circuit Diagram Used for the Evaluation of the Noise and Bandwidth Performance of the Classical Transimpedance Amplifier and the Switched Integrator.

PRODUCT	NOISE at 10kHz (nV/√Hz)	BANDWIDTH (MHz, typ)	INPUT CAPACITANCE (pF, typ)	INPUT BIAS CURRENT (pA, max)
OPA111BM	8	2	4	1
OPA124BP	8	1.6	4	1
OPA627BP	6	16	15	5
OPA404G	12(1)	6.4	4	4
OPA128BM	15(1)	1	3	0.15
OPA2111BM	8	2	4	4
OPA2107BM	8(1)	4.5	6	5

NOTE: (1) Denotes typical values.

TABLE I. Low Noise FET Input Op Amps Typically Used In Transimpedance Amplifier Applications. In transimpedance applications, the input capacitance of the amplifier equals input common-mode capacitance plus input differential capacitance.

The first step in designing the transimpedance amplifier is selecting the feedback resistor, R_2. By knowing the maximum expected I_{IN}, R_2 is selected to optimize the signal-to-noise ratio with the formula:

$$R_2 = \frac{V_{OUT(max)}}{I_{IN(max)}},$$

where $V_{OUT(max)}$ = maximum output voltage of the op amp

$I_{IN(max)}$ = maximum current from the photodiode based on maximum expected light intensity

Typical values for R_2 would be between 10kΩ and 100MΩ. It is possible that optimum noise performance can be obtained with a $V_{OUT(max)}$ that is less than the full output swing of the amplifier, in which case the above equations are not applicable. The above equation is designed to optimize the signal-to-noise ratio at the output of the amplifier.

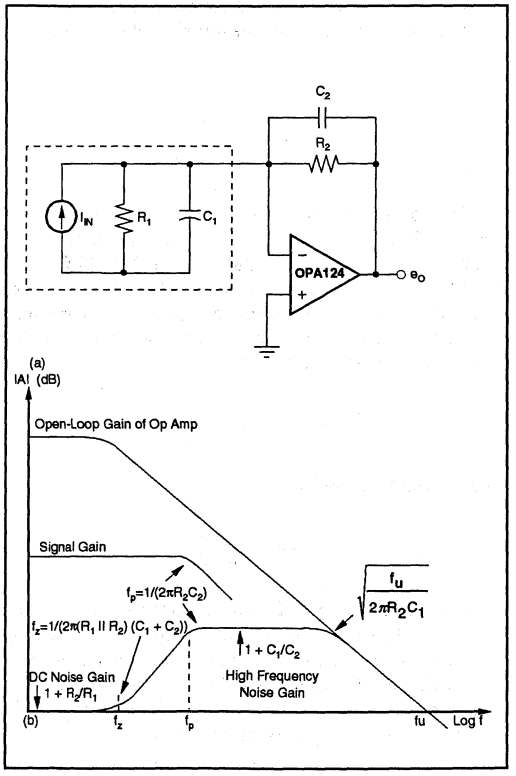


FIGURE 7. Noise And Signal Response of the Classical Transimpedance Amplifier.

The model in Figure 7 shows the overall noise gain response of the transimpedance circuit. The signal bandwidth is determined by a pole generated by R_2 and C_2. The noise bandwidth is determined by the open loop gain roll off of the op amp. To maximize the signal bandwidth and insure an approximate 45° phase margin with a 25% step function overshoot, C_2 is selected using the formula below:

$$C_2 = \sqrt{\frac{C_1}{2\pi R_2 \bullet f_u}}$$

where f_u = op amp unity gain bandwidth

Here the signal bandwidth and noise bandwidth are identical and equal to:

$$BW = \frac{1}{2\pi R_2 C_2}$$

In some applications, an overshoot of 25% may be too much. A more conservative 5% overshoot can be designed with a phase margin of 65° by using the formula below to select C_2:

$$C_2 = 2 \bullet \sqrt{\frac{C_1}{2\pi R_2 \bullet f_u}}$$

where f_u = op amp unity gain bandwidth

Typical calculated values for C_2 would be from sub-pico farads to 20 or 30pF. Actual minimum circuit values for C_2 are dependent on the stray capacitance of R_2 and PC board layout. Typically, a resistor has 0.5pF of stray capacitance. Using the C_2 value calculated above (for a 65° phase margin), the effective noise bandwidth is equivalent to the noise gain 3dB bandwidth times $\pi/2$ or:

$$BW_{\text{effective noise}} = \frac{1}{2R_2C_2}$$

and the signal bandwidth is:

$$BW_{\text{signal}} = \frac{1}{2\pi R_2 C_2}$$

Usually it is necessary to follow the transimpedance amplifier with a low pass filter to further reduce the wideband noise beyond the signal bandwidth. A single pole, low-pass filter with a bandwidth at twice the signal bandwidth of the transimpedance amplifier can easily improve the dynamic range of the transimpedance amplifier by 4 or 5 dB.

Brute force calculations should be performed to understand the noise contributions of the regions illustrated in Figure 7 (see OPA101 data sheet). For instance, R_1 contributes to overall noise gain in the lower frequencies and can be mostly ignored. This insight is valuable when considering design options to further improve the circuit. Once the details are understood, an easier approach is to use a macromodel and simulate the results. The macromodel must be able to simulate the noise performance of the op amp. The appropriate

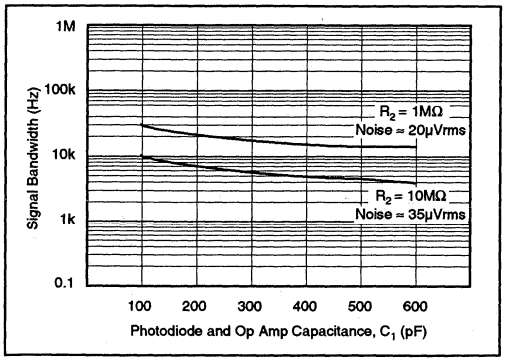


FIGURE 8. Signal Bandwidth and Output Noise Change With Changes in Input Capacitance, C_1, of a Transimpedance Amplifier Using the OPA111 as the Op Amp.

Burr-Brown macromodel for the OPA627 is the OPA627E.MOD. The PSpice Probe command needed to calculate the cumulative rms noise is SQRT(S(V(ONOISE) • V(ONOISE))). Figure 8 shows how a transimpedance amplifier's (designed using the OPA124) signal bandwidth and output noise change with values of input capacitance. Note that the output noise is unexpectedly flat across changes in C_1. This is because the signal and noise bandwidth decrease with increases of C_2. A lower noise bandwidth yields lower rms noise at the output of the amplifier. The signal-to-noise ratio improves.

To improve the signal-to-noise ratio of a transimpedance amplifier, the designer can select a lower noise amplifier, reduce the $(1+C_1/C_2)$ noise gain, reduce the feedback resistor value, or reduce the signal bandwidth of the system with an additional filter or a slower op amp. Lower noise FET amplifiers usually have a wider bandwidth and higher input capacitance than the higher noise FET amplifiers. If a lower noise, wider bandwidth amplifier is selected as the op amp for the transimpedance amplifier, the increase in bandwidth and input capacitance may cause more noise in the system than the original op amp. A filter can be used to reduce the overall bandwidth and reduce the noise. Additionally, the noise gain of the transimpedance amplifier can be reduced by increasing C_2 or decreasing C_1. The photodetector can be selected in order to reduce C_1. Sometimes this is not possible because of the design constraints of photodetector vs the signal source. C_2 can be increased at the expense of reduced bandwidth. More elaborate techniques can be used to reduce noise, such as a more complex feedback network around the amplifier or boot-strapping the photodetector. These techniques are beyond the scope of this application note. Refer to the reference articles for more depth.

One fundamental performance difference between the traditional transimpedance amplifier and the switched integrator is that the amplifier gives a real time representation of the light excitation at the output of the amplifier, and the switched integrator gives a time-averaged representation of

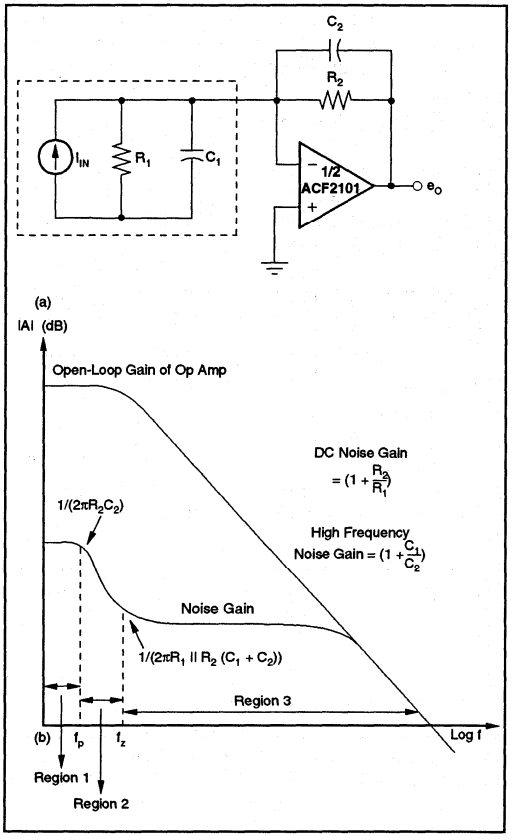


FIGURE 9. Noise and Signal Response of a Switched Integrator.

the input information from the photodetector. The real time solution is limited in bandwidth by the selected amplifier, the settling time of the amplifier, and the required feedback capacitor and resistor (C_2 and R_2). Additionally, a filter is usually used following the output of the transimpedance amplifier to further reduce noise at higher frequencies.

This approach is optimal for low and medium bandwidth applications where information about the amplitude and shape of the input signal is critical. The design problem is complex because of the trade-offs between noise and bandwidth and the abundance of op amp choices. Also, the capacitor and resistor accuracy requirements make this design difficult and sometimes expensive to manufacture in a production environment.

NOISE ANALYSIS OF SWITCHED INTEGRATOR AMPLIFIER

Where the traditional transimpedance transfer function is dominated by the feedback resistor, R_2, the switched integrator amplifier transfer function is dominated by the ratio of the feedback capacitor, C_2, and time. Referring to Figure 3, when S_1 is closed, the input current flows past the inverting node of the op amp (which is held at virtual ground) and charges C_2. The input current consequently causes the voltage at the output of the op amp to change in the negative direction over time. The voltage output of the switched integrator represents the average current input signal over a specified time, as opposed to the real time signal of the previous example. The ACF2101 switched integrator, shown in Figure 3, has a maximum input current specified at 100µA. The input current is restricted by the internal capacitor of the ACF2101 (100pF) and the 1V/µs slew rate of the amplifier. If an external capacitor is used, input currents can exceed 100µA as long as the following ratio is true:

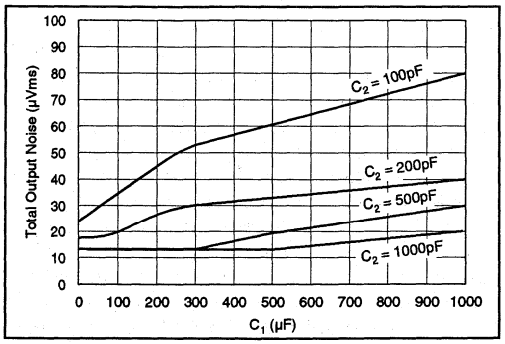


FIGURE 10. Total Output Noise vs C_1 and C_2 of the ACF2101 Switched Integrator.

$$\frac{C_2}{\text{(integration time)}} \geq 10^6 \text{ (farad/sec)}$$

where the integration time equals the amount of time between samples.

If that ratio is less than 10^6 (farad/sec), the ACF2101 may loose accuracy at the output. Whenever possible, the internal capacitor should be used with the ACF2101 to insure greater gain and linearity accuracy. Figure 9 is used to evaluate the noise contribution of the op amp, gained by the feedback network of the ACF2101 and the photodiode. Here the reset switch, (S_2 as illustrated in Figure 3) is modeled as a noiseless resistor (R_2). The typical resistance of S_2, when it is open, is 1000GΩ. The switched integrator, ACF2101, has an internal feedback capacitor, C_2, of 100pF. The user may choose to use an external capacitor instead of the internal capacitor provided. Typical values can range up to 2000pF. If an external capacitor is used, care must be taken to choose an integration capacitor with a low voltage coefficient, temperature coefficient, memory, and leakage current. Suitable types include NPO ceramic, polycarbonate, polystyrene, and silver mica.

The total noise contribution of the op amp and the feedback network of the switched integrator is equivalent to the

square root of the sum of the squares of three regions as shown in Figure 9. The noise in the first region is equal to the average op amp noise over that region times the square root of the region bandwidth. The pole in the noise gain of the switched integrator circuit generated by R_2 and C_2 is in the sub-Hertz region. For example, if C_2 = 100pF and R_2 = 1000GΩ the pole generated by the RC pair is equal to 1.59mHz. To calculate the noise contribution of this region the average noise over the region is multiplied times the square root of 1.59mHz which is equal to $39.87E^{-3}$. Quick calculations show that any noise gained by the DC gain $(1+R_2/R_1)$ of the switched integrator is negligible. In addition, the zero generated by the $(R_1 \parallel R_2)(C_1+C_2)$ combination is also in the low frequency range. Using a typical value of 100MΩ for R_1, 50pF for C_1, 1000GΩ for R_2 and 100pF for C_2, the zero is located at 10.6Hz. Again, the noise contribution from this region is negligible. Consequently, the noise contribution from the op amp and its feedback network in conjunction with the photodiode is dominated by the op amp noise times $(1 + C_1/C_2)$.

In addition to the gained op amp noise mentioned above, charge injection and $^{KT}/_{C}$ (capacitor noise) also contribute to the total noise figure of the switched integrator. The switch network shown in Figure 4 is used for the switches of the ACF2101 to reduce charge injection noise. Figure 10 illustrates the total output noise of the switched integrator with various C_1 and C_2 values.

The ACF2101 switched integrator is a sampled system controlled by the sampling frequency (f_S), which is usually dominated by the integration time. The fastest feasible sampling frequency for the ACF2101 is 42.55kHz. This assumes that the internal capacitor (100pF) is used. The full scale output is –10V and the settling time requirements are to 0.01% accuracy. Input signals should be below the Nyquist frequency ($f_S/2$) to avoid aliasing errors. The bandwidth of the ACF2101 is determined by the slew rate of the amplifier, settling times of the reset (S_2) and select (S_3) switches as well as the on-to-off and off-to-on switching speeds. The slew rate of the amplifier is guaranteed a minimum of 1V/µs. The output node requires at least 10µs to reach full scale. This time restraint can be reduced if the full 10V swing capability of the ACF2101 is not used.

The settling time of the reset switch (S_2) is 5µs to 0.01% accuracy, which is limited by slew rate of the amplifier and the $R_2 \parallel C_2$ time constant. The reset switch settling time increases with larger values of C_2; however, if the user also reduces the full scale signal output as described above, this time is reduced proportionally to the output swing maximum. The select switch (S_3) has a 2µs settling time to 0.01% accuracy for loads ≤ 100pF and the delay between switching should be about 0.5µs.

The signal-to-noise ratio of the switched integrator can be reduced by selecting a higher value integration capacitor, C_2. The switched integrator is limited in bandwidth by the amplifier and the nature of the transfer function. The output signal of the integrator is time averaged. The sampling frequency is restricted by the size of the integrating capacitor, the slew rate of the amplifier, the settling time of the switches and amplifier. The bandwidth of the switched integrator can be improved by decreasing the integration capacitor, C_2. As shown in Figure 11, the settling time of the reset switch is increased with increases in C_2.

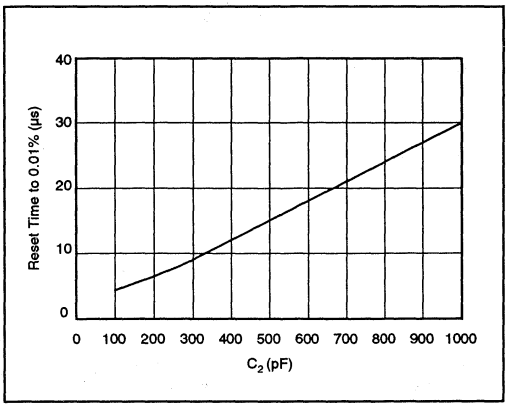


FIGURE 11. Reset Time C_2 vs the ACF2101 Switched Integrator.

The switched integrator requires external digital support circuitry to drive the hold, reset and select switches. If an external integration capacitor (C_2) is used, gain accuracy can be compromised due to the accuracy of the capacitor. The select switch allows the user of the ACF2101 switched integrator to eliminate a sample hold amplifier.

COMPARING THE TRADITIONAL TRANSIMPEDANCE AMPLIFIER TO THE SWITCHED INTEGRATOR

Two examples are selected for comparison of the transimpedance amplifier and the switched integrator amplifier. In both examples, optimum noise solutions and optimum bandwidth solutions are considered.

	OPTIMUM NOISE PERFORMANCE		OPTIMUM BANDWIDTH PERFORMANCE	
	TRANS-IMPEDANCE	SWITCHED INTEGRATOR	TRANS-IMPEDANCE	SWITCHED INTEGRATOR
Device	OPA124	ACF2101	OPA627	ACF2101
I_B	1pA	1pA	5pA	1pA
C_2	0.5pF	100pF	0.5pF	1.5pF
Signal Bandwidth	3.2kHz	50Hz	3.2kHz	3.35kHz
Noise Bandwidth	5kHz	250kHz	79kHz	250kHz
Noise	200µVrms	35µVrms	400µVrms	100µVrms
SNR	94dB	109dB	88dB	100dB

TABLE II. Transimpedance and Switched Integrator Design Comparison Using a 100pF Photodiode with Maximum Output Current of 100nA. Values of R_2 were calculated assuming a 65° phase margin.

The first design problem uses an average sized photo diode (C_1 = 100pF) with a maximum output current of 100nA. As shown in Table II, the OPA124 was selected for the low noise comparison and the OPA627 was selected for the wide-bandwidth comparison. The fullscale output of the transimpedance amplifier is designed to be –10V. R_2 is selected to be 100MΩ. C_2 of the OPA124 low noise circuit is restricted by the parasitic capacitance of the feedback resistor, 0.5pF. The OPA124 has a maximum input bias current of 1pA, low drift of 1μV/°C, and low offset voltage. The signal-to-noise ratio of this design is 94dB with a signal bandwidth of 3.2kHz.

In contrast, the ACF2101 is configured to minimize noise by using the on-chip capacitor C_2 = 100pF. As shown in Figure 10, the rms noise performance is typically 35μVrms. This noise performance can be improved by using a higher value external capacitor, but, the bandwidth performance of the circuit is compromised. The signal-to-noise ratio of the switched integrator is better than the transimpedance configuration at 109dB, but the bandwidth is only 50Hz.

In the second section of Table II, the two circuits are optimized for bandwidth. Here the OPA627 is selected as the preferred op amp in hopes of improving the bandwidth of the transimpedance amplifier. The transimpedance design using the OPA627 does indeed change the bandwidth of the circuit, but in an undesirable way. C_2 is still limited to 0.5pF because of the stray capacitance of R_2, consequently the signal bandwidth does not change from the OPA124 design. The noise bandwidth, however, does change by a factor of ~16, causing a significant increase in noise. The signal-to-noise ratio of this circuit is 88dB. The designer would be better off using the OPA124 as the amplifier instead of the OPA627 for this application.

In contrast, the ACF2101 is also configured to maximize bandwidth. Here a feedback capacitor of 1.5pF is selected. PC board layout precautions should be taken to reduce stray capacitance. The signal bandwidth of the circuit is designed to 3.35kHz with a signal-to-noise ratio of 100dB. In this example, the noise and bandwidth performance of the ACF2101 switched integrator is better than the transimpedance configuration. The ACF2101 switched integrator is best optimized for low input current, high input capacitance applications.

Table III illustrates the second design problem where the photodiode has the same stray capacitance (C_1) of 100pF but a maximum current signal of 100μA. The OPA124 is selected for the low noise transimpedance amplifier. In this case, R_2 is selected to be 100kΩ and C_2 equal to 18.2pF. The noise performance of this amplifier is 31μVrms with a signal-to-noise ratio of 110dB.

	OPTIMUM NOISE PERFORMANCE		OPTIMUM BANDWIDTH PERFORMANCE	
	TRANS-IMPEDANCE	SWITCHED INTEGRATOR	TRANS-IMPEDANCE	SWITCHED INTEGRATOR
Device	OPA124	ACF2101	OPA627	ACF2101
I_B	1pA	1pA	5pA	1pA
C_2	18.2pF	500pF	6.76pF	210pF
Signal Bandwidth	87kHz	10kHz	235kHz	24kHz
Noise Bandwidth	275kHz	250kHz	740kHz	250kHz
Noise	31μVrms	15μVrms	108μVrms	20μVrms
SNR	110dB	116dB	99dB	114dB

TABLE III. Transimpedance and Switched Integrator Design Comparison Using a 100pF Photodiode With Maximum Output Current of 100μA. Values of R_2 were calculated assuming a 65° phase margin.

The switched integrator is designed with C_2 = 500pF (external capacitor). A larger capacitor is used to improve the noise performance of the circuit. The noise performance of the switched integrator is improved over the transimpedance amplifier, yet the bandwidth is considerably smaller.

The bandwidth and noise performance of the transimpedance amplifier can be improved by using the OPA627 in place of the OPA124. As shown in Table III, the signal bandwidth is nearly tripled. On the other hand, the switched integrator is designed for improved bandwidth performance by decreasing C_2 to equal 210pF. Although the noise performance is better than the transimpedance amplifier, the bandwidth is restricted by the slew rate, settling times, and switching times of the switched integrator.

IN CONCLUSION

This application note has taken a look at a few variables that optimize the performance of circuits that amplify photodiode signals. In addition to the solutions presented, alternatives should also be explored before the final design is released to production.

REFERENCES

OPA101 Product Data Sheet, Burr-Brown PDS-434.

Graeme, Jerald, "FET Op Amps Convert Photodiode Outputs to Usable Signals", EDN, October 29, 1987.

ACF2101 Product Data Sheet, Burr-Brown PDS-1078.

Graeme, Jerald, "Circuit Options Boost Photodiode Bandwidth", EDN, May 21, 1992.

Graeme, Jerald, "Phase Compensation Optimizes Photodiode Bandwidth", EDN, May 7, 1992.

BURR-BROWN® APPLICATION BULLETIN

Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

MTTF, FAILRATE, RELIABILITY AND LIFE TESTING

by Bob Seymour

At Burr-Brown, we characterize and qualify the reliability of our devices through high temperature life testing. The results of this testing are quantified with such values as MTTF and failure rate. This information can be very valuable when used for comparative purposes or applied to reliability calculations. However, this information loses its worth if it is not precisely understood and appropriately employed. It is the intent of this application note to bring together, in a concise format, the definitions, ideas, and justifications behind these reliability concepts in order to provide the background details necessary for full and correct utilization of our life testing results.

SOME PRELIMINARY DEFINITIONS

Reliability is "the probability that a part will last at least a specified time under specified experimental conditions"[1].

MTTF is the mean time to the first failure under specified experimental conditions. It is calculated by dividing the total number of device • hours by the number of failures. It is important to note, at this time, that the dimensions of MTTF are not hours per failure, but rather, device • hours per failure. If each part has a 0.1% chance of failure before 1 hour then 10 parts have a 1% chance experiencing a failure by that time. The MTTF will be the same in both cases. 1 failure in 10 hours on 1 part or 1 failure in 1 hour on 10 parts both produce an MTTF of 10 device • hours.

Failure rate is the conditional probability that a device will fail per unit of time. The conditional probability is the probability that a device will fail during a certain interval given that it survived at the start of the interval.[5] When failure rate is used to describe the frequency with which failures are expected to occur, the time units are typically device • hours.

FITS is simply failure rate scaled from failures per device • hour to failures per billion device • hours.

ON TO THE DETAILS

In the definition section MTTF is defined as the average time, in device • hours, per failure observed under specific experimental conditions such as a life test. Here at Burr-Brown we use a slightly modified formula for MTTF. We calculate 2 times the total device • hours, T_{dh}, divided by the upper 60% confidence limit of a chi-square distribution with 2 times the observed number of failures + 2 degrees of freedom, $X^2(2f + 2)$. Our formula is

$$MTTF = \frac{2T_{dh}}{\chi^2(2f+2)}$$

Since both time and failures are doubled, these definitions are roughly equivalent. Some explanation is in order.

If multiple life tests are run on the same type of device, it is unlikely that all tests will have the same number of failures for the same number of device • hours. Rather there will be a distribution of failures. The minimum value must be 0 for no failures. The maximum value could correspond to 100% failures, but we can presume that we are running enough parts that this will not happen. Rather the distribution will taper off as the number of failures increases. Somewhere in between there will be a concentration of failures.

The chi-square calculation provides us with a tool for adjusting the actual number of failures from a limited life test to make it more accurately reflect what we might expect from the population as a whole. For example, applying a confidence level of 60% to a chi-square distribution with 8 degrees of freedom will return a value into the denominator of the MTTF calculation which is greater than or equal to 60% of the values in a chi-square distribution with a mean of 8.

One intuitive interpretation of the chi-square calculation is that the calculated value represents, roughly, a number of failures which will be greater than 60% of the failures we might get during multiple life tests. The upper 60% level is selected because it represents an approximately average estimate for MTTF and because it is widely accepted among semiconductor manufacturers and users. This method of estimating MTTF does not prevent further reliability calculations from being made at more conservative levels.

One more point remains to be explained regarding this calculation. Why do we use 2 (# failures) +2? The technical explanation for this is given later in this paper. Briefly, the factor of 2 is necessary to achieve theoretical validity of the X^2 distribution. Given the factor of 2, it can be seen that we are merely adding 1 failure to the actual number of failures. The added failure appears in the calculation as if a failure occurred at the end of the test. This assures that the test terminates with a failure, also a theoretical requirement, as well as allows calculation of MTTF even if no failures were observed.

The MTTF value by itself really only serves for comparison purposes. Many more factors need to be considered before predictive statements regarding the longevity of our components can be made. The statistical concepts of reliability and failrate allow us to make such predictions. I will present here, with justification yet to come, the statistical formulas which quantify these concepts.

Let reliability be represented by R(t) and failure rate by Z(t).

Then $$R(t) = e^{-\alpha t^{\beta}}$$

and $$Z(t) = \alpha\beta t^{\beta-1}$$

Remember, reliability is the probability that a part will function at least a specified time. Failure rate describes the frequency with which failures can be expected to occur. By examining failure rate we can make important statements about the life cycle of the product.

The life cycle of a part can be thought of as having three distinct periods: infant mortality, useful life, and wear-out. These three periods are characterized mathematically by a decreasing failure rate, a constant failure rate, and an increasing failure rate. This theory is the basis of the ubiquitously discussed "bathtub curve".

The listed formulas can model all three of these phases by appropriate selection of α and β. β affects the shape of the failure rate and reliability distributions. When $\beta < 1$ Z(t) becomes a decreasing function. $\beta = 1$ provides a constant failure rate. An increasing failure rate can be modeled with $\beta > 1$. Therefore, β can be selected to accurately model the shape of an empirically known failure rate (or of the original probability density function of T which defines the failure rate). The constant α provides the scaling factor.

Given good design, debugging, and thorough testing of product the infant mortality period of a part's life should be past by the time the parts are shipped. This allows us to make the assumption that most field failures occur during the useful life phase, and result, not from a systematic defect, but rather from random causes which have a constant failure rate. The constant failure rate presumption results in $\beta = 1$. Thus

$$Z(t) = \alpha$$

The concept of a constant failure rate says that failures can be expected to occur at equal intervals of time. Under these conditions, the mean time to the first failure, the mean time between failures, and the average life time are all equal. Thus, the failure rate in failures per device • hour, is simply the reciprocal of the number of device • hours per failure. That is

$$Z(t) = \alpha \approx 1/\text{MTTF}$$

during constant failure rate conditions.

Note that MTTF is always the number of device • hours per failure but neither failure rate nor α is always 1/MTTF.

FORMAL DERIVATIONS AND JUSTIFICATIONS

OK, it's time for some real details. Virtually all of the information on the Weibull distribution comes from *"Probability and Statistics for Engineers and Scientists"* by Ronald E. Walpole and Raymond H. Myers, copyright 1985, Macmillan Publishing Company. Much of the information in the section on MTTF is extrapolated from the lectures of Dr. Duane Dietrich, professor of Systems and Industrial Engineering at the University of Arizona. My apologies to Dr. Dietrich for any distortions.

Let's start by hypothetically running a huge life test long enough to drive all devices to failure, recording time-to-failure for each part, generating histograms, calculating MTTF, etc. A histogram of time-to-failure would be useful. Its shape is unknown and unimportant at this time. Given the hypothetical nature of the experiment, we can presume that the distribution is representative of the whole population.

From this distribution, we can describe reliability as

$$R(t) = P(T > t)$$

where T represents time-to-failure and t represents time. Note that this is merely an exact restatement of the verbal definition already presented.

Another useful function which can be derived from the time-to-failure histogram will represent the cumulative probability of failure at any time t. Let F(t) represent this function. Then

$$F(t) = P(T < t)$$

or

$$F(t) = 1 - R(t)$$

Now we are positioned to examine failure rate. Failure rate is the conditional probability that a device will fail during a certain interval, given that it survived to the start of that interval, per unit of time. Let Z(t) represent failure rate. Then

$$Z(t) = \lim_{\delta t \to 0} \frac{F(t+\delta t) - F(t)}{R(t)\delta t}$$

Now note that

$$\lim_{\delta t \to 0} \frac{F(t+\delta t) - F(t)}{\delta t}$$

is the derivative of F(t). Also $F(t) = 1 - R(t)$. Therefore, $dF(t)/dt = -dR(t)/dt$. Thus

$$Z(t) = \frac{dF(t)}{R(t)dt}$$

$$= \frac{-dR(t)}{R(t)dt}$$

$$= \frac{-d[\ell n\, R(t)]}{dt}$$

Integrating both sides results in

$$\ell n\, R(t) = -\int Z(t)dt + \ell n\, c$$

giving

$$R(t) = c\, e^{-\int Z(t)dt}$$

as the relationship between reliability and failure rate based only on the original definitions. The constant, c, must satisfy the initial condition that all parts are assumed to be functional at time t = 0 or R(0) = 1.

ENTER WALODDI WEIBULL

The statistical distribution introduced by Waloddi Weibull in 1939 provides the mechanism to make our reliability function usable. For x > 0 the distribution is given by

$$f(x) = \alpha\beta x^{\beta-1} e^{-ax^{\beta}}$$

where $\alpha > 0$ and $\beta > 0$.

Let us presume that the original probability density distribution of T (time-to-failure) is describable using the Weibull distribution. Then

$$R(t) = 1 - F(t) = 1 - \int_0^t \alpha\beta x^{\beta-1} e^{-\alpha x^{\beta}} dx$$

$$R(t) = 1 + \int_0^t de^{-\alpha x^{\beta}}$$

$$R(t) = e^{-\alpha t^{\beta}} \text{ (see appendix A)}$$

and

$$Z(t) = \frac{-dR(t)}{R(t)dt} = \frac{\alpha\beta t^{\beta-1} e^{-\alpha t^{\beta}}}{e^{-\alpha t^{\beta}}}$$

$$Z(t) = \alpha\beta t^{\beta-1}$$

Thus, the Weibull distribution provides usable mathematical descriptions of reliability and failure rate:

$$R(t) = e^{-\alpha t^{\beta}}$$

$$Z(t) = \alpha\beta t^{\beta-1}$$

But do these agree with our formulas derives strictly without presuming the Weibull distribution? This definition of Z (t) can be entered into our previous derivation to justify our assumption.

$$R(t) = c\, e^{-\int Z(t)dt}$$

$$R(t) = c\, e^{-\int \alpha\beta t^{\beta-1} dt}$$

$$R(t) = c\, e^{-\alpha t^{\beta}}$$

For R (0) = 1 then c = 1 and

$$R(t) = e^{-\alpha t^{\beta}}$$

as before. Thus, the Weibull distribution fits our original definitions, provides a solution to the original equations, and results in useful formulas for reliability and failure rate.

More on constant failrate and MTTF.

We presume constant failrate conditions during our life test evaluations. It is particularly important to understand this condition well. What are constant failrate conditions? How do they affect the Weibull equations? And what, exactly, is MTTF?

During the useful life period of our parts, there are no systematic defects or problems causing a high early failure rate nor an increasing rate of failure associated with aging. Failures during this period result from random causes. The probability of a part failing for a random defect or stress does not change as the part ages. The failure rate, the conditional probability that a part will fail at a specific time, T, given that it has survived to that time, is constant.

From the Weibull distribution, the general equation for failure rate is given by

$$Z(t) = \alpha\beta t^{\beta-1}$$

Given that Z(t) must equal a constant then b must equal 1 to drive the time variable t to unity. Thus, under constant failure rate conditions, the equations for failure rate, reliability and the Weibull distribution, become, respectively

$$Z(t) = \alpha$$

$$R(t) = e^{-\alpha t}$$

and

$$f(t) = \alpha e^{-\alpha t}$$

The function f(t) is the time-to-failure probability density function. It gives the probability that a part will fail at any given time t. The mean, or expected value, of f(t) is the average time-to-failure. This mean value is equal to $1/\alpha$. The problem is that we do no know the true value of $1/\alpha$. This value must be estimated from experimental data.

An estimator for $1/\alpha$ can be derived using the maximum likelihood method with the function f(t). Suppose we run a life test starting with N parts and experience r failures. The joint probability density function describing the life test results is given by the product of the probabilities that each failure occurred when it did. Referring to this p.d.f. as L (α, t) then

$$L(\alpha, t) = \alpha^r e^{-\alpha \sum_{i=1}^{r} t_i}$$

Implicit in this derivation is that the life test is terminated at the r^{th} failure and the dimension of t is device • hours. Our method of evaluating MTTF involves adding 1 failure to the observed failures. This assures the requirement for termination on the r^{th} failure is satisfied as well as allows calculation of MTTF even if no actual failures occur. The dimensioning of t as device • hours accounts for the test time of those parts that did not fail.

To find an appropriate estimator for $1/\alpha$ by the maximum likelihood method, we find the value of α which maximizes the function L (α, t). We are, in effect, finding the value of

α which maximizes the probability of observing what was actually observed. This is accomplished by taking the partial derivative of the $\log_e$ of L (α, t), setting it equal to zero, and solving for α:

$$\ell n\,(L(\alpha,t)) = r\ell n\,(\alpha) - \alpha\sum_{i=1}^{r} t_i$$

$$\frac{\partial \ell n\,(L(\alpha,t))}{\partial \alpha} = \frac{r}{\alpha} - \sum_{i=1}^{r} t_i$$

$$\frac{r}{\tilde{\alpha}} - \sum_{i=1}^{r} t_i = 0$$

using $\tilde{\alpha}$ to indicate the approximation,

$$\frac{1}{\tilde{\alpha}} = \frac{\sum_{i=1}^{r} t_i}{r}$$

This equation shows that $1/\alpha$ can be estimated by dividing the accumulated test time for all of the tested devices by the total number of failures. This agrees with the original definition of MTTF.

Understanding the chi-square, X^2, confidence interval calculation requires recognition that given the random variable for time-to-failure, T, has distribution

$$f(t) = \alpha e^{-\alpha t}$$

then the random variable V described by

$$V = 2\alpha\sum_{i=1}^{r} t_i$$

is distributed X^2 with 2r degrees of freedom, $X^2(2r)$. Therefore, for a specified confidence level ç

$$2\alpha\sum_{i=1}^{r} t_i > X^2(2r,\zeta)$$

and the upper confidence limit for MTTF becomes

$$\frac{1}{\alpha} < \frac{2\sum_{i=1}^{r} t_i}{\chi^2(2r,\zeta)} = \text{MTTF}$$

which, with r equal to the number of observed failures + 1, is the actual formula we use for MTTF.

To justify the X^2 distribution of the random variable V used above, apply the transformation of variable

$$V' = 2\alpha T, \frac{dT}{dV'} = \frac{1}{2\alpha}$$

to f(t) which results in

$$f(v) = \alpha e^{-\alpha\frac{V}{2\alpha}}\frac{1}{2\alpha} = \frac{1}{2}e^{-\frac{V}{2}}$$

which is distributed X^2 with 2 degrees of freedom, $X^{2(2)}$ (see Appendix B).

Now note that

$$2\alpha\sum_{i=1}^{r} t_i = 2\alpha t_1 + 2\alpha t_2 + \ldots + 2\alpha t_r$$

As shown, each factor of the above sum is distributed $X^{2(2)}$. Therefore, by the reproductive property of X^2 the summation is also distributed X^2 with r times 2 degrees of freedom, X^2 (2r) as stated.

AND FINALLY

The concepts of MTTF, failure rate and reliability have been defined, discussed and justified. In general, the time units of device • hours have been used. With this dimension, failure rate can be interpreted as the frequency with which failures can be expected to occur. This description works well with the experimental estimation of the unknown parameters and provides an intuitive perspective. However, reliability estimation is, in essence, a probabilistic science and the Weibull equations are, in essence, probability equations. As a probability equation, failure rate becomes the probability of failure per hour, not per device • hour. The reader is encouraged to give this distinction some thought.

We perform our life testing at elevated temperatures in order to accelerate failure mechanisms which might result in device failure. Our reliability reports generally supply MTTF estimates scaled over a range of temperatures appropriate to application environments. The Arehnius equation with an activation energy selected to represent typical failure mechanisms is employed to generate the tables.

Here at Burr-Brown we use a spreadsheet program to calculate and record the results of life tests. Constant failure rate is presumed. This presumption should always be verified. It may not be unreasonable to interpret MTTF as the mean time to the first failure even if the failure rate is not constant. However, failure rate and reliability predictions based on that MTTF will be wrong.

APPENDIX A

$$\begin{aligned} d\exp(-\alpha x^{\beta})/dx &= \exp(-\alpha x^{\beta})\, d(-\alpha x^{\beta})/dx \\ &= \exp(-\alpha x^{\beta})(-\alpha\beta)(x^{\beta-1}) \\ &= -\alpha\beta x^{\beta-1}\exp(-\alpha x^{\beta}) \end{aligned}$$

therefore replacing

$$\begin{aligned} -\int_0^t \alpha\beta x^{\beta-1}\exp(-\alpha x^{\beta})\,dx &= -\int_0^t d\exp(-\alpha x^{\beta})/dx\,dx \\ &= -\int_0^t d\exp(-\alpha x^{\beta}) \end{aligned}$$

and

$$\begin{aligned} R(t) &= 1 + \int_0^t d\exp(-\alpha x^{\beta}) \\ &= 1 + \exp(-\alpha x^{\beta})\Big|_0^t \\ &= 1 + \exp(-\alpha t^{\beta}) - 1 \end{aligned}$$

APPENDIX B

The chi-square distribution with r degrees of freedom is given by

$$f(v) = \frac{1}{2^{\frac{r}{2}}\Gamma\left(\frac{r}{2}\right)} v^{\frac{r}{2}-1} e^{-\frac{v}{2}}$$

Setting r = 2 for $X^{2(2)}$ results in

$$\frac{1}{2^{\frac{2}{2}}\Gamma\left(\frac{2}{2}\right)} v^{\frac{2}{2}-1} e^{-\frac{v}{2}} = \frac{1}{2} e^{-\frac{v}{2}}$$

as indicated.

REFERENCES

(1) Walpole, Ronald E., and Myers, Raymond H., *"Probability and Statistics for Engineers and Scientists,"* Macmillan Publishing Company, 1985.

(2) Box, Hunter, and Hunter, *"Statistics for Experimenters,"* John Wiley & Sons, Inc., 1978.

(3) Besterfield, Dale H., *"Quality Control"*, Prentice-Hall, 1986.

(4) Kececioglu, P.E., Dr. Dimitri, *"Reliability Engineering Principles and Benefits with Applications,"* the lecture notes of Dr. Dimitri Kececioglu, P.E.; 1981.

(5) Lawless, J.F., *"Statistical Models and Methods for Lifetime Data,"* John Wiley & Sons, Inc., 1982.

BURR-BROWN®
APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

OPT201 PHOTODIODE-AMPLIFIER REJECTS AMBIENT LIGHT

by Mark Stitt and Wally Meinel (602) 746-7162

Many applications call for the measurement of a light signal in the presence of ambient background light. Sometimes the photodiode can be optically shielded from background light to eliminate unwanted signals. Another way to solve the problem is to combine a photodiode-amplifier like the OPT201 with a DC restoration circuit to reject low-frequency background light signals.

The circuit for a photodiode amplifier with DC restoration is shown in Figure 1. The circuit uses the OPT201 integrated photodiode and amplifier and an external op amp for DC restoration. The OPT201 combines a large 0.090 x 0.090 inch photodiode and high-performance transimpedance amplifier on a single chip. This combination eliminates the problems commonly encountered in discrete designs such as leakage current errors, noise pick-up, and gain peaking due to stray capacitance.

The DC restoration circuit consists of a non-inverting integrator driving the OPT201 transimpedance amplifier summing junction through a 100kΩ resistor, R_3. The current through R_3 cancels the current from the photodiode at signal frequencies below the pole frequency of the integrator to drive the output of the OPT201 to 0V. The pole-frequency of the integrator is set by R_2 and C_2.

Integrator Pole Frequency

$$f_{-3dB} = \frac{1M}{R_3(2 \cdot \pi \cdot R_2 \cdot C_2)}$$

The component values shown in Figure 1 set the low-frequency cutoff pole at 16Hz. Because of the long time constant, it may take over a second for the OPT201 output to come out of saturation when the circuit is first powered-up.

A non-inverting integrator requires a matching pole. The matching pole, set by R_1 and C_1, prevents the OPT201 output signals above the pole frequency from feeding directly back into the summing junction of the OPT201. Matching of the poles in not critical—±30% tolerance is adequate for most applications.

The value used for R_3 depends on the amplitude of the background light. With 10V output on A_1, the 100kΩ resistor can provide 100µA restoration current to the OPT201. This is ten times the photodiode current that would otherwise drive the OPT201 to 10V output when using the internal 1MΩ resistor. The DC restoration circuit can remove a background signal many times larger than the ac signal of interest providing the increased signal-to-noise level critical in many applications. Reducing the value of R_3 will increase the DC restoration range, but will also increase the noise gain of the transimpedance amplifier. Reducing R_3 to 10kΩ would increase noise from 130µVrms to 650µVrms. Values above 100kΩ for R_3 will not substantially reduce noise.

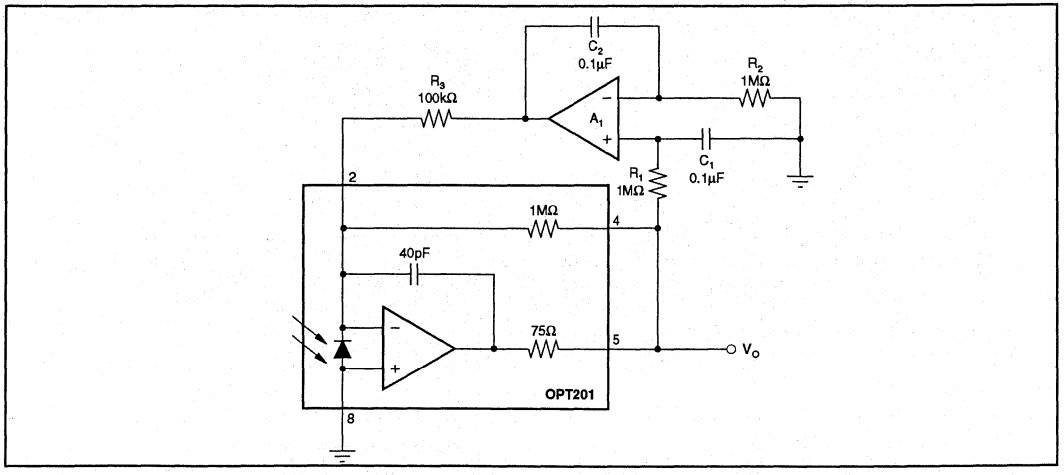


FIGURE 1. Photodiode-Amplifier with DC Restoration Rejects Unwanted Background Light.

BURR-BROWN®

APPLICATION BULLETIN

Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

IMPLEMENTATION AND APPLICATIONS OF CURRENT SOURCES AND CURRENT RECEIVERS

This application guide is intended as a source book for the design and application of:

- Current sources
- Current sinks
- Floating current sources
- Voltage-to-current converters (transconductance amplifiers)
- Current-to-current converters (current mirrors)
- Current-to-voltage converters (transimpedance amplifiers)

This is not an exhaustive collection of circuits, but a compendium of preferred ones. Where appropriate, suggested part numbers and component values are given. Where added components may be needed for stability, they are shown. Experienced designers may elect to omit these components in some applications, but less seasoned practitioners will be able to put together a working circuit free from the frustration of how to make it stable.

The applications shown are intended to inspire the imagination of designers who will move beyond the scope of this work.

R. Mark Stitt (602) 746-7445

CONTENTS

DESIGN OF FIXED CURRENT SOURCES

REF200 IC CURRENT SOURCE DESCRIPTION

The REF200 dual current source has two current sources plus a current mirror in an 8-pin plastic DIP (Figure 1). Because the circuit is fabricated with the Burr-Brown dielectrically isolated ***Difet***® Burr-Brown process, the three circuit blocks are completely independent. No power supply connections are needed to the chip. Just apply 2.5V or more to a current source for a constant 100µA output. Typical drift is less than 25ppm/°C and output impedance exceeds 500MΩ.

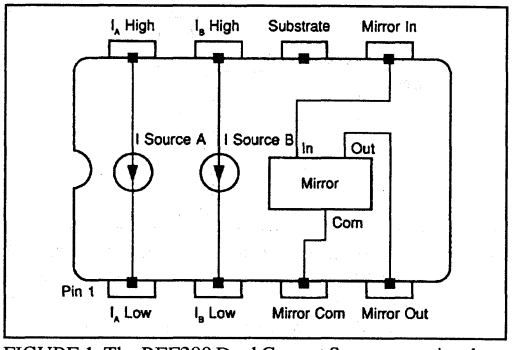


FIGURE 1. The REF200 Dual Current Source contains three completely independent circuit blocks—two 100µA current sources, and a current mirror.

The current mirror is useful in many applications. It uses a "full Wilson" type architecture as shown in Figure 2, with laser-trimming to ensure high accuracy.

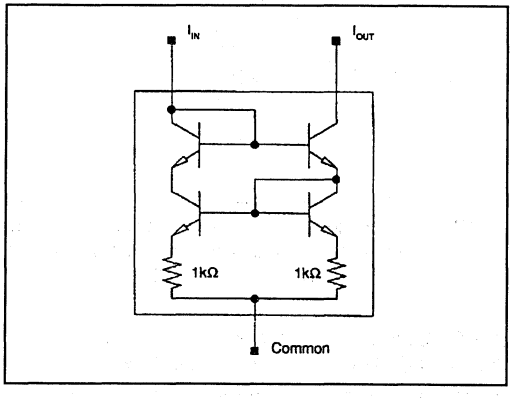


FIGURE 2. The REF200 Current Mirror uses a "full Wilson" architecture for high accuracy.

Each of the two current sources are designed as shown in Figure 3. Zero temperature coefficient (TC) is achieved by combining positive TC currents with a negative TC current. The positive TC currents are generated by a bandgap cell.

Current mirror Q_1– Q_2 forces equal currents to flow in 8/1 emitter ratioed devices Q_7 and Q_8. The proportional to absolute temperature (PTAT) voltage difference between the emitters—(k • t/q) • ln(8)—is forced across the 4kΩ resistor resulting in a PTAT current of about 13µA. Because Q_{10} matches Q_7, and Q_3 matches Q_4, equal PTAT currents flow in each of the four Q_1 – Q_4 legs. The current in the Q_4 leg biases a Vbe/12kΩ current generator formed by Q_{11} and Q_{12}. The negative TC current from Q_{11} sums at the output. The 4kΩ and 12kΩ resistors are actively laser trimmed over temperature at wafer level to give an accurate zero TC output. NPN transistors Q_5, Q_6, and Q_9 cascode Q_7 and Q_8 for improved accuracy and output impedance. Likewise, J_1 and J_2 cascode Q_3 and Q_4. Using FET cascodes rather than PNPs eliminates noise due to base current. The capacitor provides loop compensation.

100µA was chosen as a practical value for the majority of applications. It is high enough to be used directly for sensor excitation in many instances, while it is low enough to be used in low power and battery powered applications where a higher current might be excessive. Also at higher output currents, thermal feedback on the chip and self heating would reduce the output impedance.

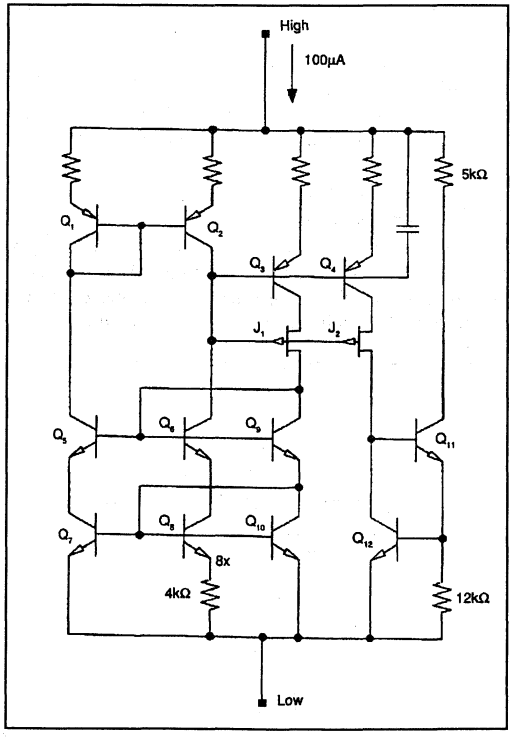


FIGURE 3. The REF200 Current Source cell is powered from its input terminals. It achieves zero TC by summing a positive TC current from a bandgap cell with a negative TC current.

Difet® Burr-Brown Corp.

PIN STRAPPING REF200 FOR: 50µA CURRENT SINK

With a 100µA current source as a reference, it is simple to construct a current source of any value. The REF200 can be pin strapped for 50µA, 200µA, 300µA, or 400µA, in addition to 100µA.

For a 50µA current sink, use the circuit shown in Figure 4. A 100µA current source is tied to the mirror common. Since a current mirror output must equal its input, 50µA flows in the input to ground, and the output is a 50µA current sink.

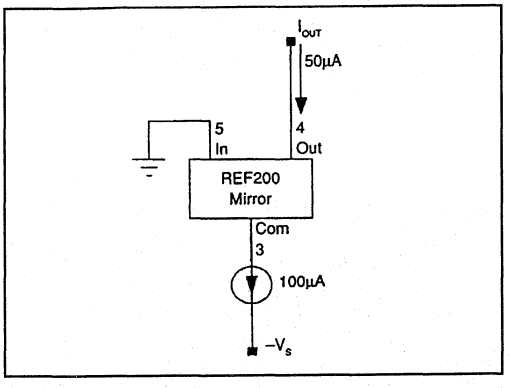


FIGURE 4. A 50µA Current Sink with compliance to ground can be made using one of the 100µA current sources and the mirror from the REF200.

PIN STRAPPING REF200 FOR: 50µA Current Source

For a 50µA current source, use the circuit shown in Figure 5. In this circuit a current sink subtracts 50µA from a second 100µA source leaving a 50µA source. Compliance is from below ground to within 2.5V of the positive rail.

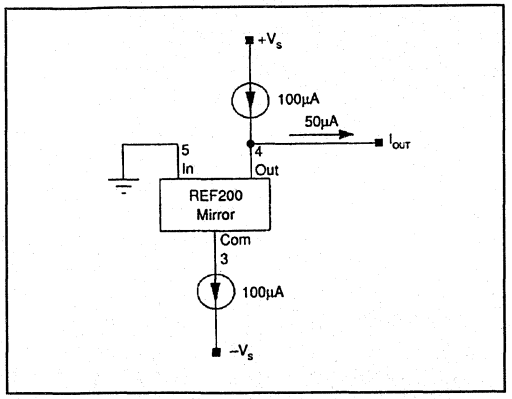


FIGURE 5. A 50µA Current Source with compliance from ground to $+V_S$ –2.5V can be made using both 100µA current sources and the mirror from the REF200.

If compliance closer to the negative rail is needed for either the 50µA sink or source, use the circuit shown in Figure 6, or Figure 7. Here the mirror input is referenced to the negative rail with either a resistor and current source, or a resistor biased zener.

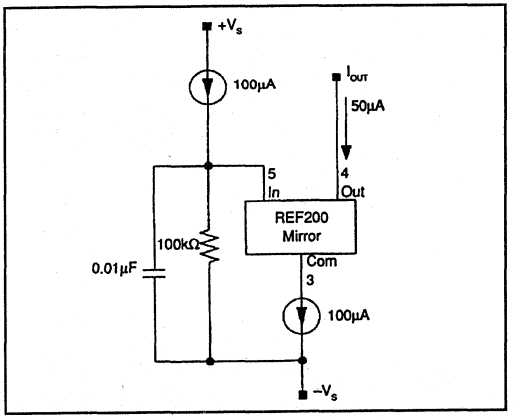


FIGURE 6. Compliance of the 50µA Current Sink (Figure 5) can be extended to $-V_S$+5V by referencing its bias point to the negative power supply rail using the other 100µA current and a resistor.

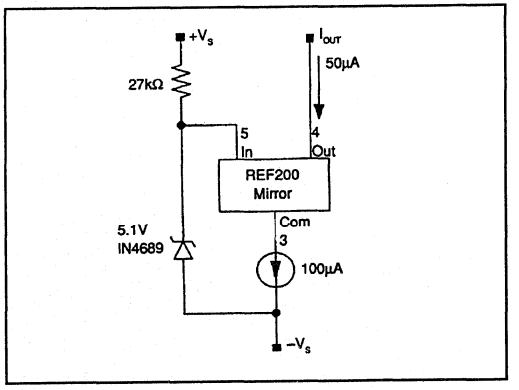


FIGURE 7. If you don't have a current source to spare, the 50µA Current Sink with compliance to $-V_S$+5V can be biased using a zener diode.

PIN STRAPPING REF200 FOR: 200µA FLOATING CURRENT SOURCE

A 200µA floating current source is formed by simply paralleling the two current sources as shown in Figure 8. For compliance nearer to the negative rail, use the mirror as shown in Figure 9. The output of the mirror can swing about a volt closer to the negative rail than the current source alone.

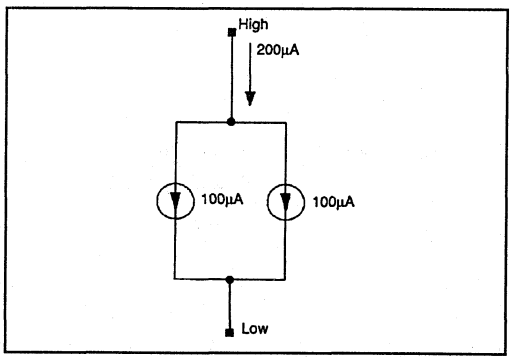


FIGURE 8. For a 200µA Floating Current Source simply parallel the two 100µA current sources from the REF200.

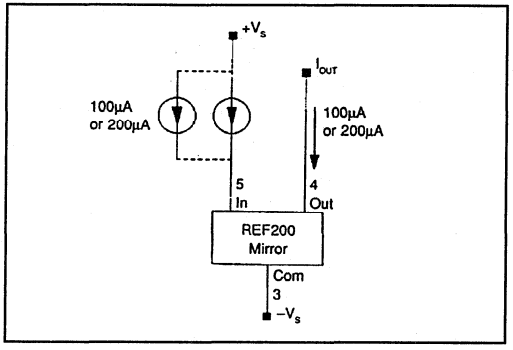


FIGURE 9. You can mirror the 100µA or 200µA Current Sources from the REF200 for a 100µA or 200µA current sink with improved compliance.

PIN STRAPPING REF200 FOR: 300µA Floating Current Source

A 300µA floating current source can be strapped together as shown in Figure 10. It is formed by paralleling a 200µA current source, made with one 100µA source and the mirror, with the other 100µA current source. The 200µA current source is made by connecting a 100µA current source to the mirror input so 100µA flows in the mirror output, and 200µA flows in the mirror common.

PIN STRAPPING REF200 FOR: 400µA Floating Current Source

A 400µA floating current source can be strapped together as shown in Figure 11. It is basically the same as the 200µA current source of Figure 10, except that 200µA is fed into the mirror input. This 200µA is summed with the 200µA that flows in the mirror output for a total of 400µA.

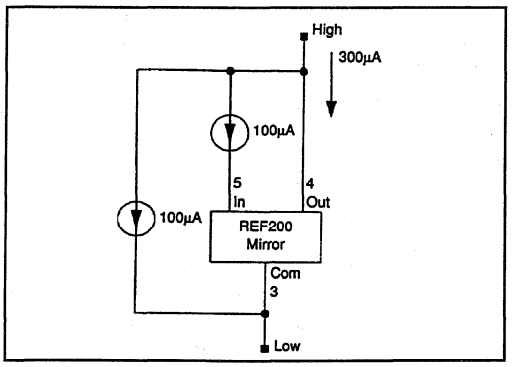


FIGURE 10. The two 100µA Current Sources and Mirror in the REF200 can be connected to form a 300µA floating current source.

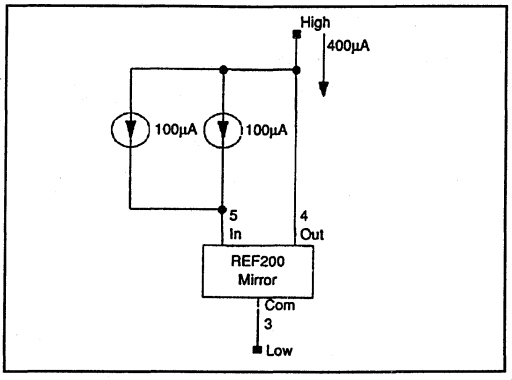


FIGURE 11. The two 100µA Current Sources and Mirror in the REF200 can be connected to form a 400µA floating current source.

RESISTOR PROGRAMMABLE CURRENT SOURCES AND SINKS USING REF200 AND ONE EXTERNAL OP AMP:

Current Source or Sink With Compliance to Power Supply Rail and Current Out >100µA

You can build a programmable current source of virtually any value using two resistors, an op amp, and a 100µA current source as a reference.

The current source shown in Figure 12 can be programmed to any value above the 100µA reference current. It has compliance all the way to the negative power supply rail. The 100µA reference forces a voltage of 100µA • R_1 at the non-inverting input of the op amp. When using a ***Difet***® op amp as shown, input bias currents are negligible. The op amp forces the same voltage across R_2. If R_1 is N • R_2, the output current is (N+1) • 100µA. So long as the op amps input common mode range and its output can swing to the negative rail within the voltage drop across R_1, the current source can swing all the way to the negative rail. If the voltage drop across R_1 is large enough, any op amp can

satisfy this requirement. Figure 13 shows the same circuit turned around to act as a current sink. It has compliance to the positive rail.

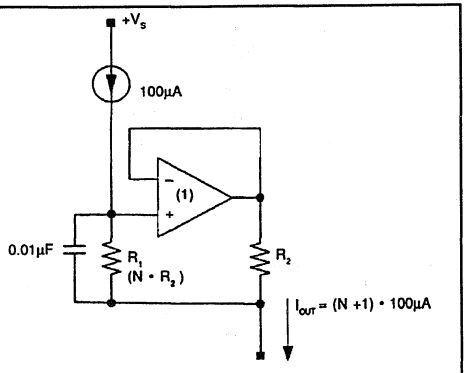


FIGURE 12. Current Source.

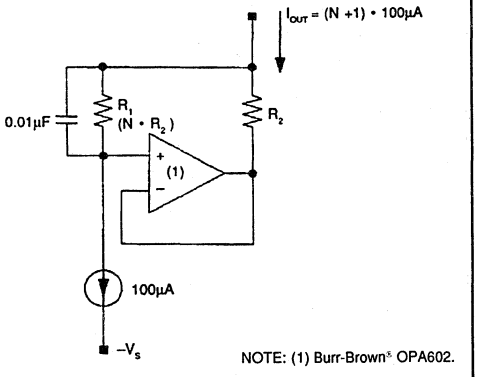
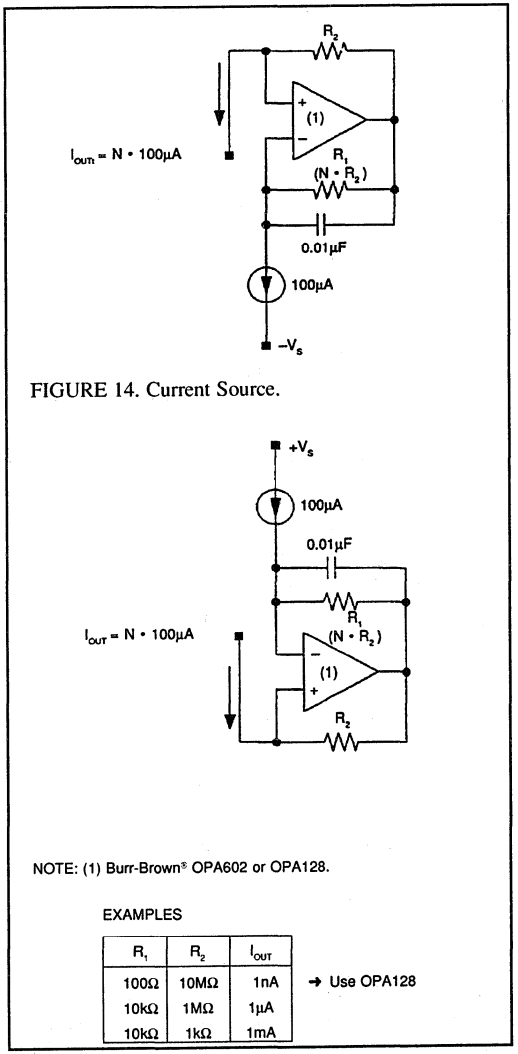


FIGURE 13. Current Sink.

FIGURES 12 and 13. For a programmable current source with any output current greater than 100µA and compliance to $+V_S$ or $-V_S$, use a 100µA current source as a reference along with an external op amp and two programming resistors.

Current Source or Sink With Any Current Out

For currents less than 100µA, use the circuits shown in Figures 14 and 15. They can be programmed for virtually any current (either above or below 100µA). In this case the 100µA current source forms a reference across R_1 at the inverting input of the op amp. Since the reference is not connected to the output, its current does not add to the current output signal. So, if R_1 is $N \cdot R_2$, then output current is $N \cdot 100\mu A$. Because compliance of the 100µA current source is 2.5V, the current source, Figure 14, can only comply within 2.5V of the negative rail—even if the op amp can go further. Likewise the current sink, Figure 15, has a 2.5V compliance to the positive power supply rail.



FIGURES 14 and 15. If you don't need compliance to the power supply rail, this circuit using a 100µA current source as a reference along with an external op amp and two programming resistors can provide virtually any output current.

Current Sources and Sinks Using Voltage References

To make a current source with the best possible accuracy use a zener-based voltage reference. The REF200 uses a band-gap type reference to allow low voltage two-terminal operation. Although this makes a more flexible general-purpose part with excellent performance, its ultimate temperature drift and stability cannot compare to the REF102 precision 10.0V buried zener voltage reference.

Make a current source from a voltage reference using the circuit shown in Figure 15A. The voltage follower connected op amp forces the voltage reference ground connection to be equal to the load voltage. The reference output then forces an accurate 10.0V across R_1 so that the current source output is $10V/R_1$.

Negative output compliance for the current source is limited by the op amp input common-mode range or output range (whichever is worse). When using the OPA111 on ±15V power supplies, the negative compliance is –10V. For compliance almost to the negative power supply rail, use a single-supply op amp such as the OPA1013.

Positive output compliance is limited by the voltage reference minimum $+V_S$ requirement. When using the REF102 on ±15V power supplies, positive compliance is +3.5V.

Make a current sink with a voltage reference using the circuit shown in Figure 15B. The op amp drives both the voltage reference ground connection and the current scaling register, R_1, so that the voltage reference output is equal to the load voltage. This forces –10.0V across R_1 so that the current sink output is $-10V/R_1$. The R_2, C_1 network provides local feedback around the op amp to assure loop stability. It also provides noise filtering. With the values shown, the reference noise is filtered by a single pole with $f_{-3dB} = 1/(2 \cdot \pi \cdot R_2 \cdot C_1)$.

Negative output compliance for the current sink is limited by the op amp and further reduced by the 10V drop across R_1. When using the OPA111 on ±15V power supplies, negative compliance is only guaranteed to ground. When using the single-supply OPA1013 op amp, negative compliance is approximately –5V.

Positive compliance is limited by the REF102, but is improved by the 10V across R_1. For a REF102 operating on ±15V power supplies, the positive compliance is +10V (limited by the op amp common mode input range).

Keep in mind that the ultimate accuracy of a voltage reference based current source depends on the absolute accuracy of the current-scaling registor. The absolute TCR and stability of the resistor directly affect the current source temperature drift and accuracy. This is in contrast to circuits using current source references, as shown in Figures 12 to 15, where accuracy depends only on the ratio accuracy of the resistors. It is much easier to get good resistor ratio accuracy than to get good absolute accuracy especially when using resistor networks.

Although these current sources made with voltage references do not have the compliance range of the previous circuits, they may be the best choice where the utmost in accuracy is required.

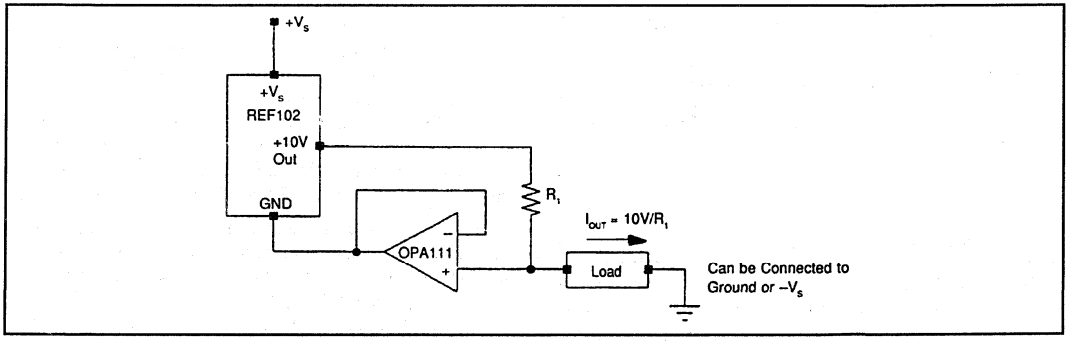


FIGURE 15A. Current Source using Voltage Reference and Op Amp.

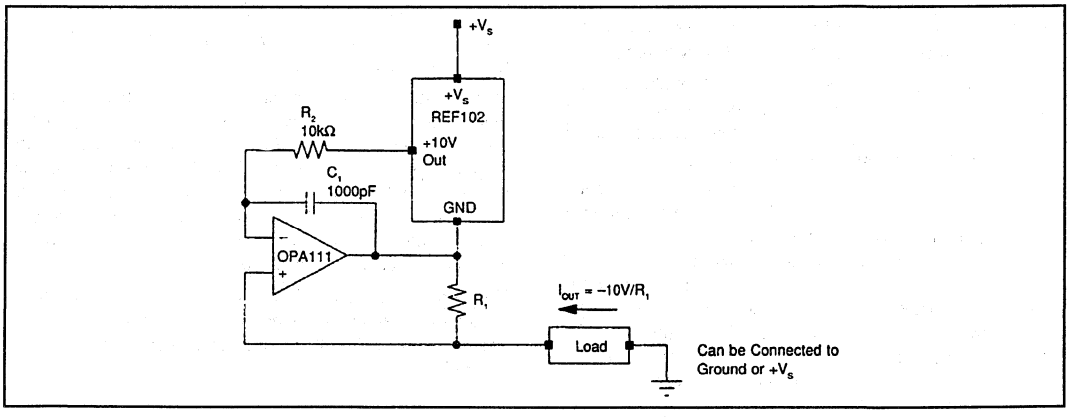
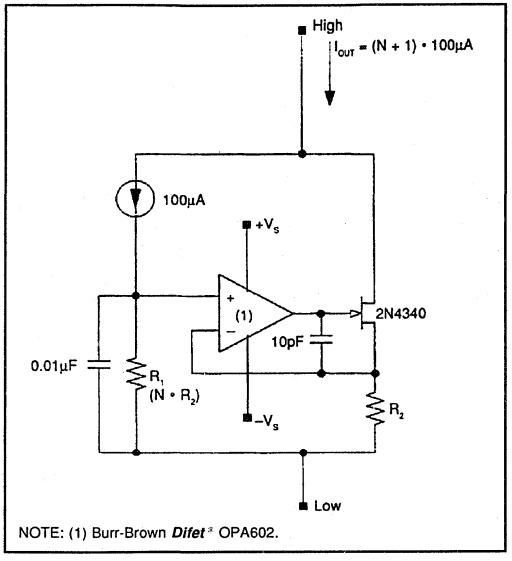


FIGURE 15B. Current Sink using Voltage Reference and Op Amp.

Floating Current Source With Current Out > 100µA

If a completely floating programable current source is needed, use the circuit shown in Figure 16. It is basically the same as the current source shown in Figure 12 except that R_2 is driven by a MOSFET. Since no current flows in the gate of the MOSFET or the inputs of the op amp, all current that enters the resistors (and no more) leaves. Therefore the current source is completely floating.

The power supplies of the op amp in this circuit, as in the other circuits, must be connected to $\pm V_S$. Also, the input and output common mode limitations of the op amp must be observed.



NOTE: (1) Burr-Brown *Difet*® OPA602.

FIGURE 16. Use a 100µA Current Source as a reference, an external op amp, two programming resistors, and a series pass element for a programmable floating curent source.

Current Sources and Sinks and Current Mirrors Using an Amplifier and a Series Pass Element

In some applications it may be desirable to make a current source or sink using a series pass element in addition to an op amp. This approach provides the benefits of cascoding and also allows arbitrarily high current outputs.

The circuit used is the same as for the programmable floating current source shown in Figure 16. The difference is that the op amp power supply connection and reference input are both returned to a fixed potential. The result is either a current source or sink, but not a floating current source. The advantage is that the output can be any value, either more than, less than, or equal to the input reference. Also, a voltage source or even a variable voltage input can be used as a reference. The examples shown in Figures 17 through 20 show 100µA current sources used as references.

Notice that since a current source is used as a reference, the circuit can also be used as a precision current mirror. Unlike mirrors which use matched transistors, this mirror remains highly accurate no matter what the mirror ratio.

The pass element can bipolar, JFET, MOSFET, or a combination. The examples recommend MOSFETS because their low gate current minimizes output error. Also, MOSFETs with very high current ratings are available, and require no additional drivers.

In many cases bipolar devices are adequate and may be preferred due to their low cost and availability. With a bipolar device, the base current will add error to the output signal as discussed in the cascoding section. Using a darlington-connected bipolar device feeds the error current back into the signal path and reduces the error by the forward current gain (beta) of the input transistor.

In some high temperature applications, darlington-connected bipolar transistors may have lower error than FETs. As a rule of thumb, the gate current of a FET or MOSFET doubles for every 8°C increase in temperature, whereas the beta of a bipolar device increases approximately 0.5%/°C. Therefore, when operating at 125°C, the gate current of a FET will be about 6000 times higher than at 25°C, while the base current of the bipolar will be 1.5 times lower.

When selecting the op amp for this application, pay particular attention to input bias current, input common mode range, and output range.

The bias current of the op amp adds to the input current, and subtracts from the output current. For a 1:1 mirror application, the error is only the mismatch of bias currents or I_{OS} of the amplifier. For other ratios, assume that the error is equal to the full amplifier bias current. For most applications, the error will be negligible if a low bias current ***Difet***® amplifier such as the Burr-Brown OPA602 is used. Its I_B is 1pA max.

Be sure to observe the input common mode range limit of the op amp. For example, when using the OPA602 in a current sink application, the voltage between the op amp negative supply and its input must be at least 4V. In a split power supply application, R_1 and R_2 can be connected to ground, and the op amp negative supply can be connected to –5V or –15V and there is no problem. In a single supply application, or when R_1, R_2, and the op amp's $-V_S$ are all connected to the negative power supply, a drop of at least 4V must be maintained across R_1.

Using a single supply op amp allows the input common mode range to go to 0V. Especially in single supply current mirror applications, it is often desirable for the input and output to go to zero. The OPA1013 has an input common-mode range which extends to its negative power supply, and its output will swing within a few mV of the negative supply. Although the OPA1013 has bipolar inputs, its bias current is low enough for most applications.

Components R_3, R_4, and C_1 form a compensation network to assure amplifier stability when driving the highly capacitive inputs of some MOSFETs. In many applications they can be omitted.

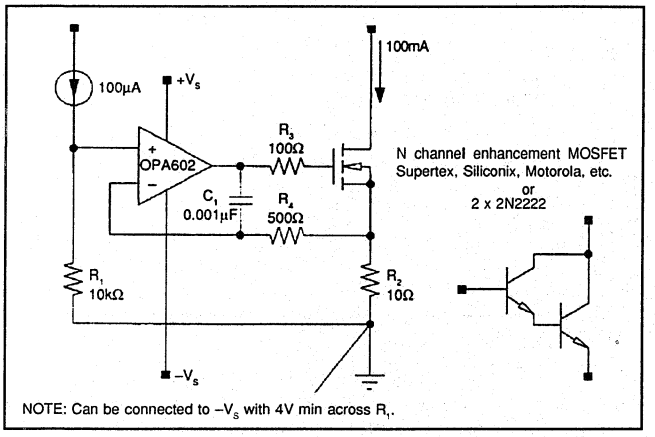


FIGURE 17. Programmable Current Sink using series pass device.

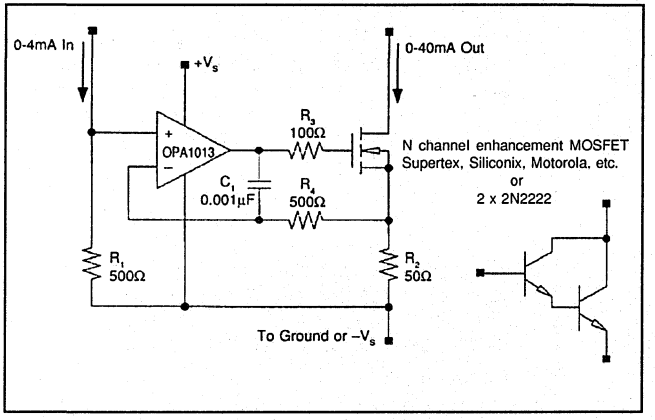


FIGURE 18. Sinking Current Mirror using series pass device.

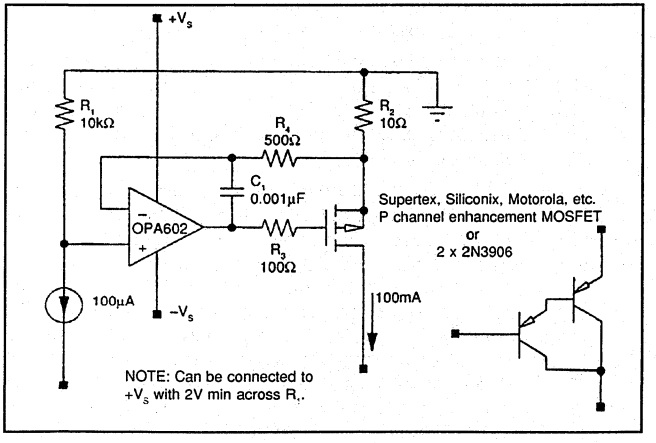


FIGURE 19. Programmable Current Source using series pass device.

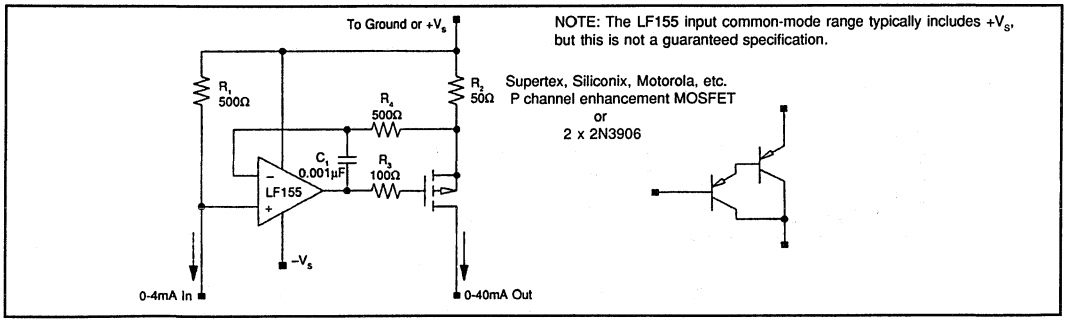


FIGURE 20. Sourcing Current Mirror using series pass device.

Floating Current Source With Current Out >100µA and No Separate Power Supply

If a programmable current source is needed, and no separate power supply is available, consider the floating current source shown in Figure 21. Here the op amp power supplies are connected to the current source input terminals. The op amp quiescent current is part of the output current.

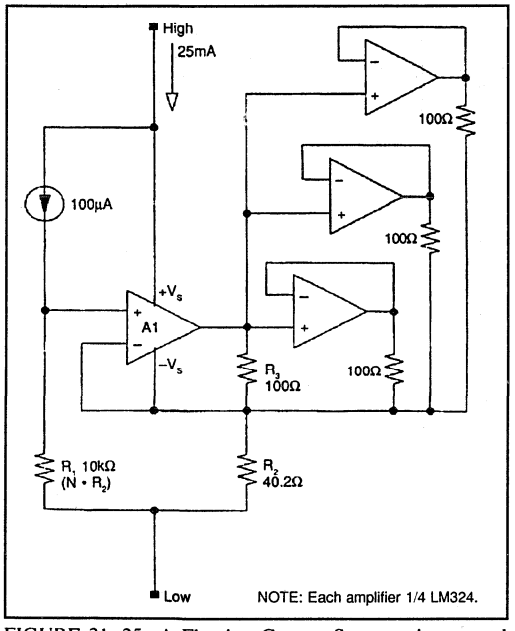


FIGURE 21. 25mA Floating Current Source using a quad single-supply op amp needs no external power supply.

There are two special requirements. First, a single supply op amp must be used (an op amp with an input common mode range that includes the negative supply rail). Also the output current must be greater than the op amp quiescent current.

The circuit is basically the same as Figure 12. The 100µA current flowing through R_1 produces a floating voltage reference at the non-inverting input of A_1. The op amp quiescent current flowing from its negative supply pin sums into the current flowing into R_2. The op amp outputs drive the additional current needed through R_2 so the voltage drop across it matches the voltage drop across R_1. If R_1 is N • R_2, the output current is (N+1) • 100µA. With the values shown, the output current is 25mA.

The op amp outputs are connected to R_2 through 100Ω resistors. The current delivered by A_1 produces an approximate 0.5V voltage drop across R_3. The other three op amps are connected as voltage followers so that the same voltage is dropped across the other three 100Ω resistors. The output current from each op amp is therefore equal and the load is shared equally. This technique allows any number of 10mA output op amps to be paralleled for high output current.

CASCODING CURRENT SOURCES FOR IMPROVED OUTPUT IMPEDANCE, HIGH FREQUENCY PERFORMANCE, AND HIGH VOLTAGE COMPLIANCE

Cascoding With FETs

The output impedance and high frequency performance of any current source can be improved by cascoding. Starting with a precision current source like the REF200 or any of the variations previously discussed, it is relatively easy to build a current source to satisfy just about any need.

Cascoding can also be used to increase high voltage compliance. High voltage compliance of a cascoded current source is limited solely by the voltage rating of the cascoding device. High voltage compliance of hundreds or even thousands of volts is possible.

Cascoding is the buffering of the current source from the load by a series pass device as shown in Figure 22. Here an N channel JFET cascodes the current source from the output. The gate of the JFET is tied to ground, its source to the current source, and its drain to the load. Variations in the load voltage are taken up by the drain of the JFET while the source voltage remains relatively constant. In this way, the voltage drop across the current source remains constant regardless of voltage changes across the load. With no changes in the voltage across the current source, and with no current lost through the JFET drain approaches infinity. AC performance of the cascoded current sink approaches that of the JFET.

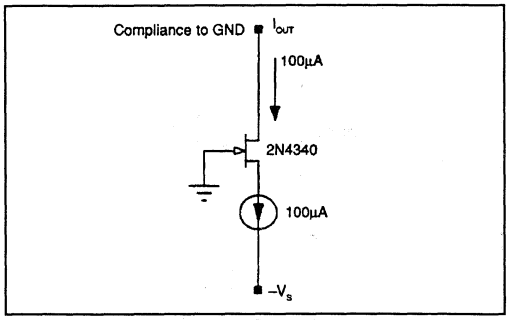


FIGURE 22. Cascoded Current Sink with compliance to ground.

Since the gate of the JFET is tied to ground, the output compliance is limited to near ground. If greater compliance is required for the current sink, the gate of the JFET can be referenced a few volts above the negative rail as shown in Figures 23 and 24. In Figure 23 the gate reference is derived from a resistor biased from the second current source. If a current source is not available, use a resistor biased zener as shown in Figure 24.

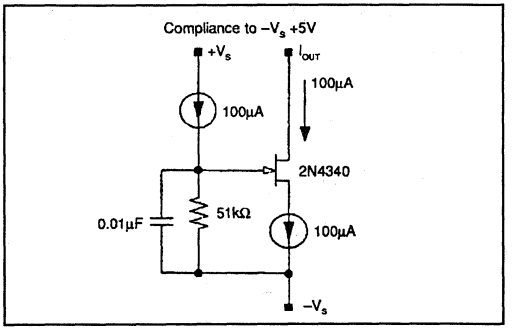


FIGURE 23. Cascoded Current Sink with compliance to $-V_S$+5V (using zener diode for bias).

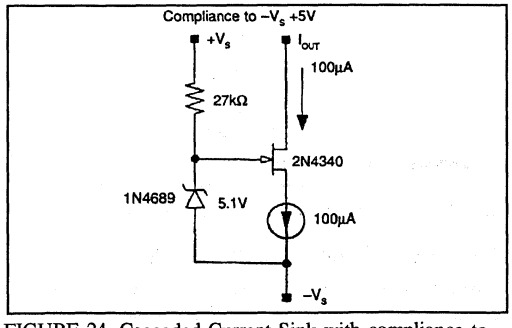


FIGURE 24. Cascoded Current Sink with compliance to $-V_S$+5V (using zener diode for bias).

To implement current sources, turn the circuits around and use P channel JFETs as shown in Figures 25 through 27.

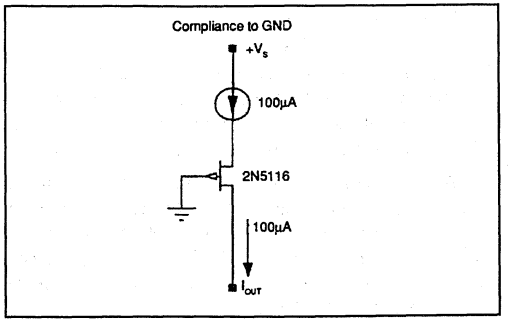


FIGURE 25. Cascoded Current Source with compliance to ground.

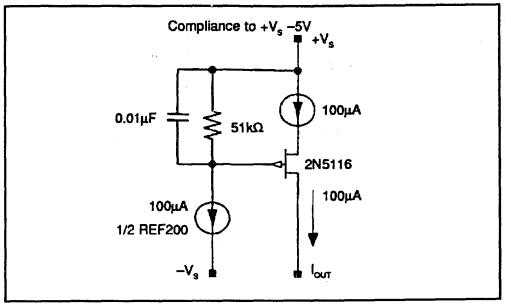


FIGURE 26. Cascoded Current Source with compliance to $-V_S$+5V (using current source and resistor for bias).

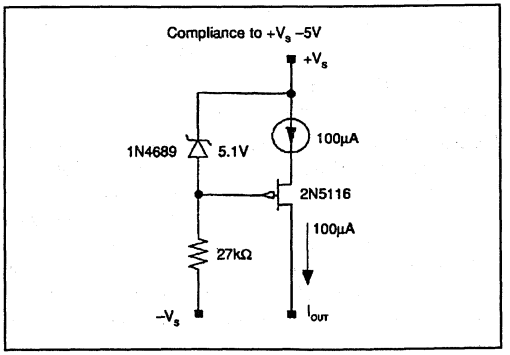


FIGURE 27. Cascoded Current Source with compliance to $-V_S$+5V (using zener diode for bias).

In most applications, JFETs make the best cascoding devices, but bipolar transistors and MOSFETs can also be used. MOSFETs can provide equivalent AC and DC performance to JFETs. Bipolar devices may offer better high frequency performance, but have a limited DC output impedance. The output impedance of a bipolar cascoded current source is limited by changes in base current with changes in collector voltage. The maximum output impedance of a bipolar cascoded current source is $b \bullet R_O$, where b is the current gain of the bipolar device, and R_O is its output impedance

200µA Floating Cascoded Current Source Using REF200

Floating cascoded current sources with typical output impedances exceeding 10GΩ can be easily implemented. Using the REF200 and a few external devices, sources of 200µA, 300µA, and 400µA can be strapped together.

The 200µA floating cascoded current source is shown in Figure 28 It is made using a cascoded current source and a cascoded current sink each biasing the other. Low voltage compliance is limited to about 8V by the sum of the gate reference voltages. High voltage compliance is limited by the lower voltage rated FET.

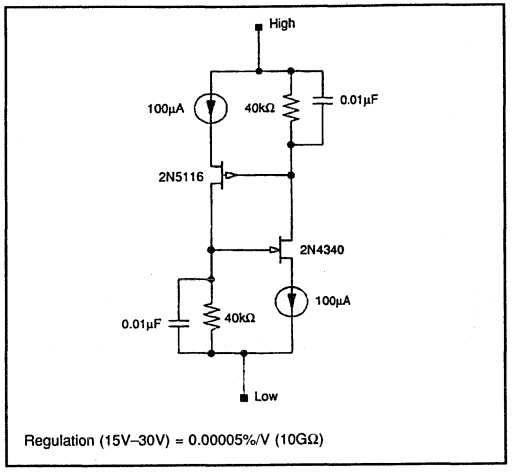


FIGURE 28. Cascoded 200µA Floating Current Source.

300µA Floating Cascoded Current Source Using REF200

The 300µA floating current source is shown in Figure 29. It is similar to the 200µA current source shown in Figure 28, except the current source in the cascoded sink section is derived from the mirror. The gate reference for the sink cascode is derived from the series combination of the mirror input and a 27kΩ resistor. The extra 100µA is obtained by summing the other 100µA current source into the sink cascode device. Compliance limits are the same as for the 200µA cascoded source.

400µA Floating Cascoded Current Source Using REF200

The 400µA floating cascoded current source is shown in Figure 30. It is the similar to the 300µA cascoded current source, except that the mirror is driven by a cascoded 200µA current source derived by the parallel combination of the two current sources in the REF200. The low voltage compliance of this circuit is about 1V better than the previous two circuits because the mirror compliance is about 1V better. High voltage compliance is still limited only by the breakdown of the lower rated FET.

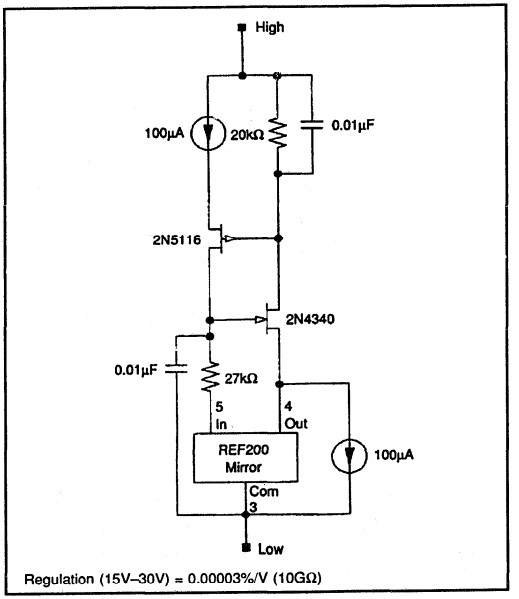


FIGURE 29. Cascoded 300µA Floating Current Source.

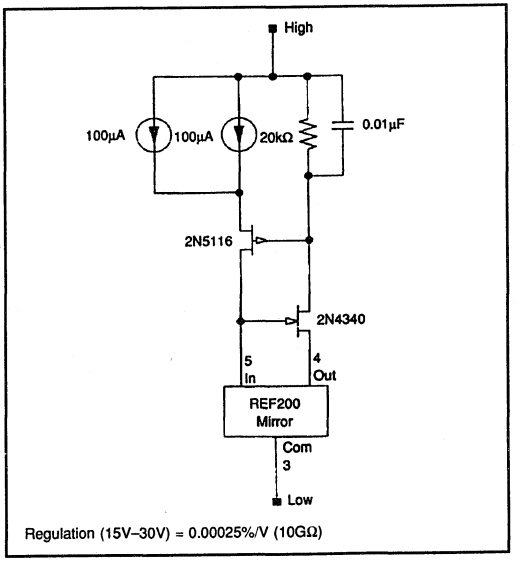


FIGURE 30. Cascoded 400µA Floating Current Source.

NOISE REDUCTION OF CURRENT SOURCES

In many modern systems, noise is the ultimate limit to accuracy. And in some systems, performance can be improved with a lower noise current source. Current source noise can be reduced by filtering, using the same basic principals used for noise reduction of voltage references. Reducing the noise bandwidth by filtering can reduce the total noise by the square root of the bandwidth reduction.

One current source noise reduction circuit is shown in Figure 31. It is basically a FET cascode circuit with the addition of an RC noise filtering circuit. The FET, as biased by the 100µA current source, forces an accurate DC voltage across the circuit.

Without the capacitor, noise from the current source would feed directly through to the output. The capacitor filters the noise at a –3dB frequency of $1/(2 \cdot \pi \cdot R \cdot C)$, or about 30Hz in this example. Filtering below this frequency will not reduce noise further, since the 30Hz pole is already below the 1/f corner of the current source, and noise can not be reduced by filtering in the 1/f region. Also, the noise of the FET and resistor are not filtered. Still, using this circuit, the noise is reduced from the typical 20pA/√Hz to less than 1pA/√Hz.

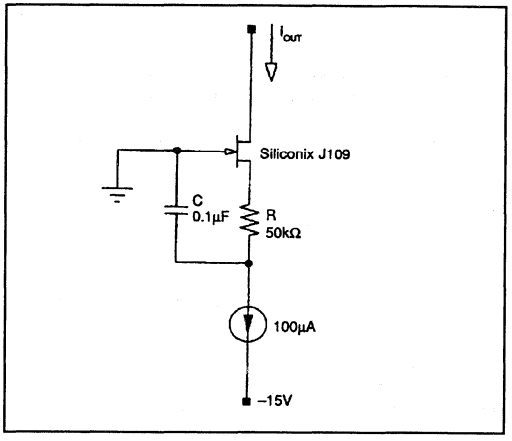


FIGURE 31. Current noise from a current source can be filtered using this circuit.

The value of the resistor used in the noise reduction circuit determines its ultimate performance. Although the noise of the resistor increases with the square root of its value, its noise degenerating effect reduces noise linearly. Therefore, the noise is reduced by the square root of the resistor increase. The practical limit for the noise reduction is the voltage drop which can be placed across the resistor.

Mathematically, current noise due to the resistor is the resistor thermal noise divided by the resistor value.

$$I_{R\,NOISE} = \frac{(1.3 \cdot 10^{-10})\sqrt{R}}{R} = (1.3 \cdot 10^{-10})/\sqrt{R}$$

With a 50kΩ resistor, the minimum theoretical noise is .6pA/√Hz, with 10kΩ, it is 1.3pA/√Hz. Noise measurements of the circuit using both 10kΩ and 50kΩ resistors and the Siliconix J109 FET agree with these theoretical numbers within 20%.

The noise reduction circuit in Figure 31 has a low voltage compliance limit near ground. For compliance below ground, use the circuit shown in Figure 32.

In addition to noise reduction, these circuits have the other advantages of a FET cascoded current sink; output impedance in the GΩ region, improved AC performance, and high voltage compliance limited only by the FET.

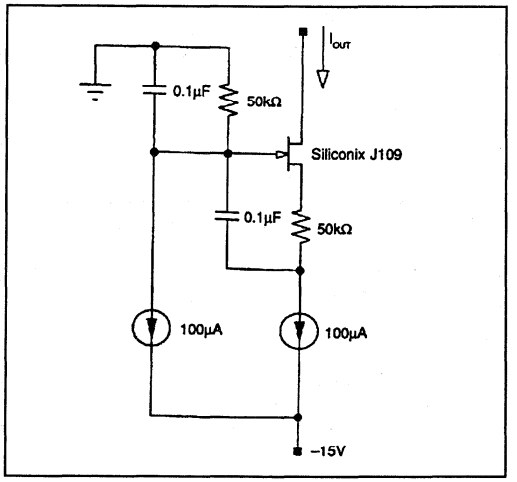


FIGURE 32. Current Noise Filtering Circuit with compliance below ground.

APPLICATIONS OF FIXED CURRENT SOURCES

VOLTAGE REFERENCES USING CURRENT SOURCES

Many design problems can be easily solved with inexpensive, easy-to-use current sources like the REF200. Although applications are endless, the collection of circuits that follows is intended to stimulate your thinking in several broad categories: fixed voltage references, floating voltage references, current excitation, fixed current references, steered current references, and biasing.

Current sources are a versatile means of forming voltage references. Why not just use a voltage reference? With a current source, a single resistor provides a programmable voltage source of any value. Low voltage references are often needed, and with this approach, it's as easy to get a 1mV reference as it is to get a 10V reference. Also, the voltage can be referenced anywhere—to the positive rail, the negative rail, or floating anywhere in between.

When impedances driven by the voltage reference are high, the voltage output from the resistor derived voltage reference can be used directly. The 100µV reference shown in Figure 33 can be used directly in voltage-to-frequency converter (VFC) auto-zero applications where an off-zero reference is needed (since zero frequency would take forever to measure, off-zero techniques are often used for calibrating VFCs). Where a lower output impedance is needed, a simple buffer can be added as shown in Figure 34.

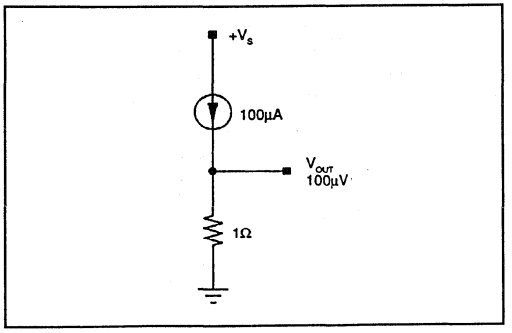


FIGURE 33. 100µV Reference for VFC off-zeroing.

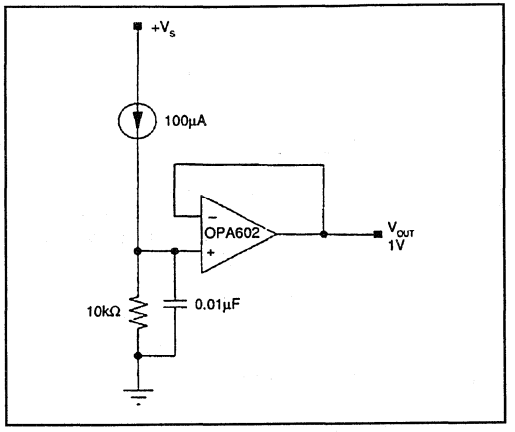


FIGURE 34. Buffered Voltage Reference.

For a floating voltage reference, simply drive the reference low side (grounded side of the voltage-setting resistor) as shown in Figure 34A. Notice that in addition to the swing limitations imposed by the op amp input common-mode range and output range, the reference high side swing is limited to 2.5V from the positive rail by the REF200's minimum compliance voltage. The low side swing is limited only by the op amp. If the reference voltage is more than about 3V this limitation can be eliminated by adding gain as shown in Figure 34B. In this example, the 1V across the reference setting-registor is amplified to 5V at the output. Since there is always 4V between the output and the op amp inputs, the high-side swing is not limited by the current source compliance or the op amp input common mode range. It is limited only by the op amp out put swing capability.

Where the voltage reference is lower than about 3V, the high side compliance will still be limited by the current source compliance. In these situations, consider the circuit shown in Figure 34C. In this case, the op amp noninverting input is driven while the current source connects to the other op amp input and a voltage setting resistor with its other terminal connected to the output. High-side compliance is limited only by the op amp. Another advantage of this circuit is its high input inpedance. The disavantage is limited low side compliance. Current source compliance limits swing to the negative rail to 2.5V — regardless of the op amp input common mode range.

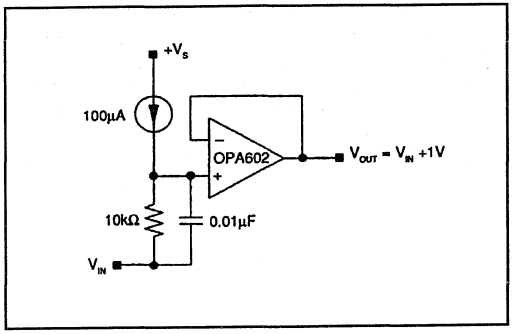


FIGURE 34A. Floating Voltage Reference.

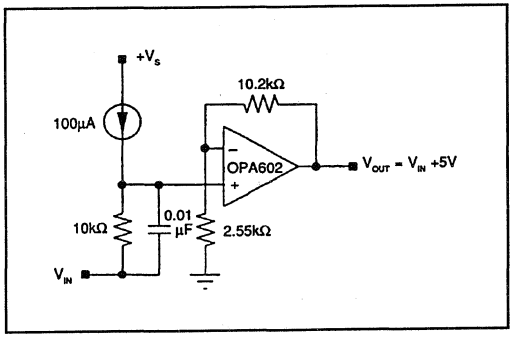


FIGURE 34B. Floating Voltage Reference with high-side compliance limited only by op amp output swing capability.

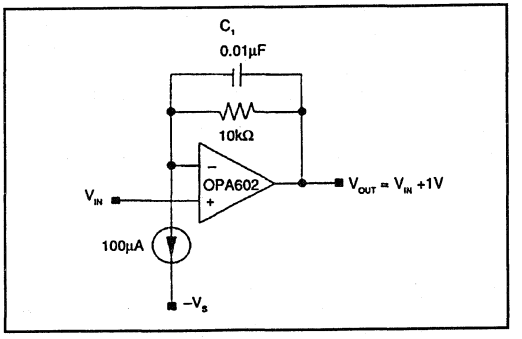


FIGURE 34C. Floating Low Voltage Reference with high impedance input drive and high-side output compliance limited only by op amp output swing capability.

OP AMP OFFSET ADJUSTMENT USING 5mV REFERENCE

Op amp offset adjustment circuits are another application for millivolt level references. Many op amps, especially duals and quads, have no built-in provision for offset adjustment. Even when offset adjustment pins are provided, using them can degrade offset voltage drift and stability (e.g. the drift of a typical bipolar input op amp is increased 3µV/°C for each millivolt of offset adjustment). External offset adjustment circuits are commonly used to solve these problems.

Conventional external offset adjustment circuits can add problems of their own. Many of these circuits use the op amp power supplies as references. Power supply variation feeds directly into the op amp input. This error appears as poor power supply rejection. Likewise, noise from the power supplies appears as op amp input referred noise.

The circuits shown in Figures 35 and 36 solve these problems. REF200 current sources provide regulated ±5mV references for stable offset adjustment. This approach provides a truly precision offset adjustment free from problems associated with power supply variations, noise, and drift.

The circuit shown in Figure 35 uses a pair of 51Ω resistors connected to ground to establish the ±5mV reference. A pot connected across this reference allows a ±5mV offset adjustment range. Additional pots can be connected, but be sure to maintain a parallel resistance >50Ω to get >±5mV range.

The second circuit, Figure 36, uses a special potentiometer manufactured by Bourns. It is especially designed for op amp offset adjustment. It has a tap at the center of the element which can be connected to ground. Using this connection eliminates the 51Ω resistors needed in the first circuit.

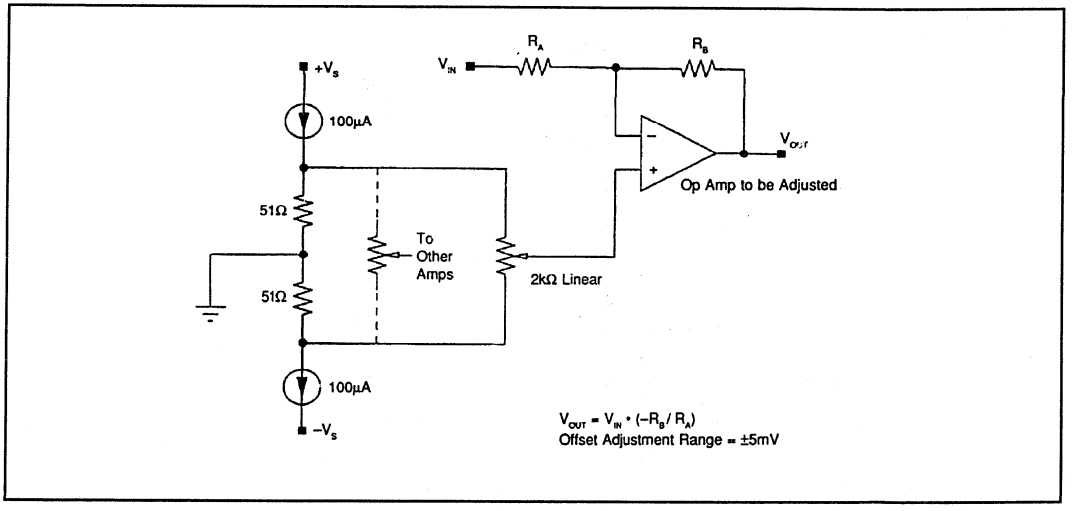


FIGURE 35. Op Amp Offset Adjustment Circuit uses the two 100µA current sources from a REF200 to provide accurate ±5mV references.

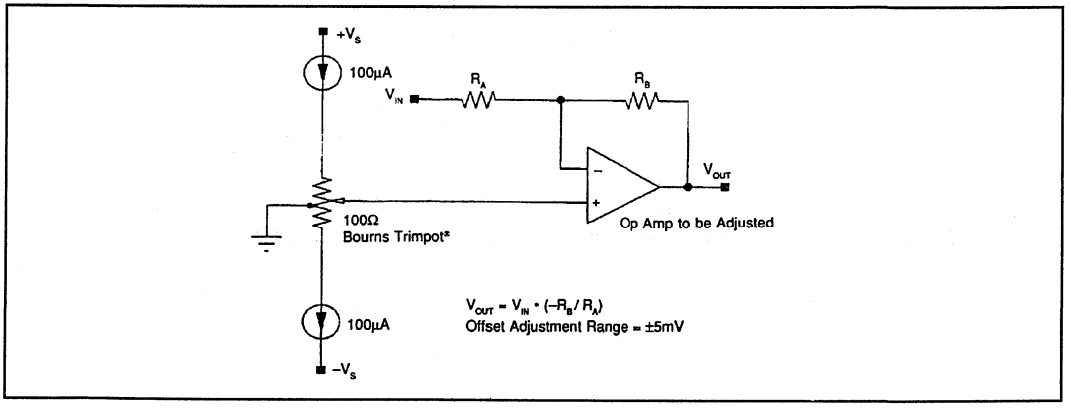


FIGURE 36. Op amp offset adjustment circuit using Bourns Trimpot®.

WINDOW COMPARATOR USING FLOATING VOLTAGE REFERENCE

The window comparator circuit, Figure 37, is an example of a floating reference application. Here, a pair of current sources is used to provide a floating bipolar window voltage driven by the V_{CENTER} input. V_O is low when V_I is either above V_{CENTER} + 100µA • R, or below V_{CENTER} – 100µA • R. Otherwise, V_O is high. By using different values for the programming resistors, the threshold can be set asymmetrically around V_{CENTER} if desired.

RTD EXCITATION USING CURRENT REFERENCE

Current sources are often used for excitation of resistor type sensors such as RTDs. If the RTD is located remotely, as it often is, voltage drops in the interconnecting wire can cause excessive errors. The usual solution to this problem is to use four wire Kelvin connections. Two wires are used to carry the current excitation signal to the RTD. The other two wires sense the voltage across the RTD. With no current flowing in the sense connection, there is no error due to wire resistance.

One problem is that the additional wiring can be very expensive. The three wire circuit shown in Figure 38 saves one wire. 200µA is used for excitation of a 1kΩ RTD, and a matching current from the current mirror is forced in the ground connection. The voltage drops through the two wires cancel thereby eliminating error.

Notice also, that one common wire (shown as a shield) can serve multiple sensors. Each additional RTD only needs one additional pair of wires.

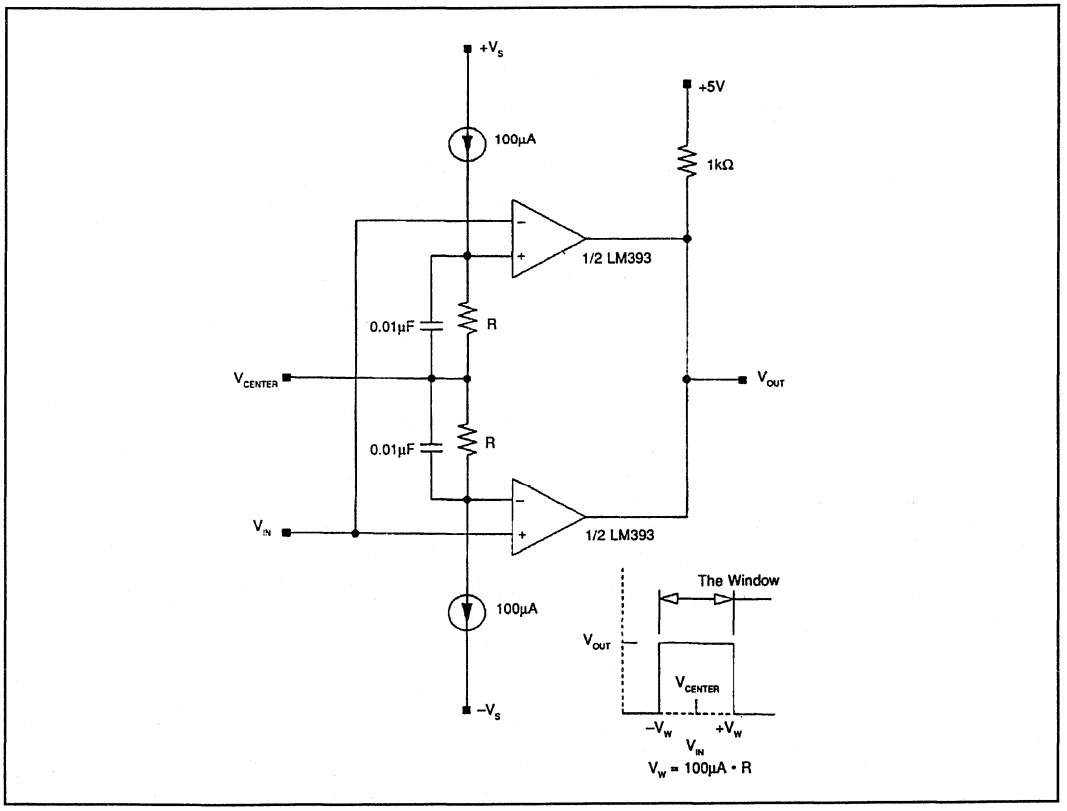


FIGURE 37. Window comparator with voltage programmable window center, and resistor programmable window width.

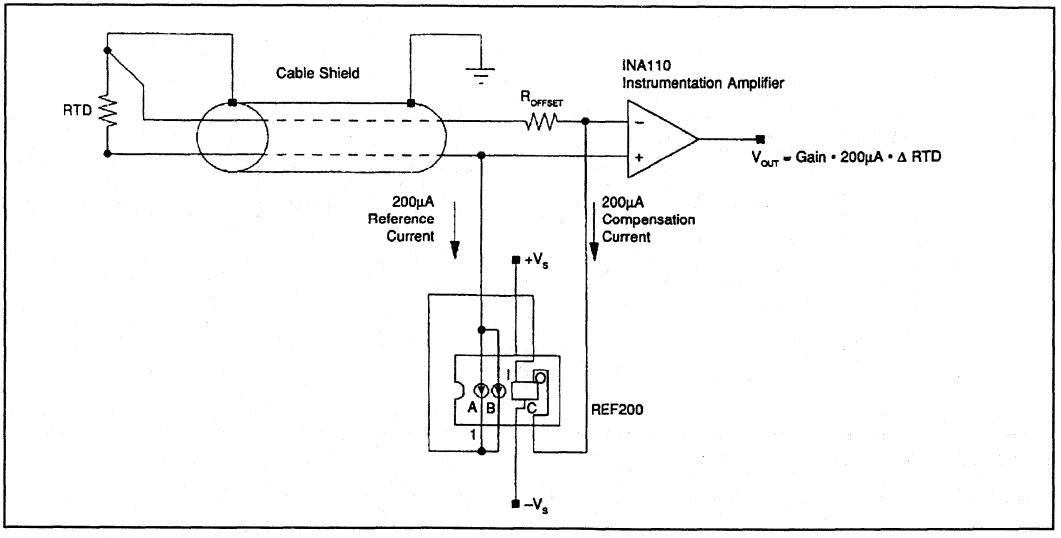


FIGURE 38. RTD excitation with three-wire lead resistance compensation.

DEAD BAND CIRCUITS USING CURRENT REFERENCE

Servo control systems frequently use dead-band and limiting circuits. The precision dead-band circuit shown in Figures 39 and 40 demonstrates the use of a current source as a fixed reference. To understand how it works, notice that, without the current reference, the circuit is an inverting half wave rectifier. Positive inputs drive the op amp output negative and feedback is through forward biased D_1. No current flows through reverse biased D_2, and the output is held at virtual ground by R_2.

Negative inputs forward bias D_2 and drive the output positive. Feedback to the output through R_2 eliminates error due to the diode drop, and the circuit functions as a precision unity gain inverter ($V_O = -V_I$). (Adding the current reference pre-biases to the input so that the output remains at virtual ground until the input current through R_1 exceeds 100µA.) The output is zero (dead) until $V_I < \pm 100\mu A \cdot R_1$. An alternate approach would be to pre-bias the input through a precision resistor connected to a voltage reference, but that would add noise gain increasing offset, drift, and noise at the output.

For a negative dead-band use the circuit shown in Figure 40. It's the same circuit with the diodes reversed.

For a double dead-band, use the circuit shown in Figure 41. It uses both the positive and negative dead-band circuits summed together by a third amplifier.

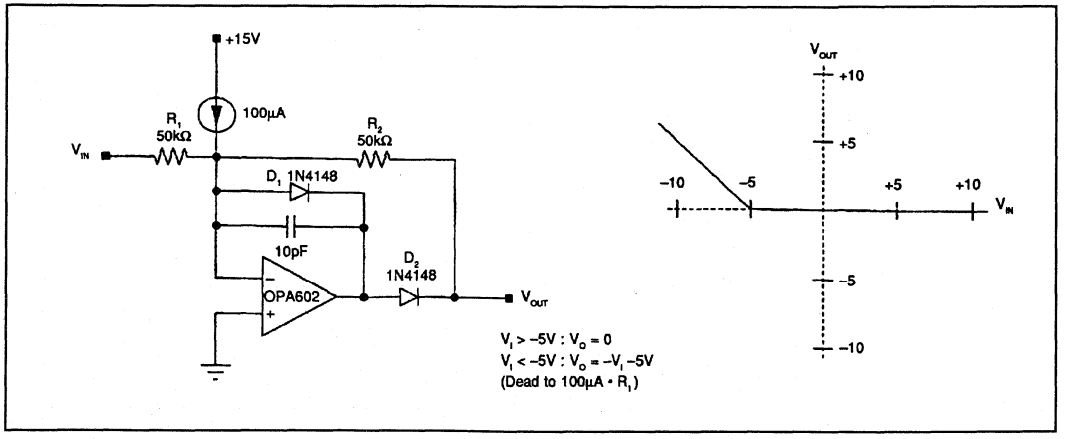


FIGURE 39. Precision positive dead-band circuit.

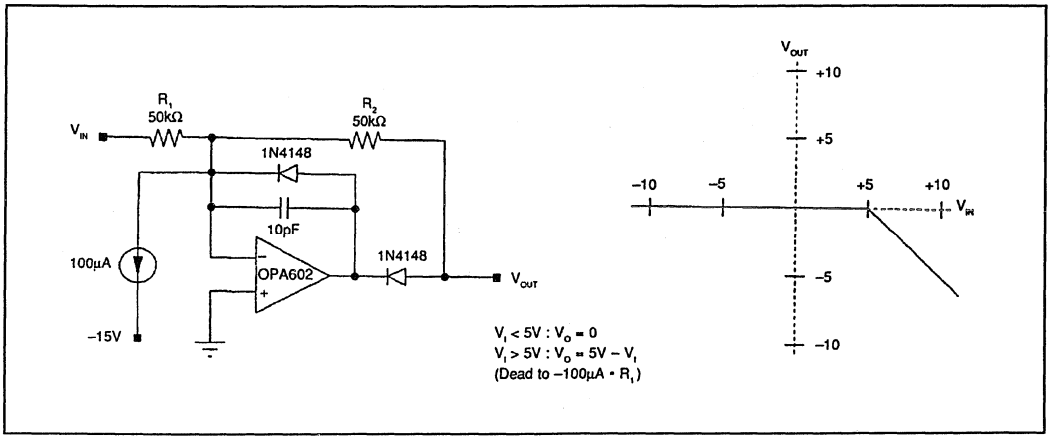


FIGURE 40. Precision negative dead-band circuit.

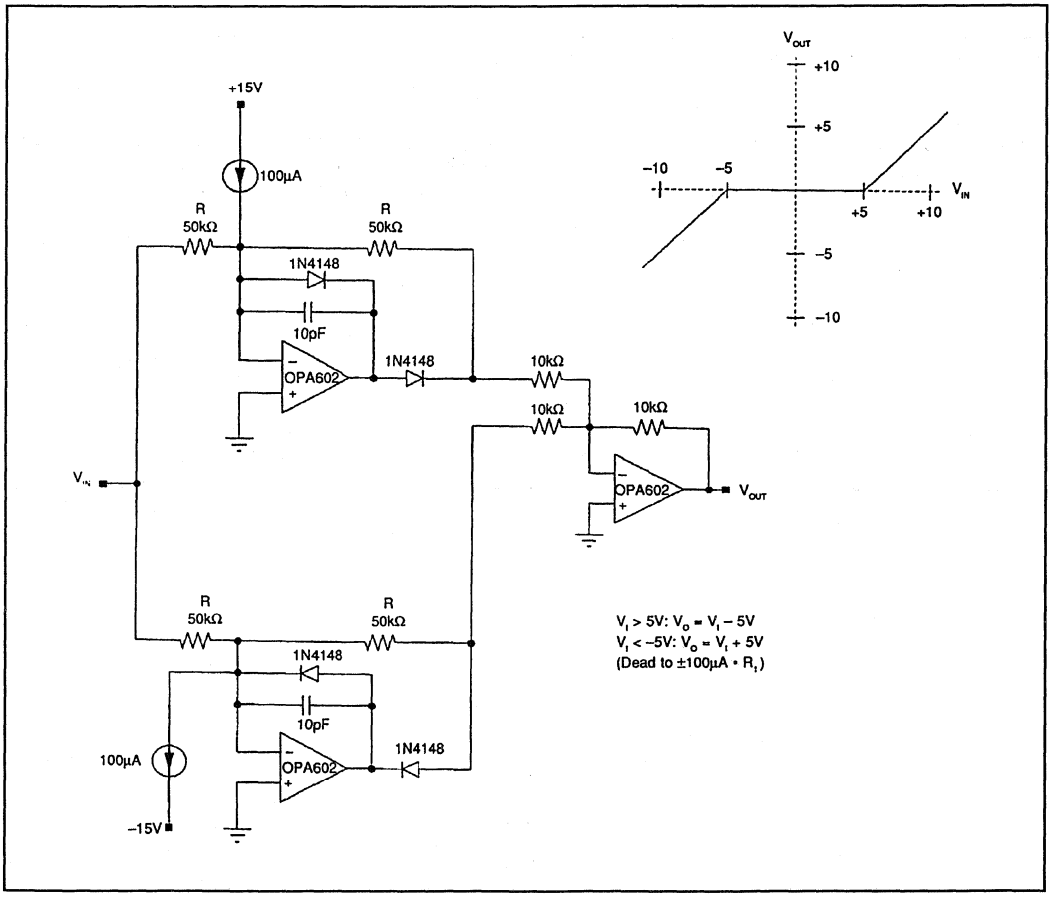


FIGURE 41. Precision double dead-band circuit.

BIDIRECTIONAL CURRENT SOURCES

One of the advantages in working with currents is that they can be steered by diodes or switches without error. As long as no current is lost through leakage, voltage drops in series with current signals do not diminish their accuracy.

The bidirectional current source shown in Figure 42 is a versatile circuit building block and an excellent example of diode steering. This two-terminal element is basically a full-wave bridge rectifier circuit with a current source connected between its DC terminals. A positive signal on the left terminal with respect to the right reverse biases D_3 and D_4 and accurately steers current through D_1 and D_2. A negative signal reverses the situation and accurately steers the same current in the opposite direction.

For one diode drop better compliance, use the bidirectional current source shown in Figure 43. The disadvantages of this circuit are that two current sources are required, and the inherent current matching of the previous circuit is lost.

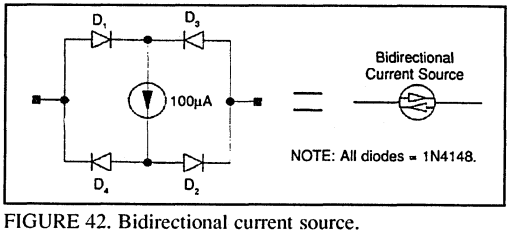


FIGURE 42. Bidirectional current source.

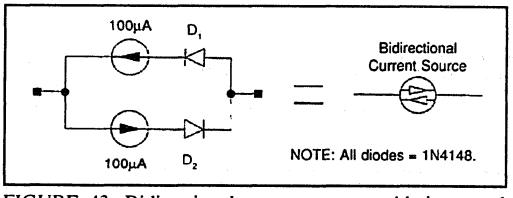


FIGURE 43. Bidirectional current source with improved compliance.

LIMITING CIRCUITS USING BIDIRECTIONAL CURRENT SOURCES

The precision double limiting circuit shown in Figure 44 puts the bidirectional current source to work. To understand how this circuit works, notice that without R_1, it functions as a precision unity-gain amplifier. The input signal is connected to the non-inverting terminal of A_1. Feedback to the inverting terminal is through the bidirectional current source, voltage-follower connected A_2, and the 1kΩ resistor. When less than 100µA is demanded from the current source, it saturates and the total voltage drop across the bidirectional current source is less than about 2V plus two diode drops. Since no current flows in the 1kΩ resistor, the circuit output voltage must equal the input voltage and errors due to A_2 and the drop across the current source are eliminated. The 1k-100pF network provides compensation for the extra phase shift in the feedback loop.

When R_1 is added, the circuit still functions as a follower for small signals where the current through R_1 is less than 100µA. When the current reaches 100µA, the current source becomes active and limits the output voltage. With the bidirectional current source, the circuit limits symmetrically in both directions.

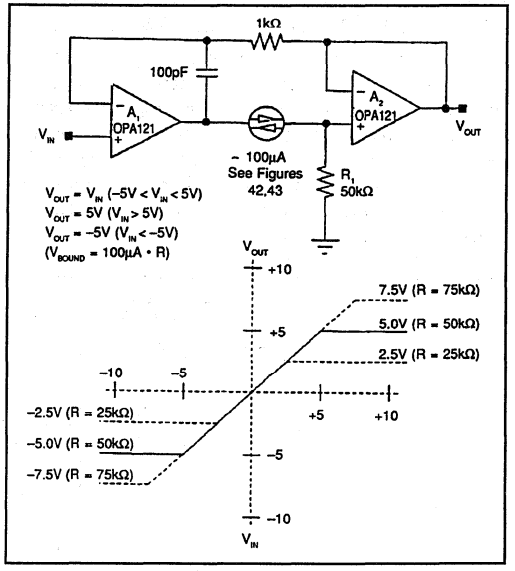


FIGURE 44. Precision double limiting circuit.

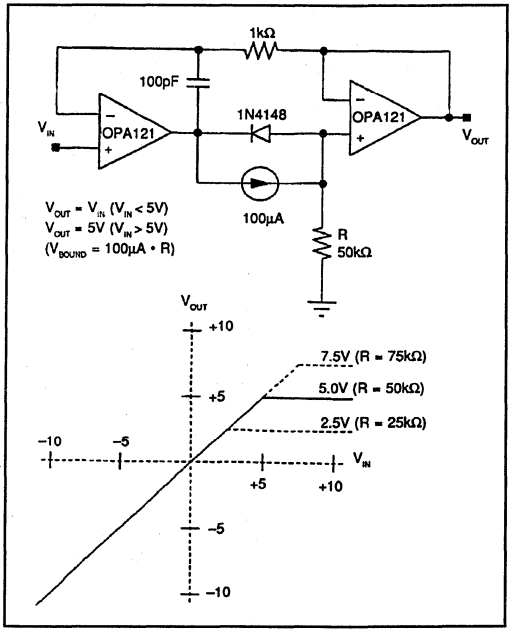


FIGURE 45. Precision limiting circuit.

If a limit in just one direction is required, replace the bidirectional current source with a current source and single diode as shown in Figure 45. For limiting in the opposite direction, reverse the polarity of the current source and diode.

PRECISION TRIANGLE WAVEFORM GENERATOR USING BIDIRECTIONAL CURRENT SOURCES

The precision triangle waveform generator shown in Figure 46 makes use of two bidirectional current sources. One steers a precision current signal into the integrating capacitor connected to the inverting input of the op amp. The other steers a precision current into the 10kΩ resistor connected to the positive op amp terminal to provide ±1V hysteresis. The result is a relaxation oscillator with precision triangle and square wave outputs of ±1V.

DUTY CYCLE MODULATOR USING BIDIRECTIONAL CURRENT SOURCES

The precision duty cycle modulator shown in Figure 47 is a variation of the triangle generator. Here the integrating capacitor is replaced by a true integrator formed by A_1 and C. This allows the summation of a ground referenced signal through the 100kΩ input resistor. With no input signal, the output is a square wave with 50% duty cycle. Input signals sum into the integrator through the 100kΩ resistor. The integrator then slews faster in one direction, and slower in the other. The result is a linear duty cycle modulation of the output signal. The modulator is said to be duty cycle rather than pulse width because the output frequency varies somewhat with input signal. For a constant frequency duty cycle modulator add a resistor in series with the inverting input of A_2 and drive that input with a resistor coupled clock signal.

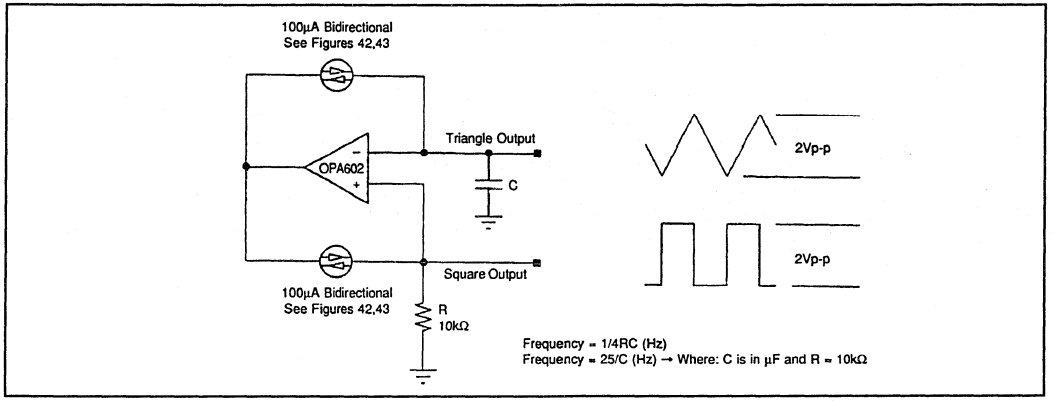


FIGURE 46. Precision triangle waveform generator.

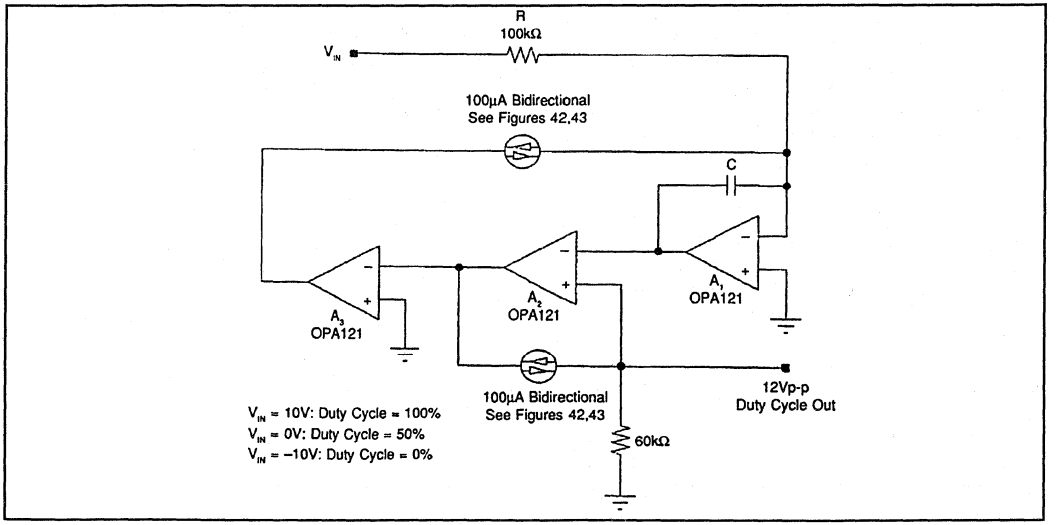


FIGURE 47. Precision duty-cycle modulation circuit.

Notice that the duty-cycle modulator has a true integrating input. This is in contrast to conventional modulators which simply use a comparator connected between the input signal and a precision triangle wave. With the conventional approach, at crossing, input noise feeds through at the comparator bandwidth resulting in jitter. Not only does the integrating input filter out input noise, it can be synchronized to input noise (such as 60Hz), completely notching out its effect. If integration takes place over one or more complete cycles of the noise signal, the undulations of the noise signal are exactly averaged out.

SLEW RATE LIMITER

In some applications, especially when driving inductors, it is necessary to limit the signal slew rate. The rate limiting circuit shown in Figure 48 uses a diode bridge for current steering in a different way. Here two current sources are connected, one to the positive terminal and one to the negative terminal, of the bridge. Without the capacitor, the circuit would act as a unity gain inverting amplifier. Feedback through the 10kΩ – 10kΩ resistor network drives the left side of the bridge. The right side of the bridge follows, driving the op amp inverting input. Voltage offset due to diode mismatch can be mitigated by using a monolithic bridge such as the one specified. When the integrator capacitor is added, charging and discharging current must flow to maintain the virtual ground. But when that current exceeds 100µA, the bridge reverse biases limiting the output slew rate to 100µA/°C regardless of input signal rate.

SINGLE SUPPLY INSTRUMENTATION AMPLIFIER

Single power supply systems are common and the need for instrumentation amplifiers (IAs) to operate in this environment is critical. While single supply op amps have been available for many years, single supply IAs have not. What's more, single supply IAs can not be made by simply using single supply op amps in the traditional manner. In a conventional IA topology the outputs as well as the inputs would need to swing to the negative rail. Although some op amps come close, no amplifier output can swing all the way to its power supply rail, especially when driving a load.

The single supply IA circuit shown in Figure 49 solves this problem by simply level shifting the input signal up by a Vbe with a matched pair of matched PNP input transistors. The transistors are biased as emitter followers by the 100µA current sources in a REF200. The ensuing circuit is a traditional three op amp IA. OPA1013s are used for input amplifiers because they are designed for single supply operation and their output can also swing near the negative rail. The Burr-Brown INA105 is used as a difference amplifier. All critical resistor matching is taken care of by the INA105. The common mode range of the single supply IA typically extends to 0.5V below the negative rail with a typical CMR better than 86dB.

VOLTAGE CONTROLLED CURRENT SOURCE USING INA105

The modified Howland current pump (Figures 50-52) is an extremely versatile voltage controlled current source. Since it has differential inputs, you can ground one input and drive the other to get either an inverting or noninverting transfer function. If you drive both inputs, the output current will be proportional to the voltage difference between the inputs.

What's more, unlike current sources made with a series pass element, which can either sink or source current, this current source has a bipolar output. It can both sink and source current.

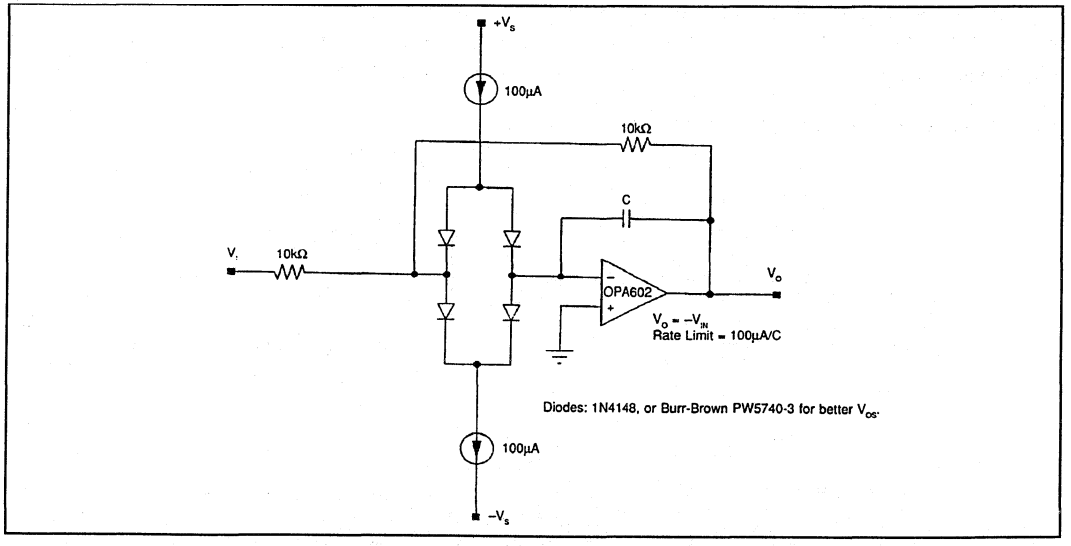


FIGURE 48. Rate limiting circuit.

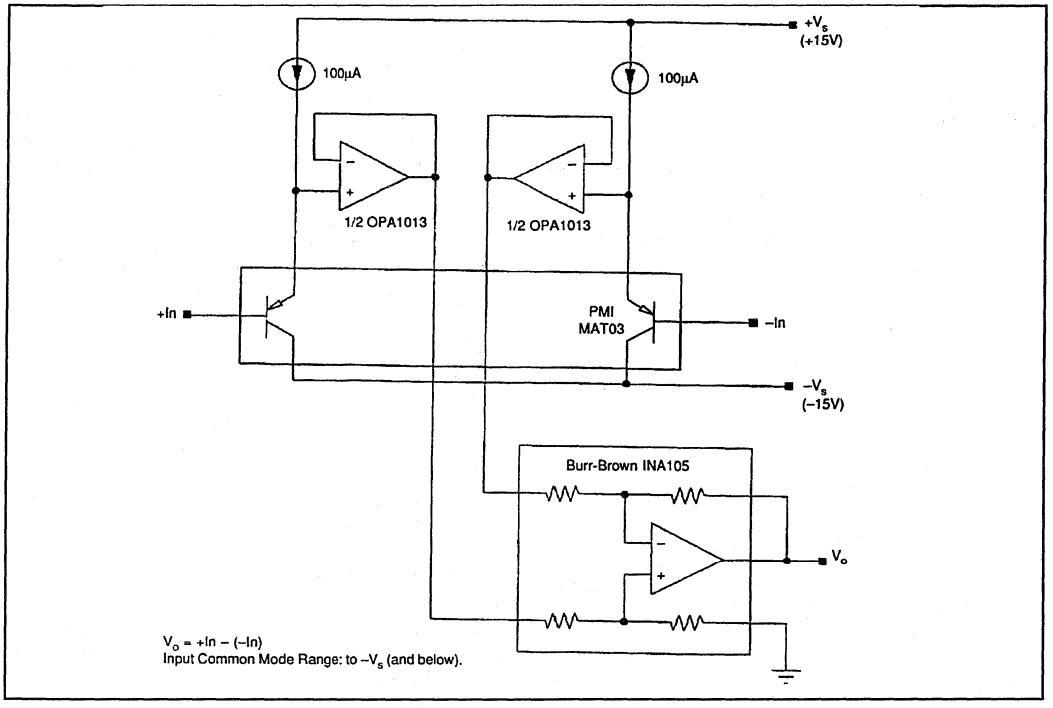


FIGURE 49. Single-supply instrumentation amplifier.

Use of this circuit was limited in the past due to the critical resistor matching and resistor TCR tracking requirements. By using the INA105 difference amplifier, the circuit can be easily implemented with the addition of two 1% resistors. Matching of the external resistors is important, but since they add to the internal 25kΩ resistors, the matching requirement is divided down by the ratio of resistance.

Output impedance of the current source is proportional to the common mode rejection (CMR) of the difference amplifier. Mismatch of feedback resistors in the difference amplifier caused by the external resistors will degrade CMR and lower the current source output impedance. Resistor match of 0.002% is required for 100dB CMR in a unity gain difference amplifier. Depending on the value of the external resistor and output impedance requirement, it may be necessary to trim the external resistor.

When the value of the external resister becomes large consider the alternate circuit shown in Figure. 51.

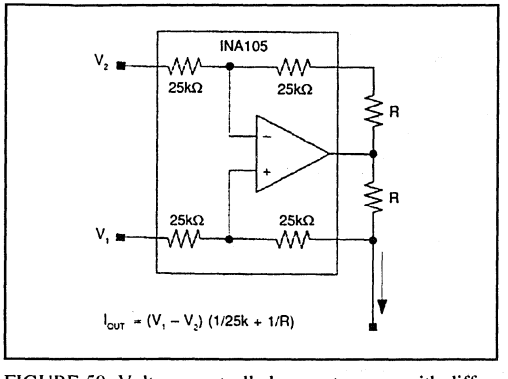


FIGURE 50. Voltage-controlled current source with differential inputs and bipolar output.

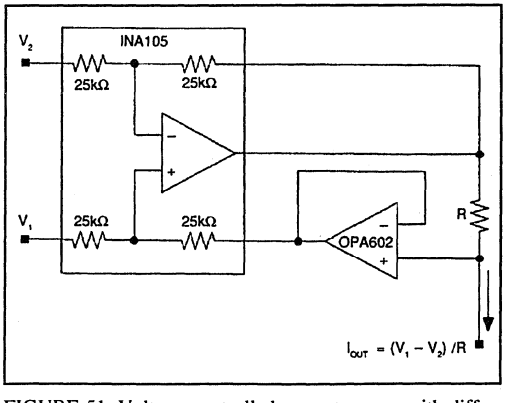


FIGURE 51. Voltage-controlled current source with differential inputs and bipolar output and circuit to eliminate feedback resistor error.

You need an extra amplifier to drive the feedback resistor in the difference amplifier, but only one external resistor is required, and no matching or trimming is needed.

In any case the output impedance of the current source can be approximated by the following relationship:

$$Z_o = R_x \bullet 10^{[CMRR/20]}$$

Where:

Z_o = equivalent output impedance of current source [Ω]

CMRR = difference amp common mode rejection ratio [dB]

(for Figure 50)

R_x = parallel combination of external resistor and 25kΩ

$$R_x = \frac{R \bullet 25k\Omega}{R + 25k\Omega}$$

(for Figure 51)

R_x = external resistor [Ω]

The INA105 can source 20mA and sink 5mA. If higher output current is required, add a current buffer as shown in Figure 52. The OPA633 shown allows output currents up to ±100mA. Since the buffer is within the feedback loop, its DC errors have no effect on the accuracy of the current source. When using other buffers make sure that their bandwidth is large enough not to degrade circuit stability.

If you want voltage gain in the voltage to current converter, use the INA106 for a gain-of-ten difference amplifier.

Don't forget that source impedance adds directly to the input resistors of the difference amplifier which can degrade its performance. A source impedance mismatch of 5Ω will degrade the CMRR of the INA105 to 80dB. If you are driving the circuit from an amplifier or other low impedance source, this should not be a problem. If you have higher source impedances, buffer the driven input(s) of the difference amplifier, or use an instrumentation amplifier such as the INA110 instead of a difference amplifier.

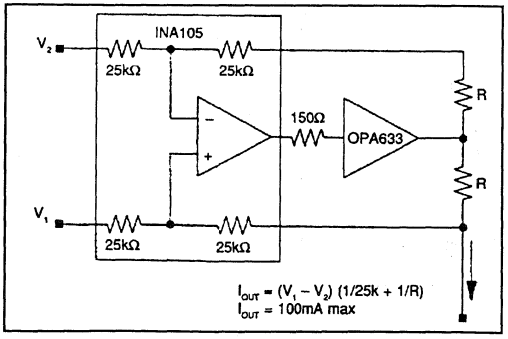


FIGURE 52. Voltage-controlled current source with differential inputs and current boosted bipolar output.

VOLTAGE CONTROLLED CURRENT SOURCE WITH INSTRUMENTATION AMPLIFIER INPUT—THE XTR101

The XTR101 is a floating current source designed for two wire 4-20mA current loop applications. It is a voltage controlled current source with a precision instrumentation amplifier input. It also contains two matched 1mA current sources which makes it suited for remote signal conditioning of a variety of transducers such as thermocouples, RTDs thermistors, and strain gauge bridges.

Figure 53 shows the XTR101 connected as a temperature controlled current source. The temperature sensing element is a thermocouple, and cold junction compensation is provided by the diode.

The product data sheet for the XTR101, (PDS-627) gives operating details for the device and shows several other applications.

SINGLE SUPPLY VOLTAGE CONTROLLED CURRENT SOURCE—THE XTR110

The XTR110 is a precision single supply voltage to current converter. Although it is designed specifically for three wire 4-20mA current transmission it can also be used in more general voltage to current source applications. As shown in Figure 54, it contains: a precision 10.0V reference and input resistor network for span offsetting (0V In = 4mA Out), a voltage to current converter for converting a ground referenced input signal to an output current sink, and a current mirror for turning the output of the current sink into a current source.

The current mirror has a gain ratio of 10:1 and uses an external pass transistor to minimize internal thermal feedback and improve accuracy. Since the mirror transistor is external, an external mirror ratio setting resistor can be added for an arbitrarily high output current.

Both the voltage to current converter, and the current mirror use single supply op amps so that the input and output signals can go to zero. In the case of the mirror op amp, the common mode range goes to the positive power supply rail rather than common.

The following table shows a range of input-output spans that is available simply by pin strapping the XTR110.

Input Range (V)	Output Range (mA)	Pin 3	Pin 4	Pin 5	Pin 9	Pin 10
0-10	0-20	Com	Input	Com	Com	Com
2-10	4-20	Com	Input	Com	Com	Com
0-10	4-20	+10	Input	Com	Com	Open
0-10	5-25	+10	Input	Com	Com	Com
0-5	0-20	Com	Com	Input	Com	Com
1-5	4-20	Com	Com	Input	Com	Com
0-5	4-20	+10	Com	Input	Com	Open
0-5	5-25	+10	Com	Input	Com	Com

For more details and applications, request product data sheet PDS-555.

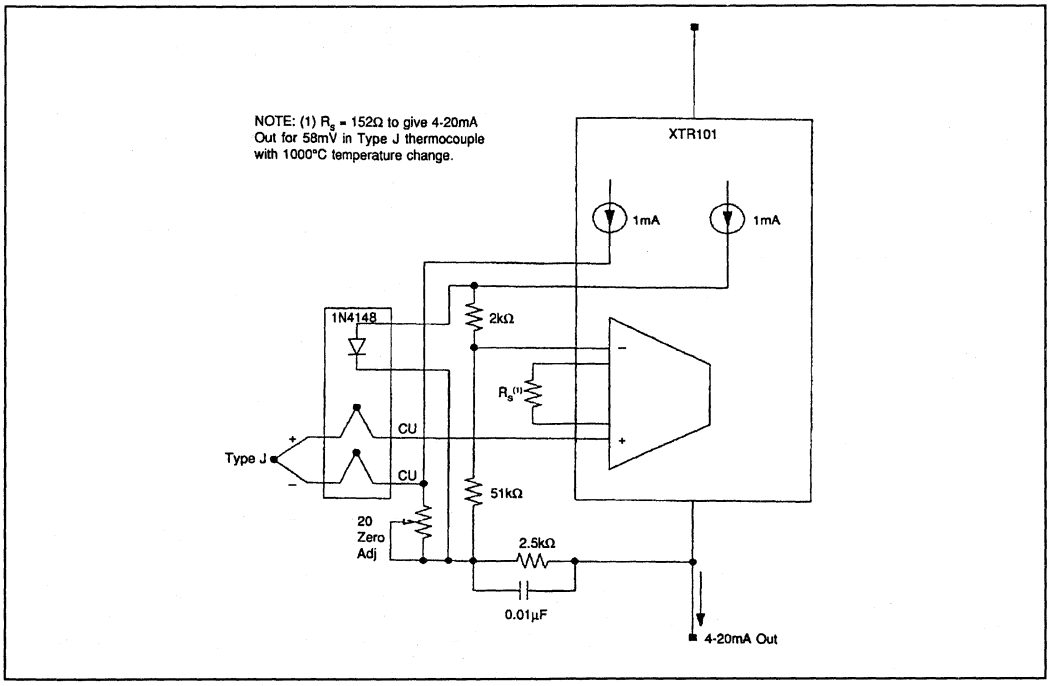


FIGURE 53. Temperature-controlled current source using XTR101.

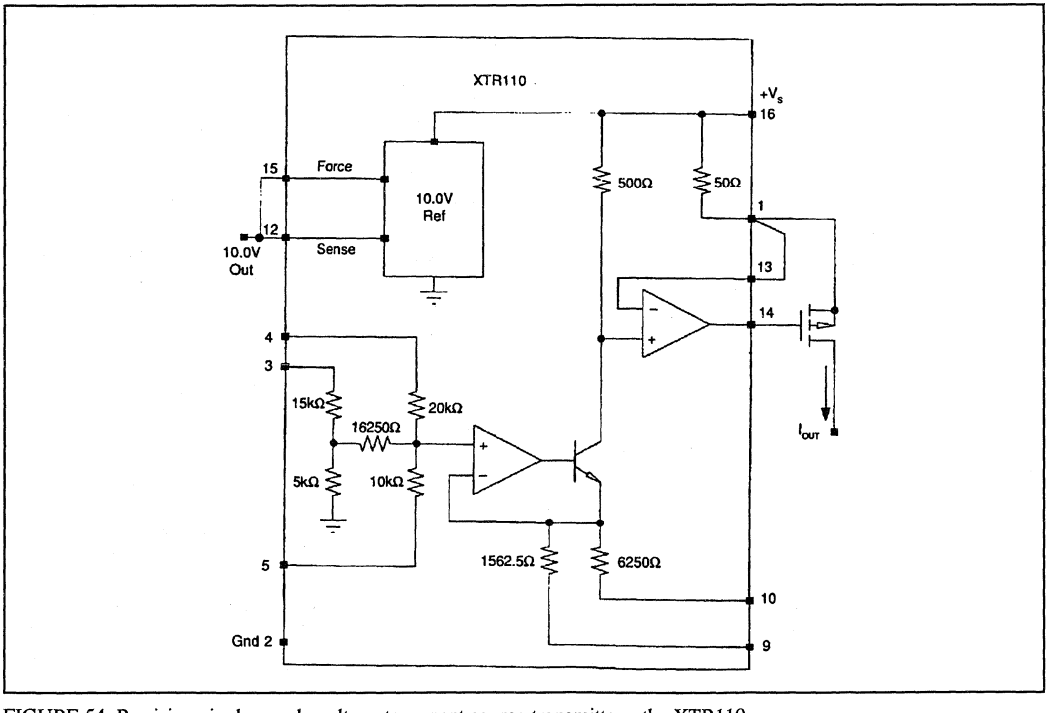


FIGURE 54. Precision single-supply voltage-to-current source transmitter—the XTR110.

CURRENT RECEIVER WITH COMPLIANCE TO BOTH POWER SUPPLY RAILS USING THE INA105

Measuring current signals can be as simple as feeding the current into a precision resistor (V = I • R). If needed, the voltage developed across the resistor can be buffered or amplified with an operational amplifier.

If common-mode signals are present on the current return end of the sense resistor, an instrumentation amplifier (IA) can be used to reject the common mode signal and reference the output signal to ground. However, a limitation of conventional IAs is that their common mode input range is limited to less than 10V.

When you need to reference the current return of the sense resistor to a higher common mode voltage, consider one of the following difference amplifiers.

Model	Input Common Mode Range	Other Features
	(1)	
INA105	± 20V	
INA117	±200V	
RCV420	± 40V	(2)

NOTES: (1) Common-mode input range specified for operation on standard ±15V power supplies. (2) Also contains a precision reference and offsetting circuitry to get 0-5V outputs with 4-20mA inputs.

Figure 55 shows a current receiver using the INA105. The input current signal is sensed across 100Ω resistor, R_S, connected to the negative power supply rail. Connecting the sense resistor to a power supply rail instead of ground maximizes the voltage drop available across the current transmitter.

Voltage divider action of the feedback resistors within the INA105 divide the common-mode input by two. Therefore, common mode input signals of up to ±20V are attenuated to an acceptable level of no more than ±10V at the op amp inputs.

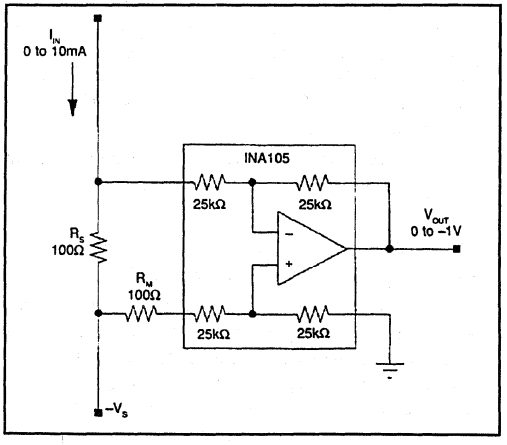


FIGURE 55. Current-to-voltage converter referenced to the negative power supply rail.

Matching resistor, R_M, preserves the resistance match of the INA105 and maintains its high common-mode rejection (CMR). Because 100Ω is small compared to the 25kΩ difference resistors, a 1% tolerance is sufficient to maintain 86dB CMR.

The INA105 references the output signal to ground with a gain of one. For a 0-10mA input the output is 0 to −1V (a transfer function of −100V/A). If a positive transfer function is desired, interchange the input pins of the difference amplifier. To reference current signals to the positive rail, simply connect the sense resistor and the other difference amplifier input to that point.

The 25kΩ input impedance of the difference amplifier causes a slight error by shunting a portion of the input current signal. In the noninverting configuration, the matching resistor lowers the difference amplifier gain, but since the shunting input impedance of the noninverting input is 50kΩ, for a unity gain difference amp, the error turns out to be the same. For a 100Ω sense resistor, the error is a approximately 0.4%. For better accuracy, select a slightly higher value sense resistor to compensate for the error according to the following equation.

$$R_S = R_M = \frac{25k \cdot X}{25k - X}$$

Where:
X = desired transfer function [V/A]

For example:
For 1V/10mA (100V/A) from Figure 55:
$R_S = R_M = 100.4\Omega$

POWER AMP LOAD CURRENT MONITORING USING THE INA105 OR THE INA117

The INA117 is a difference amplifier similar to the INA105 except that it has a 20/1 input divider allowing a ±200V common mode input range. It also has an internal gain of 20 providing an overall gain of one. The penalty is that amplifier DC errors, and resistor and amplifier noise are amplified by 20. Still for 200V applications that do not require galvanic isolation its has better performance than isolation amplifiers, and it does not require an isolated power supply.

Figure 56 shows a circuit for measuring load current in a bridge amplifier application using the INA117. At low frequencies, a sense resistor could be inserted in series with the load, and an instrumentation amplifier used to directly monitor the load current. However, under high frequency or transient conditions, CMR errors would limit accuracy. This approach eliminates these problems by gleaning the load current from measurements of amplifier supply current.

The power supply current of one of the bridge op amps is measured using INA117s and 0.2Ω sense resistors connected to the power supplies. Because the 0.2Ω sense resistor adds negligible resistance error to the 380kΩ input resistors of the INA117s, no matching resistors are required.

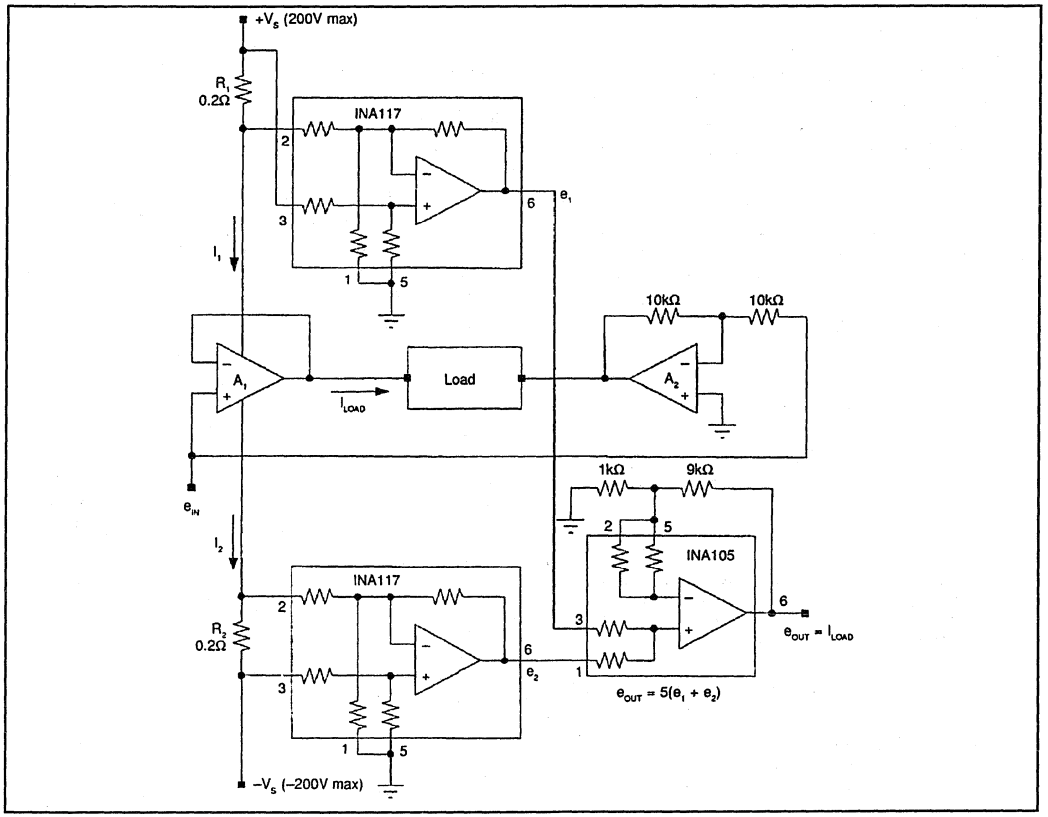


FIGURE 56. Bridge amplifier load current monitor using the INA117.

To understand how the circuit works, notice that since no current flows into the inputs of A_1:

$I_{LOAD} = I_1 - I_2$

If

$R_1 = R_2 = R$

Then

$e_1 = I_1 \cdot R$,

$e_2 = -I_2 \cdot R$,

and

$e_1 + e_2 = I_{LOAD} \cdot R$

The INA105 is connected as a noninverting summing amplifier with a gain of 5 (the accurate matching of the two 25kΩ input resistors makes a very accurate summing amplifier).

Then

$e_O = 5(e_1 + e_2) = 5(I_{LOAD} \cdot R)$,

since

$R = 0.2\Omega$,

$e_O = I_{LOAD}$ [1V/A]

4 to 20mA CURRENT LOOP RECEIVER WITH 0 to 5V OUTPUT USES THE RCV420

The RCV420 is a current-to-voltage converter designed specifically for conversion of 4-20mA input currents into 0-5V outputs. A pair of precision 75Ω sense resistors are provided internally allowing both inverting and noninverting transfer functions. Input common mode signals up to ±40V can be accommodated due to the internal 4/1 input attenuator. Also, the precision 10.0V reference used for span offseting is available to the user.

Figure 57 shows a typical application. For more details and applications, request product data sheet PDS-837.

VIRTUAL GROUND CURRENT-TO-VOLTAGE CONVERTER

When current-to-voltage conversion with no voltage burden is needed, used the transimpedance amplifier Figures 58—61. In this circuit, an op amp drives the current input node to virtual ground by forcing a current equal to I_{IN} through the feedback resistor, R_{FB}. Notice that the transfer function is inverted:

$$V_{OUT} = -I_{IN} \cdot R_{FB}$$

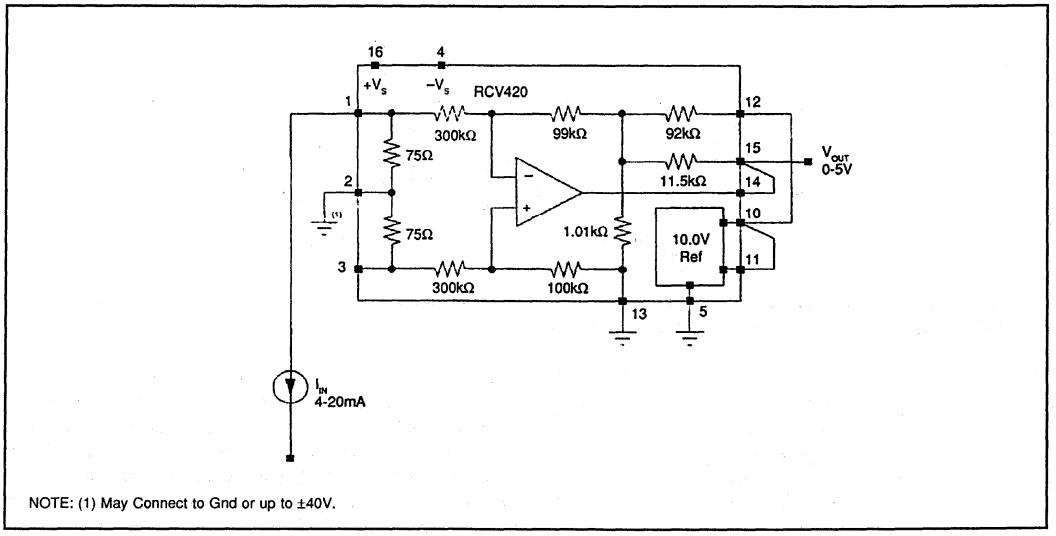


FIGURE 57. 4-20mA current loop receiver using the RCV420.

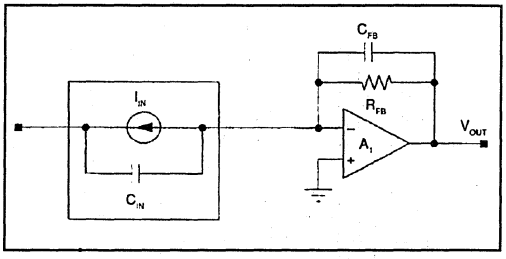


FIGURE 58. Virtual ground current-to-voltage converter.

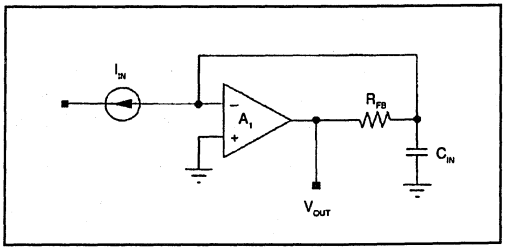


FIGURE 59. Virtual ground current-to-voltage converter redrawn to Illustrate phase delay due to input capacitance and feedback resistor.

The feedback capacitor, C_{FB}, may be needed for circuit stability. To see why, consider the redrawn circuit, Figure 59. C_{IN} represents the input capacitance of the circuit and includes input source capacitance, and op amp input capacitance. Notice that R_{FB} and C_{IN} form a single pole filter in the feedback path to the op amp input. Phase delay through this circuit subtracts from the op amp phase margin which may result in instability, especially with the large values of R_{FB} often used in these circuits. If $C_{FB} \geq C_{IN}$, the phase delay will be less than 20° assuring stability with most unity-gain-stable amplifiers.

PHOTODIODE AMPLIFIER USING VIRTUAL GROUND I/V CONVERTER

The photodiode amplifier shown in Figure 60 is a common application of the transimpedance (current-to-voltage) amplifier. In this application, the shunt capacitance of the photodiode reacting with the relatively large feedback resistor creates excess noise gain. The 1pF feedback capacitor minimizes the peaking and improves stability as discussed previously. Capacitors with the small values often required may be difficult to obtain. By using a capacitor divider circuit shown in Figure 60A, a larger value capacitor can be used. In this example, the 10pF capacitor, C_1, is reduced to an effective value of 1pF by the R_4, R_5 10/1 divider. The 100 pF capacitor, C_3, keeps the Impedance of the divider low beyond the C_1, $R_4 \parallel R_5$ zero to maintain C_1's effect. It also produces a second-order (40dB/decade) roll-off approximately one decade beyond the $C_1/10$, R_2 pole.

The addition of two passive components to the standard configuration as shown in Figure 61 introduces a second pole that significantly reduces noise. The modification also has other advantages.

The added pole of the improved circuit is formed with R_3 and C_2. Because the pole is placed within the feedback loop, the amplifier maintains its low output impedance. If the pole were placed outside the feedback loop, an additional buffer would be required. The extra buffer would add additional noise and DC error.

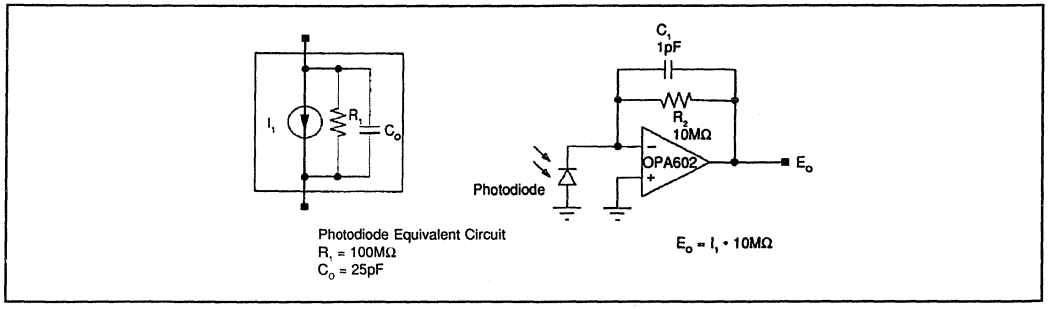


FIGURE 60. Standard transimpedance photodiode amplifier.

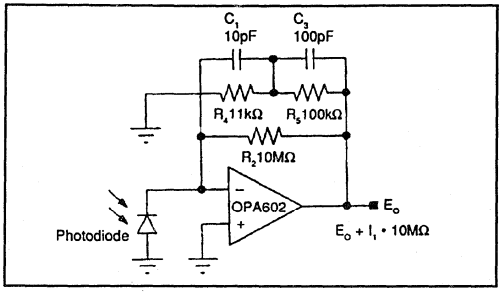


FIGURE 60A. Standard Transimpedance Amplifier with capacitor divider and added feedback pole.

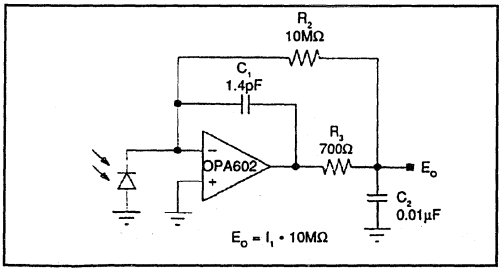


FIGURE 61. Improved transimpedance photodiode amplifier.

The signal bandwidth of both circuits is 16kHz:

$$f_{-3dB} = \frac{1}{2 \cdot \pi \cdot R_2 \cdot C_1} \text{ [Hz]} \rightarrow \text{standard circuit}$$

$$f_{-3dB} = \frac{1}{2 \cdot \pi \cdot (R_2 \cdot C_1 \cdot R_3 \cdot C_2)^{1/2}} \text{ [Hz]} \rightarrow \text{improved circuit}$$

Where, for the improved circuit:
$C_1 \cdot R_2 = 2(C_2 \cdot R_3)$
and $R_2 >> R_3$

In the standard circuit, a single 16kHz pole is formed by the 1pF capacitance in the feedback loop. The improved circuit exhibits two pole response. With $C_1 \cdot R_2 = 2 \cdot C_2 \cdot R_3$, the transfer function is two pole Butterworth (maximally flat in the passband). Figure 62 shows the transimpedance frequency response of the two circuits. At DC, the gain is 140dB or 10V/µA. The frequency response of both circuits is 3dB down at 16kHz. The conventional circuit rolls off at 20dB/decade, while the improved circuit rolls off at 40dB/decade.

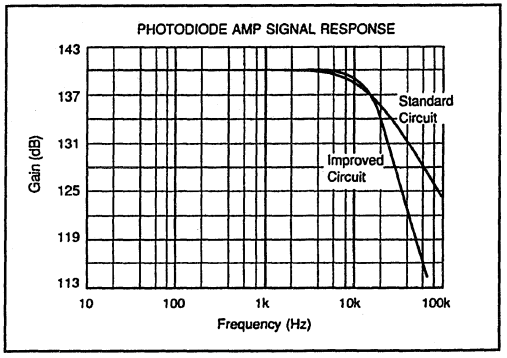


FIGURE 62. Transimpedance signal response of standard and improved photodiode amplifier.

Figure 63 shows the noise gain of both circuits. The noise problem is due to the noise gain zero formed by the relatively high photodiode shunt capacitance, C_D, reacting with the high 10MΩ feedback resistor. The noise zero occurs at:

$$f_Z = \frac{(R_1 + R_3)}{2 \cdot \pi \cdot R_1 \cdot R_3 \cdot (C_D + C_1)} \sim 673\text{Hz in this example.}$$

Both curves show peaking in the noise gain at about 673Hz due to the zero formed by the photodiode shunt capacitance. The added pole of the improved circuit rolls off the noise gain at a lower frequency, which reduces the noise above 20kHz. Since the signal bandwidth is 16kHz, the region of the spectrum above 20kHz contains only noise, not signal. With the values show, the improved circuit has 3 times less noise. With the OPA602 (voltage noise = $12nV/\sqrt{Hz}$), and including resistor noise, the improved circuit has 1Hz to 100MHz noise of 68µVrms vs 205µVrms for the standard circuit.

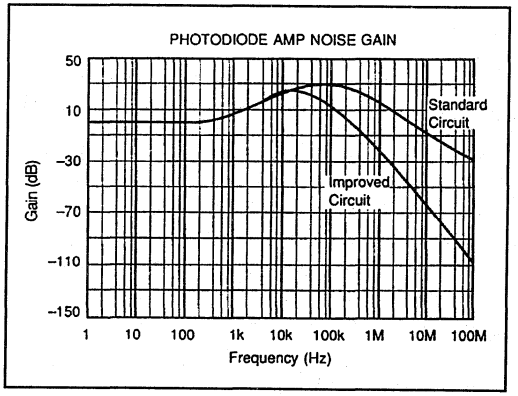


FIGURE 63. Noise gain of standard and improved photodiode amplifier.

Another advantage of the improved circuit is its ability to drive capacitive loads. Since the output of the circuit is connected to a large capacitor, C_2, driving a little extra capacitance presents no stability problems. Although the circuit has low DC impedance, the AC transfer function is affected by load. With reasonable loads, the effect is minimal. With the values shown, a load of 10kΩ in parallel with 100pF has little effect on circuit response.

For applications where the photodiode can be floated consider the noninverting I/V converter shown in Figures 64 and 65. Notice that the buffer amplifier forces zero volts across the photodiode as in the conventional transimpedance amplifier configuration.

FET input amplifiers are commonly used for photodiode amplifier applications because of their low input bias currents. However, FET amplifier bias currents increase dramatically at high temperatures (doubling approximately every 8 to 10°C). Seemingly small input bias currents at 25°C can become intolerable at high temperature. An amplifier with only 1pA bias current at 25°C could have nearly 6nA bias current at 125°C.

The difference between input bias currents, offset curent, is often much better than the absolute bias current. The typical bias current of an OPA156, for example, is 30pA, while its offset current is 3pA.

If amplifier bias current is a problem consider the circuit shown in Figure 66. The added bias current cancellation resistor R_2 cancels the effect of matching op amp input bias currents. This can provide a ten-to-one or better improvement in performance since voltage offset is due only to I_{OS} (offset current) reacting with 5MΩ.

A word of caution. Many amplifiers, especially bipolar input amplifiers, achieve low bias current with internal bias current cancellation circuitry. There may be little or no difference between their I_B and I_{OS}. In this case external bias current cancellation will not improve performance.

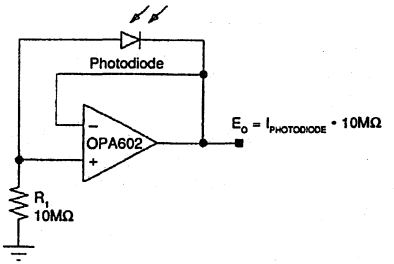


FIGURE 64.

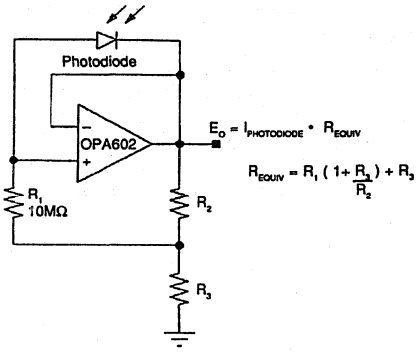


FIGURE 65.

FIGURES 64 and 65. Photodiode amplifier using floating virtual ground current-to-voltage converter.

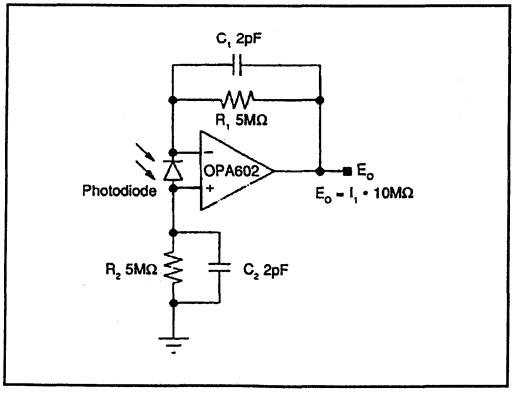


FIGURE 66. Differential Photodiode Transimpedance Amplifier gives bias current cancellation.

GLOSSARY

ABBREVIATIONS, DEFINITIONS

Bidirectional Current Source—A floating current source that provides a constant current independent of the polarity of applied voltage bias.

Current Source—This may be a general term for any current source, current sink, or floating current source. In this text it usually refers to a current generating device referenced to a positive fixed potential such as $+V_S$ of a power supply. The load must be connected between the current source and a more negative potential.

Current Sink—Current generating device referenced to a negative fixed potential such as $-V_S$ of a power supply. The load must be connected between the current sink and a more positive potential.

Difet®—Burr-Brown's trademark for an integrated circuit process which uses dielectric (DI) instead of reverse biased junctions (JI) to isolate devices. This technique eliminates the substrate leakage inherent in JI processes. The result is lower input bias currents for FET input amplifiers, and potential for higher temperature operation and radiation hardness.

Floating Current Source—A current generating device with both ends uncommitted. The load may be connected to either end, or a floating current source may be connected arbitrary between two loads. The current sources in the REF200 are floating current sources. A floating current source may require external power supplies. The floating current sources in the REF200 are self powered, and require no external power supply.

IA—Instrumentation Amplifier. An IA is not an op amp. Unlike an op amp, an IA amplifies the signal at its inputs by a fixed gain while rejecting the common mode signal. An op amp amplifies the signal at its inputs by its open loop gain (ideally infinity). An op amp therefore requires feedback components to make a useful amplifier. It normally takes three op amps and seven precision resistors to make an IA.

I_B—Bias current. The DC current that flows into or out of the input terminals of an amplifier.

IC—Integrated circuit. Often implies monolithic integrated circuit, which is a single-chip electronic circuit.

I_{OS}—Offset current. The difference in I_B of the two inputs of an amplifier.

Op Amp—Operational amplifier. An operational amplifier is a very high gain direct current amplifier with differential inputs. It is intended for applications where the transfer function is determined by external feedback components.

RTD—Resistor Temperature Device. A precision temperature transducer using platinum as the active element. Values at 0°C of 100Ω, 500Ω, and 1000Ω are standard. Due to the high cost of platinum 1kΩ RTDs are becoming more popular.

TCR—Temperature coefficient of resistance. The change of DC resistance with temperature of a resistor. Usually expressed in parts per million per °C [ppm/°C].

TCR Tracking—The match or tracking over temperature of the TCR of two or more resistors.

Transconductance Amplifier—A voltage to current converter.

Transimpedance Amplifier—A current to voltage converter. (Sometimes called transadmittance).

BURR-BROWN® APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

VOLTAGE-TO FREQUENCY CONVERTERS OFFER USEFUL OPTIONS IN A/D CONVERSION

Specialized Counting Techniques Achieve Improved Speed and Resolution

Voltage-to-frequency converters (VFCs) provide unique characteristics when used as analog-to-digital (A/D) converters. Their excellent accuracy, linearity, and integrating input characteristics often provide performance attributes unattainable with other converter types. By using efficient frequency counting techniques, familiar speed/accuracy tradeoffs can be averted.

Since an analog quantity represented as a frequency is inherently a serial data stream, it is easily handled in large multichannel systems. Frequency information can be transmitted over long lines with excellent noise immunity using low cost digital line transmitters and receivers. Voltage isolation can be accomplished with low cost optical couplers or transformers without loss in accuracy. Many channels of frequency data can be efficiently steered to one counter circuit using simple digital gating, avoiding expensive analog multiplexing circuitry.

Like a dual-slope A/D converter, the VFC possesses a true integrating input. While a successive approximation A/D converter takes a "snapshot" in time, making it susceptible to noise peaks, the VFC's input is constantly integrating, smoothing the effects of noise or varying input signals.

When system requirements suggest the VFC as an appropriate choice, a frequency measurement technique must also be chosen which meets the conversion speed requirements.

While it is clearly not a "fast" converter, conversion speed of a VFC system can be optimized by using efficient counting techniques.

The frequency counting scheme shown in Figure 1 is the most commonly used technique for converting the output of a VFC to a numerical quantity. A gate time is created by dividing a reference frequency down to a suitable period, T. The output pulses of the VFC are simply accumulated during the time the gate signal is high. If T is equal to one second, for instance, the output count M is equal to the VFC frequency. Other gate periods (often 0.1 seconds, 10 seconds, etc.) are conveniently scaled by a decimal point shift or a simple multiplying factor. The reset circuitry which must be used to clear the counter before the next gate period occurs is not shown in this simplified diagram.

Since the gate period is not synchronized to the VFC output pulses, there is a potential counting inaccuracy of plus or minus one count on M. This is easily seen by imagining a sliding window of width T along the VFC output waveform.

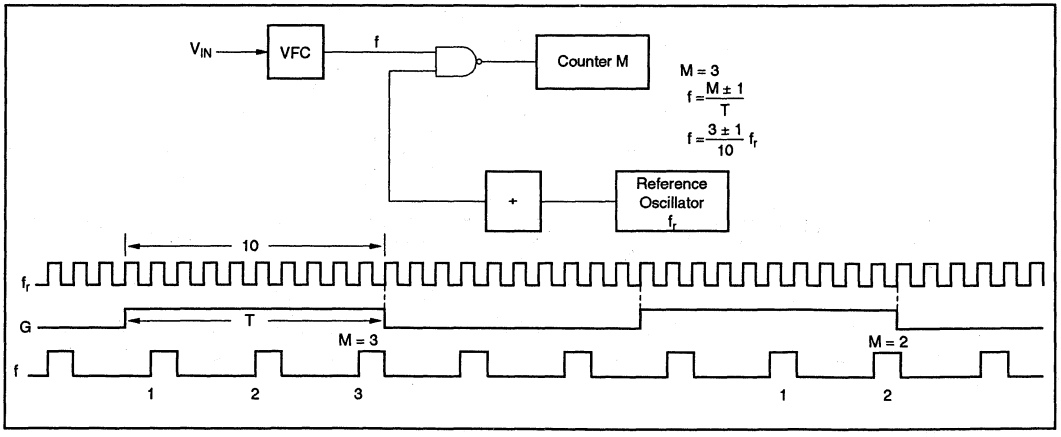


FIGURE 1. This Simplified Diagram of the Standard Counting Method Shows the Potential Inaccuracies That Can Occur. Although the first gate counts three rising edges of the VFC output frequency, f, the second gate period counts only two.

Counting the rising edges which are seen in that period, you can see how, depending on the VFC frequency, a + one count error can occur.

The resolution which can be achieved by this method is related to the gate period, T, times the full-scale frequency of the VFC. This is equal to the number of counts, M, at full scale. Many applications require relatively fast conversions (short gate periods) with high resolution. This can only be accomplished by the use of a high full-scale frequency. This is an effective solution in many cases, but since VFC linearity degrades at high operating frequency, this often limits the available accuracy.

The ratiometric counting technique shown in Figure 2 (sometimes called reciprocal counting) eliminates this tradeoff. By counting N counts of a high speed clock which occur during an exact integer M counts of the VFC, an accurate ratio or the unknown VFC frequency to the reference (f_R) is determined.

This is accomplished by using a D flip-flop clocked with the VFC output. A new, synchronized gate period is created which is an exact number of VFC pulses in duration. In contrast to the standard counting approach which has a plus or minus one count error on M, the synchronized gate precisely counts an integer number of VFC pulses. During the same synchronized gate period, high speed clock pulses are counted. Since these high speed clock pulses are not synchronized with the gate, this count has a plus or minus one count error. High resolution is achieved by making the reference oscillator a high frequency so the N count is a large number. The one count error can then be made to have a small effect on the result.

The additional resolution of this counting technique means that for a given conversion speed, the VFC can now be operated at a low frequency where its linearity and temperature drift are excellent. Again, reset and control circuitry have not been shown to clearly illustrate the fundamentals of the technique.

The resulting two counts (M and N) are divided to achieve the result of an individual conversion. This can be done in a host processor or microcontroller along with the offsetting and scaling that often must be performed.

An example of a A/D system design using a VFC is shown in Figure 3. It uses a VFC110 to convert a 0 to 10V input into a 10kHz to 100kHz output by offsetting the VFC input with a reference voltage. The 5V reference sets a constant input current through R_1 which is added to the signal input current through R_{IN}. Since the synchronized gate awaits complete cycles of the VFC to achieve an exact count, a very-low VFC frequency would cause the synchronized gate period to be excessively long. The offset at the VFC input allows 10kHz (corresponding to 0V input) to be counted during the desired conversion time.

All counter functions are provided by a type 8254 counter/timer peripheral component which interfaces to many popular microprocessor systems. It contains three 16-bit counters which can be programmed for a variety of functions. Counter C2 provided the timing necessary to generate the gate signal "G". A rising logic edge at the Convert input initiates the conversion cycle. This causes FF1 to latch "high" Counter. C2 is programmed and loaded to count 59,667 clock pulses (3.58MHz clock), then reset FF1. This creates a 16.66ms(1/60s) gate period at "G". FF2 synchronizes the gate signal

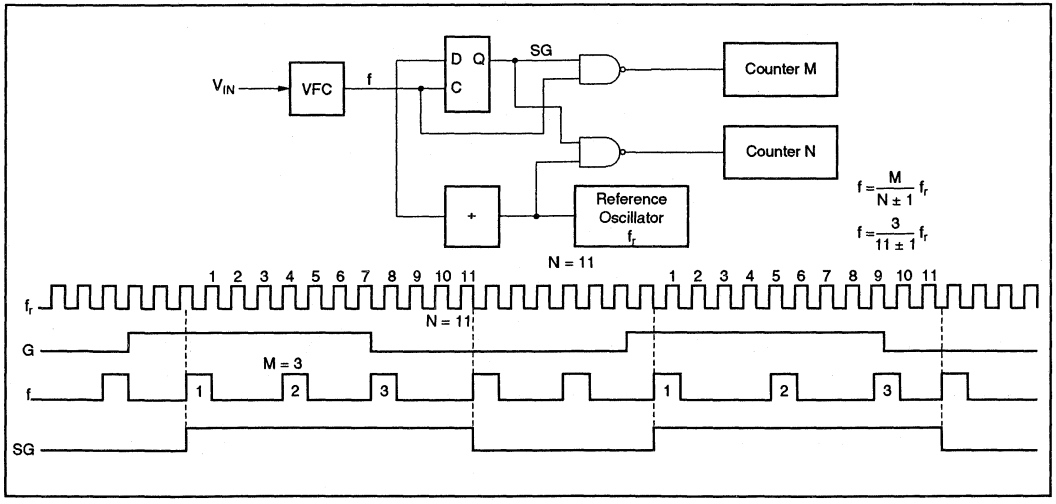
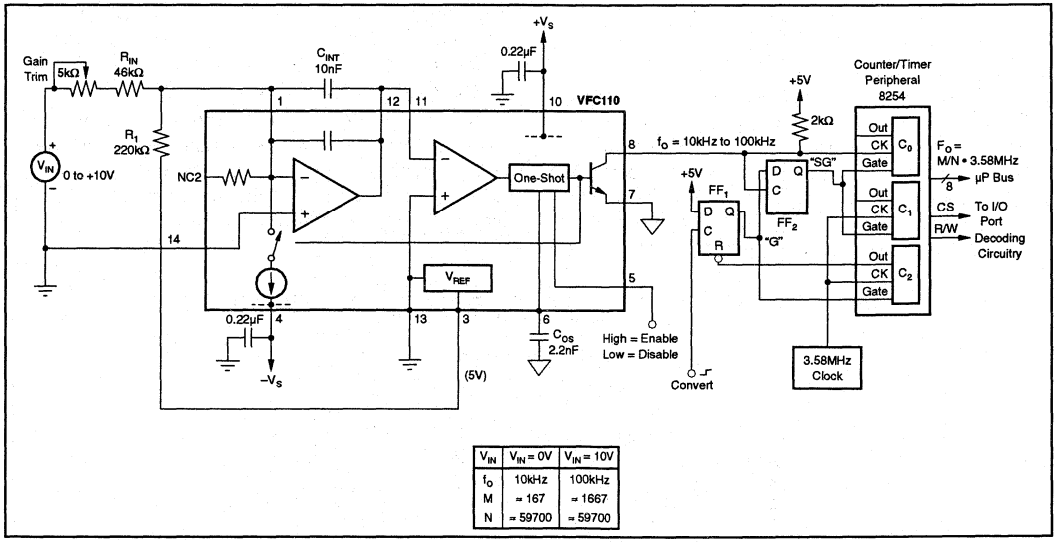


FIGURE 2. The Ratiometric Counting Scheme in This Simplified Diagram Synchronized a Gate Period to the Unknown Input Frequency from the VFC. The synchronized gate is then used to count the high frequency reference. The ratio of the exact count of M VFC pulses and the reference count, N, provide a more accurate measure of the unknown frequency.



V_{IN}	V_{IN} = 0V	V_{IN} = 10V
f_O	10kHz	100kHz
M	= 167	= 1667
N	= 59700	= 59700

FIGURE 3. The VFC Input is Offset in this Practical Example so that Low Input Can Be Converted in Short Times. Now the N count always remains near 59,700 over the full input range, while the M count ranges from 167 to 1667.

"G" to an integer number of VFC pulses, creating the synchronized gate "SG" Counter. C0 tallies the exact number (M) of VFC pulses, while C1 simultaneously counts N high speed clock pulses.

Conversion to a digital result is completed by reading the contents of counters C0 and C1 by the microprocessor. The VFC frequency is computed in software as the ratio of M and N times the clock frequency. The proper choice of counter modes programmed in the setup of the 8254 peripheral allows counters C0 and C1 to be automatically reset at the initiation of the next conversion cycle. The Convert command can be created by hardware timing or other peripheral hardware can be used to initiate the conversion process with software control.

The seemingly odd gate period time of 16.66ms has a definite purpose. Since the integration period of the VFC is equal to the counting period, an interfering signal can be rejected by counting for one period (or an integer number of periods) of the interfering signal. Line frequency noise (60Hz) can thus be rejected by counting for 1/60 second or 16.66ms. Figure 4 shows the noise rejection of an A/D converter with an integrating (counting) period of T as a function of frequency. Using a gate period of 16.66ms, the deep nulls in the response curve align with the fundamental and all harmonics of 60Hz. The shorter gate periods feasible with ratiometric counting make the precise choice of the gate period important if good line frequency rejection is to be achieved. With long gate times the line frequency noise is far down the attenuation slope where reasonable noise integration is achieved without great concern as to the precise gate period. Since the actual counting period is determined by the synchronized gate, SG, actual gate times will depend on the input VFC frequency and how the pulses randomly align with the gate. Worst case, however, occurs at low input voltage where the maximum deviation of the synchronized gate time from desired 16.66ms to equal to one period of the VFC at 10kHz or 0.1ms. Even this worst-case deviation from the ideal gate period still yields over 40dB rejection of 60Hz and its harmonics.

Conversion data is available 16.66ms after a convert command is issued, yet the counter resolution is one part in

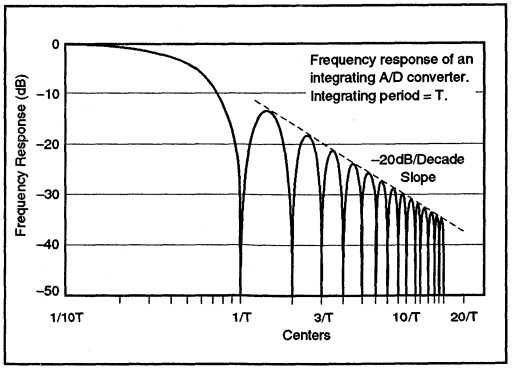


FIGURE 4. The Frequency Response of an Integrating A/D Converter Exhibits a Comb Filter Response. The deep nulls in the response are very useful for rejecting a known interfering signal and its harmonics.

59,667. Using standard counting, it would take 0.5 second to achieve the same resolution.

In principle, the resolution which can be achieved with ratiometric counting can be improved simply by increasing the frequency of the 3.58MHz reference clock. For the same 16.7ms counting period, a higher reference frequency would produce a correspondingly larger number of N counts, increasing the resolution of the result. (The 8254 is limited to 16 bits per counter, but counters could be cascaded for more resolution.) At some point, however, frequency noise (jitter) in the output of the VFC will limit the useful resolution of the result. At this point, counting with greater resolution will produce results which vary from conversion to conversion, affected by random jitter of the VFC.

Figure 5 shows the count repeatability due to frequency noise for a typical VFC110 as measured with a high-speed counter. It shows the repeatability for a 16.66ms counter gate time to be better than 18 bits—consistent with the 16 bit count used in this example.

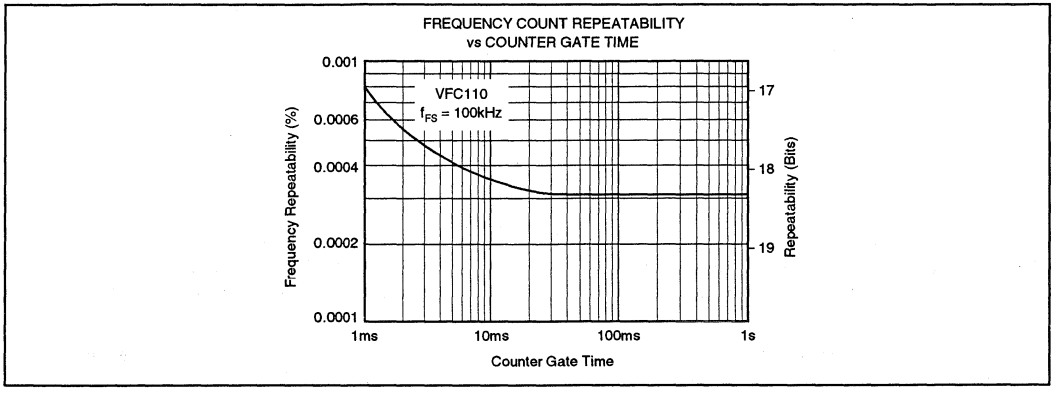


FIGURE 5.

BURR-BROWN®
APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

FREQUENCY-TO-VOLTAGE CONVERSION

By R. Mark Stitt and Rod Burt (602) 746-7445

Precision frequency-to-voltage converters (FVC)s can be made using voltage-to-frequency converters (VFCs). Burr-Brown offers a complete line of precision free-running VFCs.

VFC110 High frequency, low jitter VFC
4MHz max full-scale, ±0.02% typ linearity at 2MHz

VFC121 Precision single-supply VFC (+4.5V to +36V)
1.5MHz max full-scale, 0.03% max nonlinearity at 100kHz

VFC320 Precision VFC
1MHz max full-scale, 0.005% max nonlinearity at 10kHz

This bulletin describes three techniques for making a precision FVC using a VFC. The standard technique has high precision, but high ripple or slow settling. Adding an output filter can improve the settling-time, ripple trade-off, but adds error. A third new technique can eliminate ripple from the FVC output and improve settling time by more than 1000/1 as compared to the conventional FVC. Moreover, the DC precision is unaffected.

FVC APPLICATIONS

A rapidly-growing application for frequency-to-voltage converters is high-voltage analog signal isolation. High-voltage analog isolation amplifiers (ISO Amps), such as the Burr-Brown ISO121, are available for isolating signals up to 8000V. Higher voltage isolation of tens-of-thousands or even millions of volts as in utility-power-transmission line monitoring, nuclear event monitoring, and protection from lightning strikes calls for other techniques. You can get virtually unlimited isolation by using a voltage-to-frequency converter (VFC) to digitize an analog signal and transmit it over a fiber-optic data link to a FVC where the signal is reconstructed.

Many times VFCs are favored for analog-to-digital conversion because of their integrating input characteristic and high resolution (modern Sigma-delta analog-to-digital converters are really a variation of a VFC with digital filtering and encoding). An analog signal digitized by a VFC can be transmitted to a remote receiver serially over a single twisted pair wire cable or isolated with a single optical isolator. At the other end, the digital signal can be both

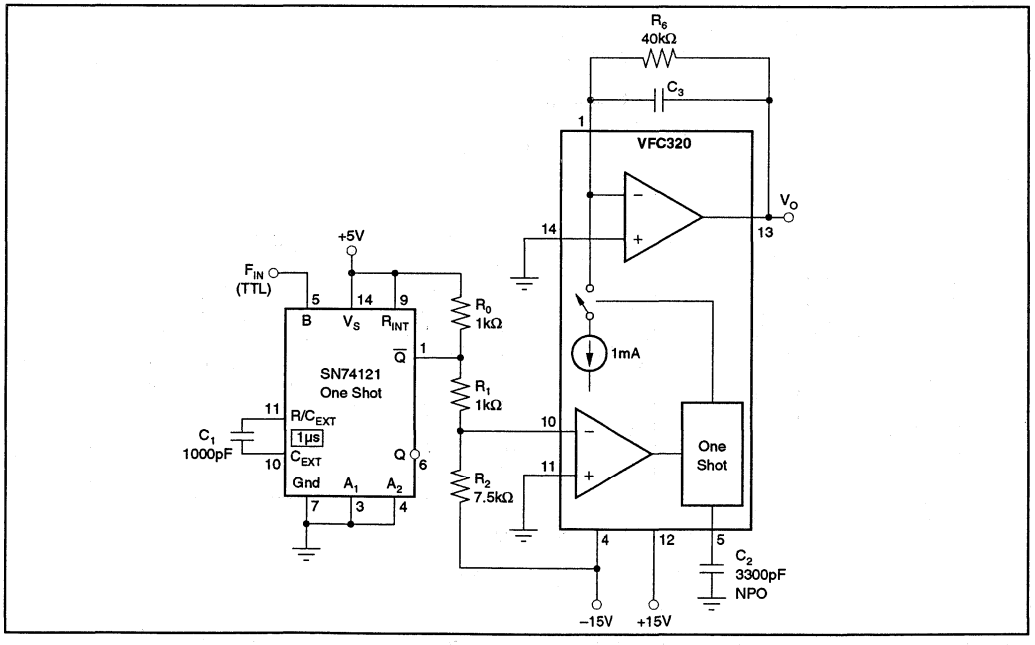


FIGURE 1. A Conventional Frequency-to-Voltage Converter. This FVC can be made by connecting a Burr-Brown VFC320 voltage-to-frequency converter in the FVC Mode. Select C_3 for ripple/settling-time trade off.

digitally processed and reconstructed to analog. An analog signal is often required, as in medical applications, for bedside monitoring on a CRT or LCD display. The fast-settling, ripple-free characteristics of the FVC described here makes it ideal for this application too.

THE CONVENTIONAL FVC

In an conventional FVC, a one-shot-controlled current reference is averaged. A serious problem with the conventional FVC results from a trade-off between ripple and settling time. Improved resolution from the FVC demands low ripple, but decreasing the ripple increases settling time.

An example of a conventional FVC circuit is shown in Figure 1. It uses a Burr-Brown VFC320 voltage to frequency converter connected in the FVC mode. The SN74121 one shot along with input resistors, R_1, R_2, and pull-up resistor R_0 convert a TTL-logic-level input into a 1µs negative-going pulse to trip the ground-referenced comparator in the VFC320. When tripped, the comparator triggers a precision one shot in the VFC320. When triggered, a 1mA current reference in the VFC320 is switched to the input of an averaging transimpedance amplifier for the period of the one shot.

The transimpedance amplifier can be thought of as an integrator consisting of an op amp in the VFC320 with an external integrating capacitor, C_3. A current proportional to the integrator output voltage is summed in through feedback resistor, R_6. Both the periodic 1mA current pulse and the current through R_6 are integrated in C_3. The average voltage at the output of the integrator is proportional to the input frequency, the precision one-shot period, the current reference, and the external feedback resistor, R_6.

The duration of the one-shot period is determined by the external one-shot capacitor, C_2. In this example, the one-shot pulse-width is set at 25µs for a full-scale FVC input range of 10kHz. It has been empirically determined that best VFC or FVC linearity is obtained when the one shot pulse width is approximatcly 25% of the full-scale input period.

The integrator output ramps up during the one-shot period, integrating the sum of the 1mA current source and the current through the feedback resistor. Then, the one-shot output ramps down during the balance of the input frequency period, integrating only the current through the feedback resistor. The peak-to-peak value of this ramp appears at the FVC output as ripple.

The value of the integrator capacitor affects the FVC output ripple, but does not affect the average DC output voltage. Increasing the value of the integrator capacitor decreases the voltage ripple, and increases the time for the integrator output to settle for a change in input frequency. Settling time follows a single pole response. The following relationships apply for the conventional FVC:

$$V_O = F_{IN} \bullet T_{OS} \bullet I_R \bullet R_6$$

(same for conventional and fast-settling FVC)

$$\text{RIPPLE} \approx T_{OS} \bullet I_R / C_3 \qquad \left(\frac{100\%}{P\%}\right)$$

$$t_S = R_6 \bullet C_3 \bullet \ln$$

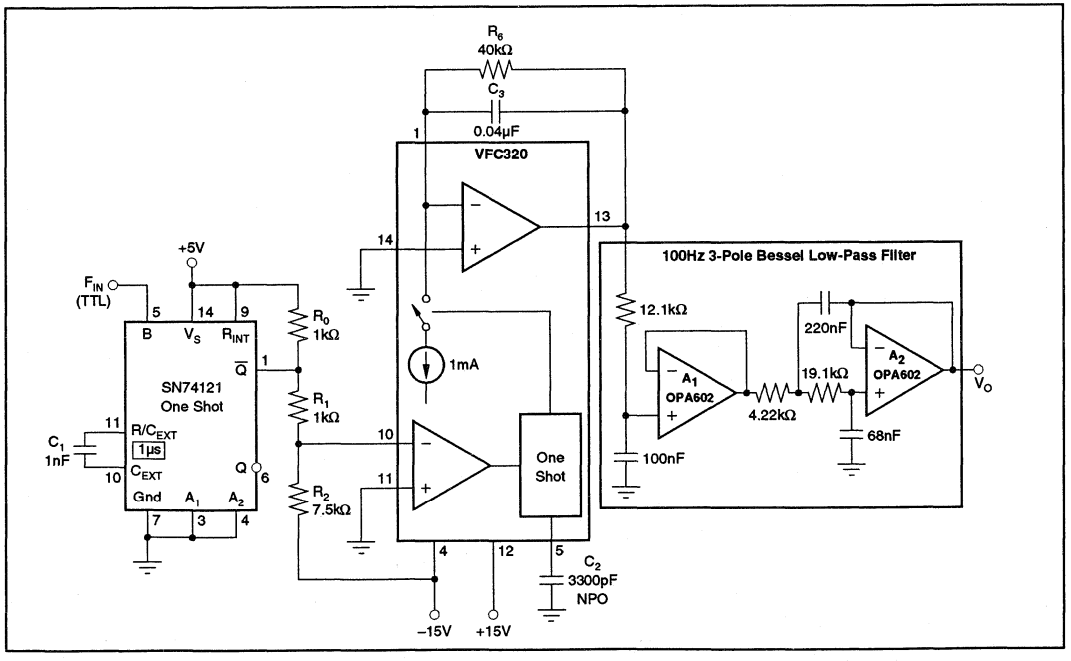


FIGURE 2. A Conventional Frequency-to-Voltage Converter. This converter with a 3-pole low-pass Bessel filter added to the output has less than 1mV ripple at 1.2kHz and can settle to 0.01% in 18ms.

Where:

V_O = Average output voltage [V]

F_{IN} = Input frequency [Hz]
(10kHz full-scale in this example)

I_R = Current reference [A]
(1mA for the VFC320)

T_{OS} = One-shot period [s]
(25µs in this example)

t_S = time for the output to settle to desired tolerance [s]

R_6 = Integrator feedback resistor [Ω]
(40kΩ for 10V full scale output with 10kHz input)

RIPPLE = Variation in V_O [Vp-p]

C_3 = Value of integrator capacitor [F]

P = Desired precision of the output signal
[% of full-scale]

CONVENTIONAL FVC PERFORMANCE

The conventional FVC has excellent DC performance, but poor dynamic performance. For example, consider an FVC with 10V full-scale output for 10kHz input. Using the VFC320 voltage-to-frequency converter with I_R = 1mA and T_{OS} = 25µs, R_6 must be 40kΩ. In the conventional FVC, for 0.01% resolution (1mV ripple), C_3 must be set to 25µF and settling time is an astoundingly long 9.2s.

FILTERING THE CONVENTIONAL FVC

In practice, the settling-time/ripple trade-off of the conventional FVC can be improved substantially by filtering the FVC output with a higher-order low-pass filter as shown in Figure 2. In this approach, a conventional FVC is designed with relatively high output ripple to give fast settling time. Then a high-order low-pass filter is added in series with the FVC output to reduce the ripple.

In the Figure 2 example, a value of 40kΩ was used for R_6 to set a 10V full-scale output for a 10kHz input. A value of 0.04µF is used for C_3 giving approximately 625mV max ripple. This is an arbitrary but adequate value to give excellent linearity and a 10V full-scale output. Higher ripple would reduce the linear output range of the FVC because, at full-scale output, the FVC must swing 10V plus approximately one half the ripple voltage.

There are many output filter possibilities for a filtered FVC. Because of its excellent pulse response a Bessel filter gives the fastest settling of any standard filter type. The tables below show examples of FVC performance for Bessel filters of order 2 through 5. The 3-pole Bessel filter gives a good settling-time complexity trade-off. Figure 2 shows the conventional FVC with a 3-pole Sallen-Key Bessel filter. With the filter f_{-3dB} frequency set to 100Hz, ripple at 1.2kHz is below 1mV and settling time to 0.01% is 18ms. Notice that ripple increases dramatically below 1.2kHz when higher-order filters are used.

The Sallen-Key filter architecture, used for the low-pass filter, was selected for low gain error. You can't include the filter in the feedback loop because the excessive phase-shift would cause instability. Since the filter must be added outside the integrator feedback loop, DC errors such as gain offset and offset drift add to the transfer function of the FVC.

FILTERED FVC PERFORMANCE WITH BESSEL FILTER

FILTER ORDER	f-3dB (Hz)	SETTLING (0.01%) (ms)	RIPPLE (at 1.2kHz) (mV)	RIPPLE (at 400Hz) (mV)
2	35	38	1	8
3	100	18	1	25
4	155	17	1	59
5	205	17	1	134

In the unity-gain Sallen-Key architecture, the op amps are connected as voltage-followers so gain error is negligible. You still must use low-drift precision op amps to reduce offset and offset drift errors.

Other active filters can be designed with easy-to-use DOS-compatible programs available free of charge from Burr-Brown—request the FilterPro™ filter design software. These programs make it easy to design a wide variety of practical Sallen-Key, Multiple Feedback (MFB), and State-Variable active filters up to tenth order. State-Variable active filters use the UAF42 monolithic Universal Active Filter which contains on-chip precision capacitors so that external capacitors are not required.

The filtered FVC gives a good improvement in settling time. However, even with the complexity of a 3-pole filter, its performance pales in comparison to the fast-settling FVC. Filtering, with a 3-pole filter, can give 18ms settling to 0.01% with less than 1mV ripple at 1.2kHz, but ripple increases at lower frequencies. For comparison, the new fast-settling FVC, using the same R_6, C_3 values, settles to 0.01% in 7.4ms with less than 1mV ripple at any frequency.

THE NEW FAST-SETTLING FVC

Instead of using a filter in series with the output, the fast-settling FVC uses a sample/hold amplifier inside the integrator feedback loop of the conventional FVC. One way to think of the fast-settling FVC is as a conventional FVC with an adaptive N-pole filter in its feedback. The order, N, of the adaptive filter approaches a very high value so that all integrator output ripple is removed regardless of input frequency. By comparison, the output ripple of the filtered FVC increases with decreasing frequency. Also, delay of the adaptive filter is low so that it can be included in the feedback loop to the integrator without adversely affecting stability. This is not possible with a conventional filter. With the filter included in the feedback loop, DC filter errors (sample/hold errors) such as gain, offset, and offset drift are divided-down by the loop gain of the integrator amplifier to negligible levels.

The fast-settling FVC is shown in Figure 3. For comparison to the filtered FVC, the same values are used for R_6 and C_3. In theory, a smaller value could be used for C_3 in the fast-settling FVC for better settling time. Ripple at the output is eliminated by using a sample/hold to sample the VFC320

integrator output. The only constraint on ripple voltage is that it must be within the linear output-swing range of integrator amplifier. Gain can be added in the sample/hold circuit to reduce the peak amplitude needed from the integrator output. In the filtered approach, added gain would also gain-up the ripple.

In the fast-settling FVC, the sample/hold acquires a feedback signal from the integrator output ramp in approximately 1µs so that the ripple of the ramp is translated to a higher frequency and substantially eliminated by a simple single-pole high-frequency filter, R_5, C_5. The delay through the high-frequency filter is low enough so that it can also be included in the feedback loop.

Since the sample/hold is in the feedback loop of the integrator, trigger timing is unimportant. The feedback loop automatically adjusts the relative level of the integrator output signal for proper alignment with the trigger pulse.

The sample/hold circuit in Figure 3 is controlled by the SN74121 one-shot through a SN7406 open-collector inverter connected as a level shifter. Pull-down resistor R_8 is added at the output of the integrator amplifier to boost output drive to the sample/hold capacitor, C_4.

Design of the sample/hold is greatly simplified because DC accuracy is unimportant. The complete sample/hold circuit consists of a common DMOS FET, Q_1, hold capacitor, C_4, and FET-input op amp, A_1. High frequency sampling glitches are also filtered out by the R_5, C_5 output filter. Since the glitch filter is also in the integrator feedback loop, associated DC errors are eliminated, and low DC output impedance is maintained.

Sample/hold gain is set to 2.0V/V by R_3 and R_4. The sample/hold gain attenuates (by two) the maximum output excursion necessary from the VFC320 integrator output, allowing both a comfortable +10V full-scale output from the FVC and a large ripple signal at the integrator output.

Gain in the feedback loop of the integrator also increases slew rate and bandwidth. With a high slew-rate op amp used for A_1, FVC slew rate is limited by the integrator op amp. Adding a gain of two in the feedback loop doubles the FVC slew rate. The actual sample/hold gain is not critical. Because it is in the feedback loop, gain errors in the sample/hold circuit do not affect the gain of the FVC or degrade its accuracy.

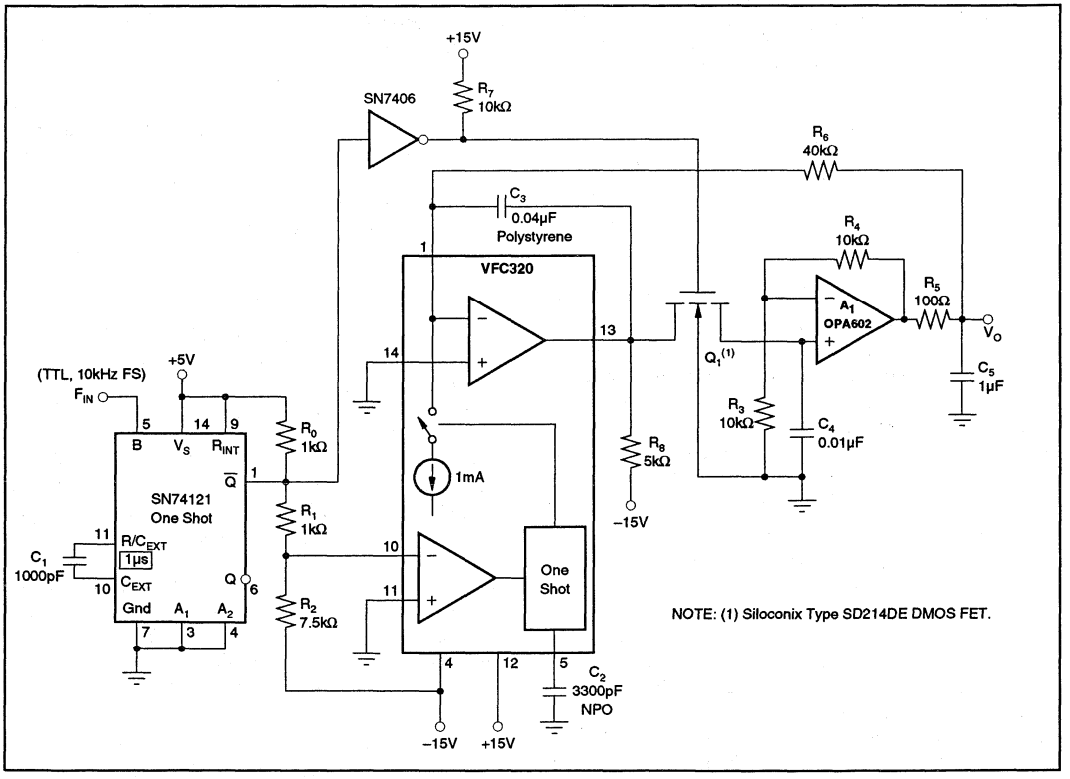


FIGURE 3. Fast-Settling Frequency-to-Voltage Converter. This converter is formed by adding a sample/hold in the feedback loop of the conventional FVC. It can settle to 0.01% in 7.4ms without ripple. Because the sample/hold is in the feedback loop, FVC precision is unaffected.

FAST-SETTLING FVC PERFORMANCE

The fast-settling FVC has the same DC transfer function as the simple FVC, but with neglegable ripple at the output. Measured DC performance of the Figure 3 FVC circuit gave nonlinearity better than 10ppm (better than 16 bits).

The scope photo in Figure 4 shows the excellent small signal ±1V (actually +6V to +8V) output step response for the FVC with a 6kHz to 8kHz input frequency change. If phase margin were low, this signal would exhibit overshoot and ringing.

Settling time of the fast-settling time FVC approximates that predicted by a single-pole system boosted by the gain in the feedback loop:

$$T_S = \ln\left(\frac{100\%}{P\%}\right) \cdot R_6 \cdot C_3/GAIN$$

Where:

GAIN = Gain of sample/hold circuit in feedback loop of integrator [V/V]

With $R_6 = 40k\Omega$, $C_3 = 0.04\mu F$, and GAIN = 2.0V/V as shown in Figure 3, 7.4ms settling to 0.01% is predicted. The scope photo in Figure 5 shows good agreement between theoretical and measured settling time for a large signal +1.2V to +10V output step due to a 1.2kHz to 10kHz input frequency change. The scope photo shows the residual error signal superimposed on the theoretical output signal. Each graticule division is approximately 0.01%.

The circuit used to measure settling time is shown in Figure 5A. A +1.2V to +10V square wave is applied to the input of both a VFC and to a precision difference amplifier. This square-wave input is the theoretical output signal—shown as one of the two traces on the scope photo Figure 5. The VFC converts the input voltage square wave into a modulated TTL-level 1.2kHz to 10kHz frequency signal. The frequency signal feeds directly into the FVC under test. The output of the FVC, ideally a delayed reproduction of the input square wave, feeds into the inverting input of the difference amplifier. The difference amplifier subtracts the FVC output from the VFC input. The output of the difference amplifier, (FVC output)-(VFC input) is the residual error signal—shown as the second trace on scope photo Figure 5. For this method to work, the VFC must have small dynamic error compared to the FVC. The VFC used in these measurements was the Burr-Brown VFC320.

Scope photo Figure 7 is a picture of a sine-wave modulated 1kHz to 9kHz TTL-level (0V to 5V) FVC input signal superimposed on the 1V to 9V FVC output. This photo was taken by driving a 1V to 9V sine-wave signal into the Figure 5A test circuit and looking at the FVC input and output. At the lower 1kHz frequency input, the steps between frequency input pulses can be seen on the sine-wave output showing excellent settling between pulses.

DISCUSSING STABILITY OF THE FAST-SETTLING FVC

Stability in sampled systems depends on sampling frequency. Since the sample/hold in the feedback loop of the fast-settling FVC is controlled by the input frequency, there is a minimum input frequency required to assure loop

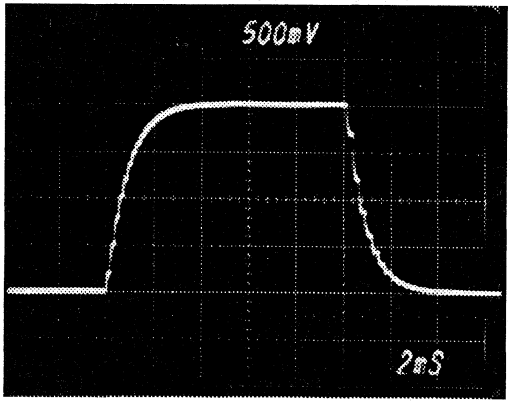


FIGURE 4. Small-Signal Step Response of the Fast-Settling FVC Shows Excellent Stability.

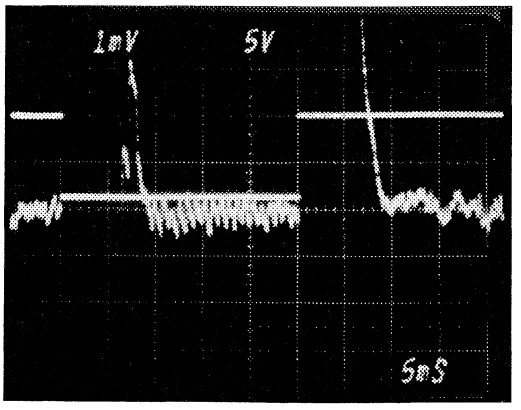


FIGURE 5. Settling Residue of the Fast-Settling FVC Confirms 0.01% Settling is Approximately 7.4ms.

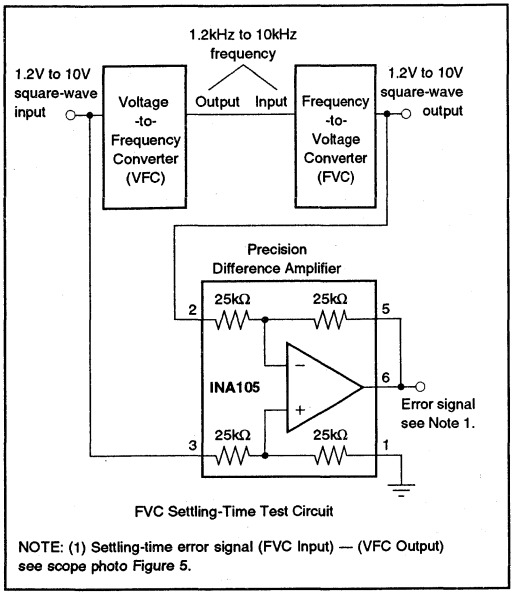


FIGURE 5A. FVC Settling-Time Measurement Circuit Used for Figure 5.

stability. As input frequency decreases, delay through the sample/hold increases thereby decreasing phase margin of the integrator loop. The feedback loop block diagram shown in Figure 6 gives a fairly accurate stability-criteria analysis. Phase margin of the loop is as follows:

$$MARGIN = 180° - 90° - delay_1 - delay_2 - delay_3$$

Where:

MARGIN = phase margin of the loop

90° = phase delay of the R_6, C_3 dominant pole

$delay_1$ = delay of sample-hold switch, Q_1, and hold capacitor, C_4

$delay_1 = Tan^{-1}(f_{UG} \bullet 2 \bullet \pi \bullet R_{Q1} \bullet C_4)$

$delay_2$ = delay due to R_5, C_5 output filter

$delay_2 = Tan^{-1}(f_{UG} \bullet 2 \bullet \pi \bullet R_5 \bullet C_5)$

$delay_3$ = delay due to sample period

$$delay_3 = \frac{360 \bullet f_{UG}}{2 \bullet f_{IN}}$$

f_{UG} = unity-gain frequency of the overall integrator loop

$f_{UG} = GAIN/(2 \bullet \pi \bullet R_6 \bullet C_3)$

GAIN = gain of the sample/hold circuit in the feedback loop

Solving for f_{IN},

(See Equation Below)

Where, in addition to previous definitions:

R_{Q1} = On-resistance of sample/hold switch-transistor, Q_1 [Ω]

Substituting the values from Figure 3, and using 25Ω for R_{Q1}, gives the following results:

MARGIN (°)	F_{IN} (Hz)
60	1200
45	780
30	600
0	400

For best pulse response and settling time the minimum input frequency should be 1.2kHz for the Figure 3 circuit example. At input frequencies below 400Hz, the loop will be unstable and the output will oscillate or lock-up.

$$f_{IN} = \frac{-90° \bullet Gain}{\pi \bullet C_3 \bullet R_6 \left(Margin - 90° + \tan^{-1}\left(\frac{Gain \bullet R_5 \bullet C_5}{R_6 \bullet C_3} \right) + \tan^{-1}\left(\frac{Gain \bullet R_{Q1} \bullet C_4}{R_6 \bullet C_3} \right) \right)}$$

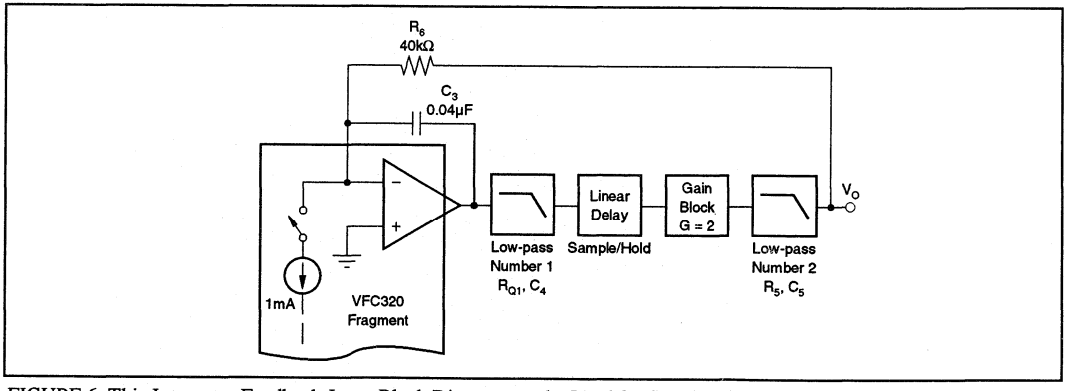


FIGURE 6. This Integrator Feedback-Loop Block Diagram can be Used for Stability Analysis of the Fast-Settling FVC.

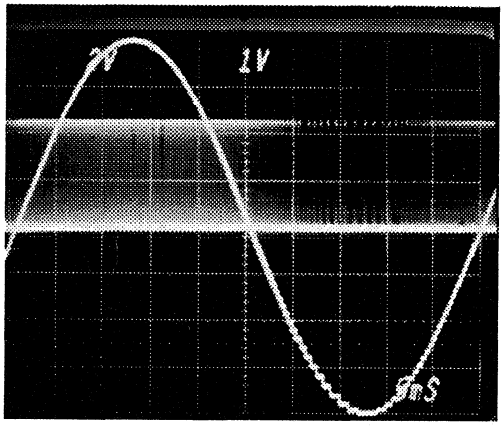


FIGURE 7. Dual-Trace Scope Photo Showing Frequency-to-Voltage Converter 1V to 9V Output for a 1kHz to 9kHz TTL-Level Frequency Input.

Model Index

Bulletins that feature the indicated Burr-Brown products are shown in **boldface**. Bulletins listed in normal typeface use the indicated product, but may not specifically feature it or explain its operation.

For Immediate Assistance, Contact Your Local Salesperson

Burr-Brown North American Distributor Sales Offices

ALABAMA
Insight Electronics
Huntsville, AL
205-830-1222
800-677-7716

ARIZONA
Insight Electronics
Tempe, AZ
602-829-1800
800-677-7716

ARKANSAS
Insight Electronics
Richardson, TX
214-783-0800
800-677-7716

North Star Electronics
Carrollton, TX
214-980-2999
800-882-6418

CALIFORNIA
Insight Electronics
Sunnyvale, CA
408-720-9222
800-677-7716

Insight Electronics
Westlake Village, CA
818-707-2101
800-677-7716

Insight Electronics
Irvine, CA
714-727-3291
800-677-7716

Insight Electronics
San Diego, CA
619-587-1100

J.I.T. Supply
Brea, CA
714-256-9100

COLORADO
Insight Electronics
Englewood, CO
303-649-1800
800-677-7716

CONNETICUT
North Star Electronics
Wilmington, MA
508-657-5155
800-635-3724

GEORGIA
Insight Electronics
Duluth, GA
404-717-8566
800-677-7716

IDAHO
Insight Electronics
Kirkland, WA
206-820-8100
800-677-7716

ILLINOIS
Insight Electronics
Schaumburg, IL
708-885-9700
800-677-7716

INDIANA
Insight Electronics
Schaumburg, IL
708-885-9700
800-677-7716

LOUISIANA
Insight Electronics
Richardson, TX
214-783-0800
800-677-7716

North Star Electronics
Carrollton, TX
214-980-2999
800-882-6418

MAINE
Insight Electronics
Burlington, MA
617-270-9400
800-677-7716

North Star Electronics
Wilmington, MA
508-657-5156
800-635-3724

MASSACHUSETTS
Insight Electronics
Burlington, MA
617-270-9400
800-677-7716

North Star Electronics
Wilmington, MA
508-657-5156
800-635-3724

MINNESOTA
Insight Electronics
Edina, MN
612-897-0464
800-677-7716

MONTANA
Insight Electronics
Kirkland, WA
206-820-8100
800-677-7716

NEW HAMPSHIRE
Insight Electronics
Burlington, MA
617-270-9400
800-677-7716

North Star Electronics
Wilmington, MA
508-657-5156
800-635-3724

NEVADA
(Nothern)
Insight Electronics
Sunnyvale, CA
408-720-9222
800-677-7716

(Southern)
Insight Electronics
San Diego, CA
619-587-1100
800-677-7716

J.I.T. Supply
Brea, CA
714-256-9100

NEW MEXICO
Insight Electronics
Tempe, AZ
602-829-1800
800-677-7716

NEW YORK (Upstate)
North Star Electronics
Wilmington, MA
508-657-5155
800-635-3724

OHIO
Insight Electronics
Cleveland, OH
216-467-7526
800-677-7716

OKLAHOMA
Insight Electronics
Richardson, TX
214-783-0800
800-677-7716

North Star Electronics
Carrollton, TX
214-980-2999
800-882-6418

OREGON
Insight Electronics
Beaverton, OR
503-644-3300
800-677-7716

PENNSYLVANIA
North Star Electronics
Langhorne, PA
215-750-7733

RHODE ISLAND
Insight Electronics
Burlington, MA
617-270-9400
800-677-7716

North Star Electronics
Wilmington, MA
508-657-5156
800-635-3724

TEXAS
Insight Electronics
Austin, TX
512-331-5887
800-677-7716

Insight Electronics
Richardson, TX
214-783-0800
800-677-7716

Insight Electronics
Sugarland, TX
713-448-0800
800-677-7716

North Star Electronics
Carrollton, TX
214-980-2999
800-882-6418

UTAH
Insight Electronics
Englewood, CO 80112
303-649-1800
800-677-7716

WASHINGTON
Insight Electronics
Kirkland, WA
206-820-8100
800-677-7716

WISCONSIN
Insight Electronics
Schaumburg, IL
708-885-9700
800-677-7716

WYOMING
Insight Electronics
Kirkland, WA
206-820-8100
800-677-7716

CANADA
SEMAD
Burnaby, British Colombia
604-451-3444

SEMAD
Calgary, Alberta
403-252-5664

SEMAD
Markham, Ontario
905-475-3922

SEMAD
Pointe Claire, Quebec
514-694-0860

SEMAD
Ottawa, Ontario
613-526-4866

Or, Call Customer Service at 1-800-548-6132 (USA Only)

Burr-Brown North American Sales Offices and Sales Representatives

BURR-BROWN CORPORATION
PO Box 11400
Tucson, AZ 85734
Telephone: 602-746-1111
Fast Product Info:
800-548-6132
Fax: 602-741-3895

ALABAMA
Rep, Inc.
205-881-9270 Huntsville, AL

ALASKA
Wilson Electronics Sales Team
206-946-8016 Federal Way, WA

ARIZONA
Summit Sales
602-998-4850 Scottsdale, AZ

ARKANSAS
Burr-Brown Corporation
214-783-4555 Dallas, TX

CALIFORNIA
I Squared, Inc.
408-988-3400 Santa Clara, CA

Burr-Brown Corporation
818-991-8544 Agoura Hills, CA
714-835-0712 Santa Ana, CA

COLORADO
Sales Technology, Inc.
303-530-9409 Fort Collins, CO

CONNECTICUT
Burr-Brown Corporation
617-229-0300 Burlington, MA

DELAWARE
Delta Technical Sales
215-957-0600 Hatboro, PA

FLORIDA
Marathon Technical Assoc.
305-785-0072 Pompano, FL
813-725-3199 Clearwater, FL
407-872-5775 Orlando, FL

GEORGIA
Rep, Inc.
404-938-4358 Tucker, GA

HAWAII
Burr-Brown Corporation
714-835-0712 Santa Ana, CA

IDAHO
Wilson Electronics Sales Team
206-946-8016 Federal Way, WA

ILLINOIS
Sumer, Inc.
708-991-8500
Rolling Meadows, IL

Hitec Central, Inc.
314-291-5920 Bridgeton, MO

Rep Associates Corporation
319-373-0152 Cedar Rapids, IA

INDIANA
LM Devoe Co.
317-842-3245
Indianapolis, IN

IOWA
Rep Associates Corporation
319-373-0152 Cedar Rapids, IA

KANSAS
Hitec Central, Inc.
816-796-6684
Independence, MO

KENTUCKY
LM Devoe Co.
317-842-3245
Indianapolis, IN

LOUISIANA
Burr-Brown Corporation
214-783-4555 Dallas, TX

Development Technical
Sales, Inc.
713-988-6546 Houston, TX

MAINE
Burr-Brown Corporation
617-229-0300 Burlington, MA

MARYLAND
Marktron, Inc.
301-251-8990 Rockville, MD

MASSACHUSETTS
Burr-Brown Corporation
617-229-0300 Burlington, MA

MICHIGAN
Burr-Brown Corporation
708-437-2877
Arlington Heights, IL

MINNESOTA
Electronic Sales Agency, Inc.
612-884-8291 Bloomington, MN

MISSISSIPPI
Rep, Inc.
205-881-9270 Huntsville, AL

MISSOURI
Hitec Central, Inc.
314-291-5920 Bridgeton, MO

816-796-6684
Independence, MO

MONTANA
Front Range Marketing
801-288-2500 Murray, UT

NEBRASKA
Hitec Central, Inc.
816-796-6684
Independence, MO

NEVADA
I Squared, Inc.
408-988-3400 Santa Clara, CA

Summit Sales
602-998-4850 Scottsdale, AZ

NEW HAMPSHIRE
Burr-Brown Corporation
617-229-0300 Burlington, MA

NEW JERSEY
J-Square Marketing
516-935-3200 Hicksville, NY

Delta Technical Sales
215-957-0600 Hatboro, PA

NEW MEXICO
Summit Sales
602-998-4850 Scottsdale, AZ

NEW YORK (METRO AREA)
J-Square Marketing
516-935-3200 Hicksville, NY

NEW YORK (UPSTATE)
Elcom Sales Inc.
716-385-1400 Pittsford, NY
315-685-8967 Syracuse, NY

NORTH CAROLINA
REP, Inc.
919-469-9997 Morrisville, NC

615-475-4105 Jefferson City, TN

NORTH DAKOTA
Electronic Sales Agency, Inc.
612-884-8291 Bloomington, MN

OHIO
Versatron Inc.
216-944-0082 Willoughby Hills, OH

OKLAHOMA
Burr-Brown Corporation
214-783-4555 Dallas, TX

OREGON
Wilson Electronics Sales Team
206-946-8016 Federal Way, WA

PENNSYLVANIA
Delta Technical Sales
215-957-0600 Hatboro, PA

Versatron Inc.
216-944-0082 Willoughby Hills, OH

RHODE ISLAND
Burr-Brown Corporation
617-229-0300 Burlington, MA

SOUTH CAROLINA
REP, Inc.
615-475-4105 Jefferson City, TN

SOUTH DAKOTA
Electronic Sales Agency, Inc.
612-884-8291 Bloomington, MN

TENNESSEE
Rep, Inc.
615-475-4105 Jefferson City, TN

Rep, Inc.
205-881-9270 Huntsville, AL

TEXAS
Burr-Brown Corporation
214-783-4555 Dallas, TX

Development Technical
Sales, Inc.
713-988-6546 Houston, TX

UTAH
Front Range Marketing
801-288-2500 Murray, UT

VERMONT
Burr-Brown Corporation
617-229-0300 Burlington, MA

VIRGINIA
Marktron, Inc.
301-251-8990 Rockville, MD

WASHINGTON
Wilson Electronics Sales Team
206-946-8016 Federal Way, WA

WASHINGTON, D.C.
Marktron, Inc.
301-251-8990 Rockville, MD

WEST VIRGINIA
Versatron Inc.
216-944-0082 Willoughby Hills, OH

WISCONSIN
Sumer, Inc.
414-784-6641 Brookfield, WI.

Electronic Sales Agency, Inc.
612-884-8291 Bloomington, MN

WYOMING
Front Range Marketing
801-288-2500 Murray, UT

CANADA
Dynasty Components
Ottawa, Ontario
613-596-9800

Vancouver, British Colombia
604-657-4433

Calgary, Alberta
403-560-1212

Toronto, Ontario
416-672-5977

Montreal, Quebec
514-843-1879

For Immediate Assistance, Contact Your Local Salesperson

Burr-Brown International Sales Offices and Sales Representatives

BURR-BROWN CORPORATION
International Sales
PO Box 11400
Tucson, AZ 85734
Telephone (1) 602-746-1111
Fax (1) 602-741-3895
Telex 066-6491 BURRBROWN ATU

AUSTRALIA
Kenelec Pty. Ltd.
Victoria (61) 3 560-1011

AUSTRIA
Burr-Brown Research Gesm.b.H.
Vienna (43) 1 602 63 71

BELGIUM
Microlink N.V.
Brussels (32) 2 5218650

BRAZIL
Aplicacoes Electronicas
Artimar Ltda.
Sao Paulo (55) 11 231-0277

CANADA
Dynasty Components
Ottawa, Ontario
613-596-9800

CHILE
Instrumentacion y Controles
Santiago (56) 2 225 1848

CHINA
Schmidt & Co. (H.K.) Ltd.
Wanchai (852) 5070222

COLOMBIA
Instrumentacion Ltda.
Bogota (57) 1 6121313

DENMARK
Prescom A/S
Lynge (45) 42 189800

FINLAND
Perel Oy
Hyvinkaa (358) 14 434600

FRANCE
Burr-Brown International S.A.
Le Chesnay
(33) 1 39 54 35 58
Lyon (33) 78 64 09 77
Toulouse (33) 61 40 03 06

GERMANY
Burr-Brown Int. GmbH
Filderstadt (49) 711 77040
Bremen (49) 421 25 39 31
Düsseldorf (49) 21 54 84 45
Erlangen (49) 91 31 2 40 36
Frankfurt (49) 61 54 8 20 81
München (49) 89 61 77 37

GREECE
Peter Caritato and Assoc. S.A.
Athens (301) 9020115

HONG KONG
Schmidt & Co. (H.K.) Ltd.
Wanchai (852) 507 0222

Jetronic Technology Ltd.
Aberdeen (852) 873-2810

HUNGARY
Siex Elektronikelemente
Zirndorf, Germany (49) 911 60-7014

INDIA
Oriole Services & Consultants
Pvt. Ltd.
Bombay (91) 22 511 3621

ISRAEL
Gallium Electronics (1986) Ltd.
Ramat-Hasharon
(972) 3 5402242

ITALY
Burr-Brown Int. S.r.l.
Milano (39) 2 580 10504

JAPAN
Burr-Brown Japan Ltd.
Atsugi (81) 462 48 4695
Osaka (81) 6 305 3287
Nagoya (81) 52 775 6761
Tokyo (81) 33 586 8141

MALAYSIA
Serial System Pte. Ltd.
Singapore (65) 280-0200

MEXICO
Borcla, S.A. de C.V.
Mexico City
(52) 5 7031751

NETHERLANDS
Burr-Brown International B.V.
Maarssen (31) 3465 50204

NEW ZEALAND
Enertec Services Ltd.
Auckland (64) 9 479-2377

NORWAY
Hefro Elektronikk A/S
Oslo (47) 22 67 68 00

POLAND
Delta Tech
Warsaw (48) 22 465370

PORTUGAL
Ibertronics, LDA
Amadora (34) 1542504

PUERTO RICO
Marathon Technical Assoc.
Mayaguez (809) 831-4050

SINGAPORE
Serial System Pte. Ltd.
Singapore (65) 280-0200

SLOVENIA
I & R Electronic
Ljubljana (38) 61 222007

SOUTH AFRICA
Advanced Semiconductor
Devices (Pty) Ltd.
Johannesburg (27) 11 444-2333

SOUTH KOREA
KML Corporation
Seoul (82) 2 595-9101

SPAIN
Unitronics, S.A.
Madrid (34) 1 5425204

SWEDEN
Bexab Sweden AB
Taeby (46) 8 630 8800

SWITZERLAND
Burr-Brown AG
Rueschlikon
(41) 1 7240928

TAIWAN
Alpha Precision
Instrumentation Corp.
Taipei (886) 2 508-3066

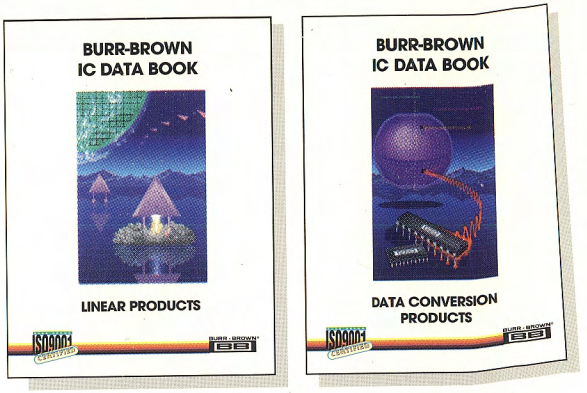
New Mercury Industrial Corp.
Taipei (886) 2 397-5565

TURKEY
Inter Muhendislik,
Danismanlik ve Ticaret A.S.
Istanbul (90) 1 349 9400

UNITED KINGDOM
Burr-Brown Int. Ltd.
Watford (44) 923 233837

VENEZUELA
Autotrol Tecnologia C.A.
Caracas (58) 2 241-6214

Also available —



Linear and Data Conversion Product IC Databooks

Burr-Brown Corporation

Street Address:
6730 S. Tucson Blvd.
Tucson, AZ 85706

Mailing Address:
P.O. Box 11400
Tucson, AZ 85734-1400

Tel: (602) 746-1111
Twx: 910-951-1111
Cable: BBRCORP
Telex: 066-6491

For immediate product information,
contact your local Burr-Brown
sales representative,
or call (USA only)
Toll-Free **1-800-548-6132.**
Fax: (602) 741-3895

BURR - BROWN®

BURR-BROWN ISO9001 CERTIFIED